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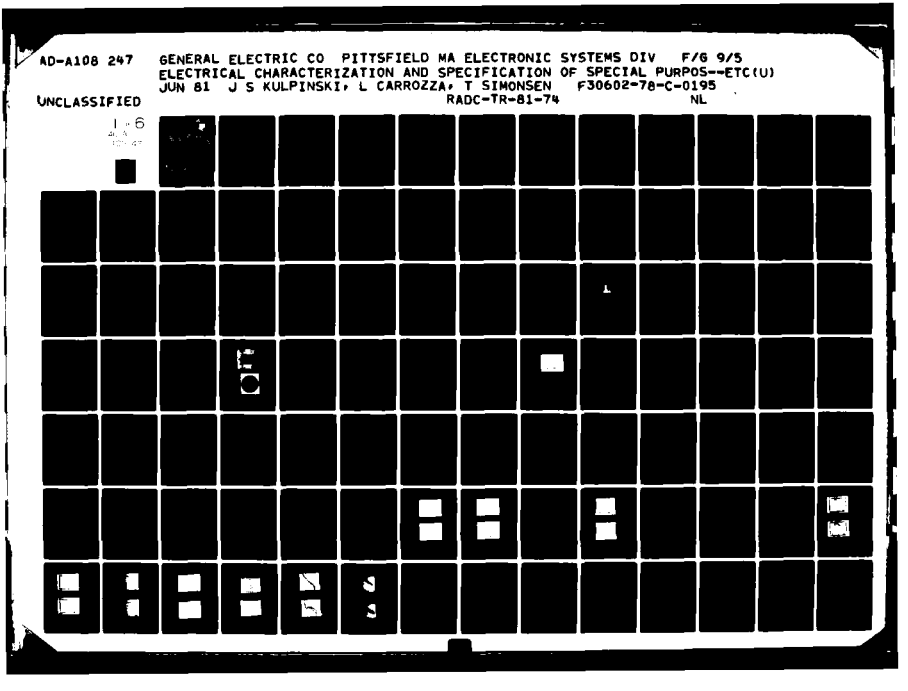

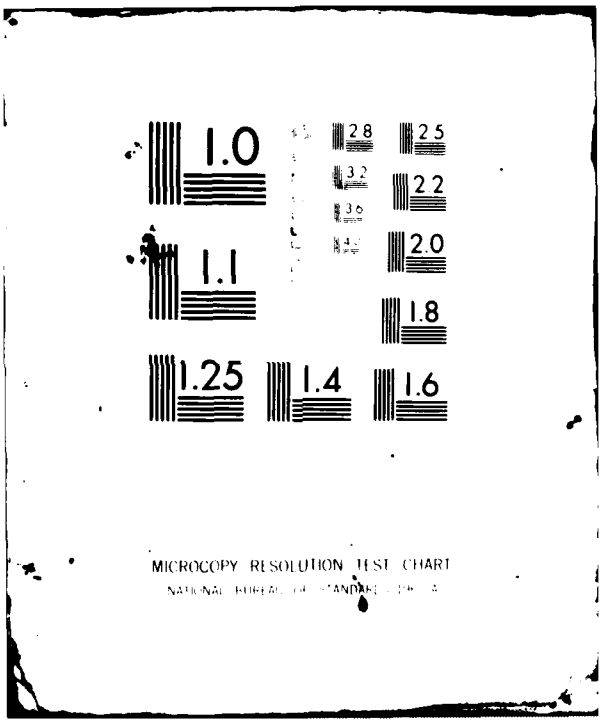
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MICROCOPY RESOLUTION TEST CHART

LEVEL II

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RADC-TR-81-74
Final Technical Report
June 1981

ELECTRICAL CHARACTERIZATION AND SPECIFICATION OF SPECIAL PURPOSE LINEAR MICROCIRCUITS

General Electric Ordnance Systems

John S. Kulpinski

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

This report has been reviewed by the RADC Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RADC-TR-81-74 has been reviewed and is approved for publication.

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Linear Microcircuit	Comparators	
Characterization	D/A Converters	
Op Amps	A/D Converters	

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report covers the work performed by General Electric, Ordnance Systems pertaining to the electrical characterization and MIL-M-38510 specification of linear microcircuits. The period of report is August 1978 to October 1980. This technical report is divided into chapters covering specific device types with electrical characterization, test methodology and results discussed. The following device types/families were characterized with the resulting slash sheets depicted:

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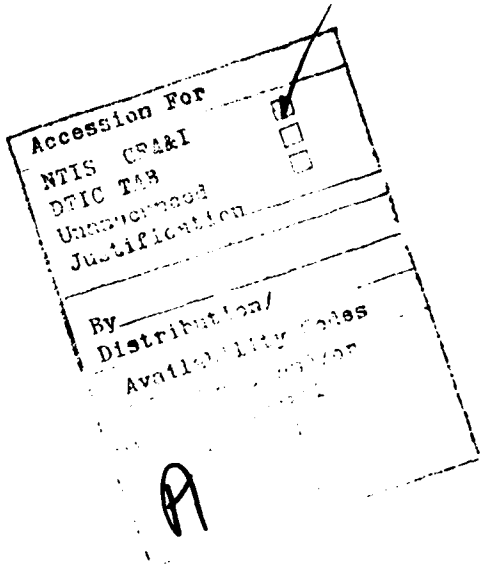
Device Family	Commercial Type Nos.	Slash Sheet
Adjustable Positive Voltage Regulators	78G, 78MG, LM117H, LM117K LM150K, LM138K	/117
Adustable Negative Voltage Regulators	79G, 79MG, LM137H, LM137K	/118
BiFet Operational Amplifiers	LF155/6/7, LF155A/6A/7A	/114
Multiple BiFet Operational Amplifiers	TL061/2/4, TL071/2/4 LF151/3	/119
Voltage References	LM129A, LM199A	/124
Programmable Voltage References	AD584S, AD584T	/128
12 Bit A/D Converters	MN5200 & MN5210 family	/120
12 Bit D/A Converters	562, 563	/121
Sample/Hold Amplifiers	LF198, 5537	/125

Data obtained during device characterization is published in handbook form obtainable under separate cover from this document. However, samples of data sheets, histograms, and plots, are included in this report.



PREFACE

This report was prepared by General Electric Ordnance Systems, 100 Plastics Avenue, Pittsfield, Massachusetts, for Rome Air Development Center, Griffiss Air Force Base, Rome, New York, under contract F30602-78-C-0195. It covers the period from Sept. 1978 to Sept. 1980. An interim Technical Report (RADC-TR-80-49) was prepared in 1979 (dated May 1980) covering in detail the work accomplishments for the first year's effort. This final report focuses upon the work accomplished in the second year ending September 1980; highlights from the first year are also included.

The work on this project was performed by the Electronic Circuits Engineering Operation of Ordnance Systems. Project responsibility was held by Mr. John Kulpinski of Circuit Design Engineering. Key individuals who made significant contributions to this work effort were Messrs. Louis Carrozza, Theodore Simonsen, Donald Van Alstyne of Circuit Design Engineering and Messrs. Larry Deluca, John Dunn, Robert Mossman, Daniel Mui, Jamie Schwehr, George Smith and Thomas Wetzel of Circuit Test Engineering.

Mr. Thomas Dellecave, RBRA, is the Project Engineer at RADC for this contract.

ELECTRICAL CHARACTERIZATION AND SPECIFICATION OF SPECIAL PURPOSE LINEAR MICROCIRCUITS

List of Sections

Acronyms and Symbols

A,amp	Ampere
AD	Analog Devices
A/D	Analog-to-Digital
ADC	Analog-to-Digital converter
AE	Gain error
AVS(+/-)	Open loop voltage gain (single-ended, 0 to +, 0 to -)
BPO	Bipolar offset
BPOE	Bipolar offset error
BW	Bandwidth
BWE	Bit weight errors
ΣBWE	Sum of the bit weight errors
BZE	Bipolar Zero Error
Clk	Clock
CM	Common mode
CMR	Common mode rejection
CMOS	Complememtary metal oxide semiconductor
CPW	Clock pulse width
CS	Channel Separation
d,D	Delta
D/A	Digital to Analog
DAC	Digital to Analog Converter
dB	Decibel
DBPO/DT	Bipolar offset drift
DBZ/DT	Bipolar zero drift
delta VR/delta T	Reference voltage temperature coefficient
delta VR/delta t	Reference voltage long term stability
delta VR (current)	Reference voltage change versus output current
delta VR (temp cycle)	Reference voltage temperature cycling hysteresis
DESC	Defense Electronics Supply Center
DIIO/Dt	Input offset current/temperature coefficient
DISCD (line)	Standby current drain change versus line voltage (regulators)
DISCD (load)	Standby current drain change versus load current (regulators)
DIP	*Dual inline package*
DIZS/Dt	Zero scale current drift
DSE	Dynamic sampling error (S/H)
DUT	Device Under Test
DVFS/Dt	Gain error drift
DVIN/DVOUT	Ripple rejection
DVIO/DT	Input offset voltage temperature coefficient
DVOUT/DIL	Load transient response

DVOUT/DVIN	Line transient response
DVR/DT	Reference voltage temperature coefficient
DVM	Digital voltmeter
E(T)	A/D converter transition voltage bit error in LSB.
E(MC)	A/D converter major or minor carry error in LSB.
E(N),ET(N)	Bit transition error at address N
en(S)	Breadboard noise (sample mode)
en(H)	Breadboard noise (hold mode)
Eo	Test circuit output voltage error (D/A converter)
eirms	RMS input voltage (regulators)
eorms	RMS output voltage (regulators)
E.O.C.	End of convert status.
E.O.S.	End of search status.
FRR	Feedthrough rejection ratio
FRRAC	Feedthrough rejection ratio , A.C. input
FS	Full scale
FSR	Full scale range
FSV,VFS	Full scale voltage
FSVR,VFSR	Full scale voltage range
FTE	Feedthrough error (MDAC)
fts	Settling time of step response to specified accuracy
G	Gain of test circuit error amplifier (D/A converters)
GE	General Electric Company
GEOS	General Electric Company, Ordnance Systems
GND	Ground
HEX	**Hexadecimal**
HL	High limit
Hz	Hertz,cycles per second
Iadj,IADJ	Adjustment pin current (regulators)
IADJ (line)	Adjustment pin current line voltage regulation
IADJ (load)	Adjustment pin current load current regulation
IIBK	Input breakdown current
+ICC,Icc	Positive supply input current
ICH(+)	Hold capacitor charging current (+ input)
ICH(-)	Hold capacitor charging current (- input)
Icont, ICTL	Control pin current (regulators)
IEE,Iee	Negative supply input current
IFS	Full scale current
IHL(+)	Leakage current into hold with + charge
IHL(-)	Leakage current into hold with - charge
+IIB	Input bias current, non-inverting input

-IIB	Input bias current, inverting input
IICL	Input clamp diode current limit
IIH	High level input current (digital)
IIL	Low level input current (digital)
IIO	Input offset current
IL	Load current
ILOG,Ilog	Logic power supply input current
IMAX	Maximum current
IMIN	Minimum current
IOFF	Strobe current for VSTBOFF
ION	Strobe current for VSTBON
IOS(+)	Output short circuit current (for positive output)
IOS(-)	Output short circuit current (for negative output)
IOSC	Output short circuit current (regulators)
Ipk	Peak output current
Ipeak	Peak output current with forced output voltage (regulators)
IQ	Quiescent current (regulators)
IR	Voltage reference input current
IREF,Iref	Reference voltage supply current
IS	Temperature stabilizer supply current
ISCD	Standby current drain (regulators)
ISI	Initial temperature stabilizer supply current
IZS	D/A zero scale current
IZS'	D/A complementry zero scale current
JAN	Joint Army Navy
JC-41	JEDEC Committee on Linear Integrated Circuits
JEDEC	Joint Electron Devices Engineering Council
JFET	Junction Field Effect Transition
K	Kilo
L,LE	Linearity error (Endpoint)
LE (BF)	Linearity error (Best Fit)
LL	Low limit
ln	Natural logarithm
LSB	Least significant bit of a D/A or A/D converter
LSI	Large Scale Integration
LTPD	Lot Tolerance Percent Defective
M	Monotonicity
M,m	Milli
mA	Milliampere
MAX (+)	Maximum positive analog input voltage
MAX (-)	Maximum negative analog input voltage
MC,MCE(N)	Major carry error (at the Nth transition)
MDAC	Multiplying D/A Converter
min	Minute,minimum
MPCAG	Military Parts Control Advisory Group

MSB	Most significant bit of a D/A or A/D converter
mV	Millivolt
N,n	Nano
NA,nA	Nanoamperes
Ni(BB)	Breadboard noise
No	Output noise voltage
Ni(PC)	Popcorn noise
+ NL	Summation of maximum positive bit weight errors
- NL	Summation of maximum negative bit weight errors
NSC	National Semiconductor Corporation
NT	Transition uncertainty (A/D converters)
OS	(GE) Ordnance Systems
P,P	Pico
PD,Pd	Quiescent power dissipation
PDA	Percent defective allowable
pk	Peak
PPM	Parts per million
PPM/C	Parts per million per degree celsius
+PSRR	Power supply rejection ratio, positive supply
-PSRR	Power supply rejection ratio, negative supply
+PSS	Power supply sensitivity,positive supply
-PSS	Power supply sensitivity,negative supply
PWA, PWB,...	Pulse width of pulse A, etc.
QPL	Qualified Product List
RADC	Rome Air Development Center
REF DAC	Reference Digital-to-Analog Converter
RF, Rf	Amplifier feedback resistor
RI	Amplifier input scanning resistor
Ri	*Input resistance*
RSC	Series charge resistance
RL	Load resistance
s,sec	Second
SA	Successive approximation
SAR	Successive approximation register
SC	Start convert
S/H	Sample and hold circuit
S/N	Serial number
SO	Serial output (A/D converters)
SR(+)	Slew rate (max dVo/dt), positive
TA	Ambient temperature
tap	Aperture time (S/H)
taq	Acquisition time (S/H)
Tc	Case temperature

tc,tCT	Conversion time for an A/D Converter
T.C.	Temperature coefficient
td	Delay time
tpHL	High to low propagation delay time
tpLH	Low to high propagation delay time
TR(tr)	Transient response, rise time
TR(ts)	Transient responsea, settling time (S/H)
TR(os)	Transient response, overshoot
ts (power)	Settling time, power up (voltage references)
ts (strobe)	Settling time, strobe up (voltage references)
tSHL	Settling time, high-to-low
tSLH	Settling time, low-to-high
tTHL	Digital signal fall time
tTLH	Digital signal rise time
TTL	Transistor - transistor logic
T2L	Transistor - transistor logic
u	Micro
uA	Microamperes
uF	Microfarad
uV	Microvolt
us	Microsecond
V	Volts
Vadj	Adjustment pin voltage (regulators)
VBE	Base-to-emitter voltage
Vcc	Positive supply voltage
Vcm	Command mode voltage
Vcont	Control pin voltage (regulators)
Vee	Negative supply voltage
VF	Forced voltage
VFS,VFSI	Gain error (Full Scale) (D/A Conv.)
+VFS	Positive full scale voltage
-VFS	Negative full scale voltage
VFSE	Absolute accuracy
VHC	Hold capacitor voltage (S/H)
VHS	"Hold" step voltage
Vi(N)	Ideal analog voltage at the input of A/D converter for an output address code of N
VIH	Logic "1" input voltage
VIL	Logic "0" input voltage
VIN	Input voltage, digital input voltage for D/A and A/D converters
VIN (a)	Analog input voltage for A/D converters
VIN/VOUT	Ripple rejection (regulators)
VIO	Input offset voltage
VIO	Zero error (A/D converters)
VIO ADJ(+)	Adjustment for input offset voltage
Vlog	Logic supply voltage (A/D converters)
VM	Measured signal voltage

Vo	Analog output voltage
VOH	Output voltage, high level (digital)
VOI(n)	D/A output voltage on straight line between zero and FS for address n
VOL	Output voltage, low level (digital)
VOM(n),VM(N)	D/A converter output voltage measured for address N
VOP	Output voltage swing (peak)
VoSTB	Output voltage for VSTB=0.4V
VOUT	Voltage output
VOUT/VIN	Line voltage transient response
VOUT/IL	Load current transient response
VOUT(RECOV)	Regulator output recovery voltage after output short to ground
VR, VREF	Reference voltage
VRDAC(n)	Reference D/A converter output for address n
VRLINE	Line regulation
VRLOAD	Load regulation
VROS	Reference D/A output offset voltage
VRTH	Thermal voltage regulation
VS	Temperature stabilizer voltage (voltage references)
+VS	Positive supply voltage
VS/H	Logic command (S/H)
VSTART	Voltage start-up
VSTBON	Strobe voltage for delta Vo=-10mV
VSTBOFF	Strobe voltage for Vo=+10mV
VTH	Logic threshold voltage
Vz	Zener voltage (voltage references)
W	Watts
$\overline{X}$	Data mean of X
X-OR	Exclusive OR
Zi	Input impedance
ZD	Dynamic impedance
Zo	Output impedance
Zz	Zener impedance (voltage references)
oC	Degrees centigrade
σ	Sigma
θ	Thermal resistance

SECTION I

INTRODUCTION

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SECTION I

INTRODUCTION

Objectives

The overall objective of this work effort is to characterize and specify certain linear microcircuit devices for inclusion in MIL-M-38510 ("General Specification for Microcircuits") detailed slash sheets.

Generally, "characterization" of a device type includes several related tasks:

- o Assessment of test parameters, limits, and test conditions.
- o Development of test procedures and test circuits compatible with automatic test systems.
- o Analysis of limits and verification of test circuits via sample device testing and data evaluation.
- o Assessment of device performance, identification of anamolies.
- o Generation and verification of detailed burn-in life test circuits

Concurrent with characterization, detailed MIL-M-38510 slash sheet development includes:

- o Formulation of Table I, Electrical Performance Characteristics selection of test parameters required by military users and determination of test conditions and limits, compatible with automatic test methods and with device yield.

- o Formulation of Table II, Electrical Test Requirements; Table III, Group A Inspection; Table IV, Group C End Point Electrical Parameters.

- o Design of static and dynamic test circuits, terminal connection diagrams, steady-state power and reverse bias burn-in circuits, accelerated burn-in and life test circuits.

All of the above activity is either guided by or reviewed by the manufacturers of the devices involved, and by Rome Air Development Center (RADC).

Another objective of this effort is to provide follow-up support for maintaining existing linear MIL-M-38510 slash sheets to current status, including support to Rome Air Development Center for manufacturer qualification and related activities.

All of the characterization and specification effort performed is guided by the fundamental objectives of the JAN 38510 program - namely quality, reliability, interchangeability, and standardization

Scope of Applied Effort

The specific tasks included in this effort are the characterization and specification of the following generic device types:

- o Adjustable Positive Voltage Regulators
- o Adjustable Negative Voltage Regulators
- o Precision BIFET Op Amps
- o Multiple BIFET Op Amps (single, dual, quad)
- o 12-bit A/D Converters
- o 12-bit D/A Converters
- o Precision Voltage References
- o Programmable Voltage References
- o Precision Sample and Hold Circuits

Additional required tasks included:

- o Assessment of pending changes to existing MIL-M-38510 linear slash sheets.
- o Support to RADC in the evaluation of manufacturer qualification submittals.
- o Recommendation to RADC of devices types to be considered for MIL-M-38510 specification.
- o Review of MIL-M-38510 specifications generated by other activities (RADC, NASA).
- o Attendance at JC-41 Committee and Subcommittee meetings.
- o Survey of user needs and manufacturer recommendations for data converter specification development.

Background

General Electric Ordnance Systems, one of 166 operating product departments of the General Electric Company, develops and produces precision electromechanical and electronic military systems. Current activities include development, design and production of fire control and guidance systems for the Navy's TRIDENT Fleet Ballistic Missile program, the MK 73 Gun and Guided Missile Director (TARTAR), the MK 80 Director (AEGIS), the PHALANX close-in weapon system, MK 45 Gun Mounts, turret drive and stabilization systems for the Army's Infantry Fighting Vehicle, advanced torpedo propulsion, and jet engine controls.

As users of microcircuits for military systems, Ordnance Systems has also performed electrical characterization of certain linear, digital, and interface microcircuits for MIL-M-38510 specification under contracts to Rome Air Development Center. These specification activities date back to 1971 and include sixteen separate contracts.

General Electric began this current effort in MIL-M-38510 linear microcircuits in September of 1978, having previously completed similar characterization and specification contracts in 1976 and 1977. Philosophies for establishing parameters, limits, and test circuits for conventional devices like op amps, comparators, and regulators were developed and coordinated with RADC, DESC, and the device manufacturers.

This current effort extended past efforts to newer devices and to additional generic families, and in addition established important groundwork in the development of automatic tests and specifications for high-resolution (12-bit) data converters. However, previously-negotiated philosophies could not be applied directly to these markedly different generic families. (For example, an all-codes linearity test for a 12-bit data converter requires 4096 data points at each of 3 temperatures and two power supply levels.)

Currently there are approximately thirty completed and in-process linear/interface slash sheets in the MIL-M-38510 program. Six slash sheets are devoted to Op Amps, including the bipolar "standards", followers, BIFETs, quads, high-slew- rate, and lo-power and lo-noise BIFETs. Comparators, transistor arrays, and precision timers are contained in four slash sheets, as are CMOS and JFET analog switches. Voltage regulators are specified in six separate slash sheets, and precision voltaage references in two others. Three slash sheets are devoted to D/A Converters, and one each to A/D Converters, sample-hold, peripheral drivers, memory core drivers, and line drivers and receivers.

Development of Slash Sheets

A procedure for developing new slash sheets to MIL-M-38510 has evolved through negotiations among all concerned parties. Device selection is influenced by user needs, which is determined from the marketplace and from organized committees, such as the Military Parts Control Group (MPCAG) at DESC, the G12 Solid State EIA Device Committee, and the Microelectronics Project Group of the Electronics Systems Committee of AIA. These recommendations are balanced with manufacturer recommendations obtained via the JC-41 Committee on Linear Microcircuits. Devices of recent vintage, having high usage, multiple application potential in military systems, proven performance, and two or more sources are given priority. Single-source devices are acceptable, especially for hybrid devices, although multiple sources are preferred. Availability of devices, and expressed manufacturer interest in supporting slash sheet development, are additional important considerations. Manufacturers typically recommend devices for slash sheet action in JC-41 Committess, and then chair a JC-41 Subcommittee for preparation of slash sheet parameters, limits, and test circuits.

The industry data sheet forms the basis for the military specification parameters and limits. Typically, such data sheets do not specify all of the necessary parameters over the military temperature range and over the common mode voltage range. The JC-41 Subcommittee, or the device manufacturer, usually prepares a proposed spec which contains more information than the industry data sheet. Conflicting items are negotiated in committess or via direct contact with manufacturers.

Data provides another base for determining parameters and limits. Devices for test are purchased from distributors, are also obtained from manufacturers via RADC request. Test circuits, compatible with automatic test systems, are developed. The devices are tested on a Tektronix S3263 Automatic Test System at GE Ordnance Systems Electronic Test Center. Data obtained at -55°C, +25°C, and +125°C ambient is correlated to bench or vendor test data, analyzed, reduced and documented in data handbooks. Recommended limits are compared to the statistical sample data; parameter limits which are grossly inconsistent with the data are readily identified.

Specification additions, changes, and alternate approaches are discussed at the committee level. Device anomalies are identified in lab bench tests. Failure modes are also identified. User caution notes are added to the specification if it is deemed appropriate.

Burn-in circuits are usually recommended by the manufacturer and evaluated by RADC and/or GEOS on the available test samples. An objective is to minimize the number of external components while stressing the device near its limits.

Rough draft copies of the final slash sheet are prepared at GEOS and are forwarded to RADC for review. DESC distributes copies of this spec to manufacturers and users for final comments. Following assessment of the comments by all concerned parties, DESC prepares and issues the slash sheet.

Characterization Data

Data obtained during device characterization is usually published in handbook form separate from this document. Samples of the data sheets, histograms, and plots, are included in this report. The following data handbooks were published during this contract effort:

Characterization Data for MIL-M-38510/114, BIFET Op Amps
(Commercial Types LF 155, -156, -157) Nov 78

Characterization Data for MIL-M-38510/114, BIFET Op Amps
(Commercial Types LF155A, -156A, -157A) April 1979

Characterization Data for MIL-M-38510/119 Multiple BIFET Op Amps (Commercial Types TL 061, -062, -064, TL 071, -072, 074, uAF 771, -772, -774, LF 151, -153, -147) Oct 79

Characterization Data for MIL-M-38510/117 and /118, Positive and Negative Adjustable Voltage Regulators (78MG, 78G, 79MG, 79G) Dec 79

Characterization Data for MIL-M-38510/117 and /118, Positive and Negative Adjustable Voltage Regulators (LM117H, LM117K, LM137H, and LM137K) Dec 79

Characterization Data for MIL-M-38510/117, Positive Adjustable Voltage Regulators (LM150K and LM138K) May 80

Characterization Data for MIL-M-38510/121, 12-Bit D/A Converter (AD562 and HI562) May 80

Characterization Date for MIL-M-38510/125, Sample and Hold Circuits (LF198) Sept 1980

Characterization Data for MIL-M-38510/124, Precision Voltage References and MIL-M-38510/128, Programmable Voltage References (LM129A, LM199A; AD584) Nov 1980

Characterization Data for MIL-M-38510/120, 12-Bit A/D Converters (MN5200 and 5210 families) In process

Formal Meetings Attended (GE internal meetings not included)

JC-41 Committee on Linear ICs

Nov. 1, 2, 1978	-	Phoenix, AZ
Feb. 27, 28, 1979	-	Monterey, CA
June 19, 20, 1979	-	Washington, DC
Oct. 2, 3, 1979	-	Orlando, FL
Feb. 5, 6, 1980	-	Phoenix, AZ
June 10, 11, 1980	-	Washington, DC
Oct. 7, 8, 1980	-	Burlington, MA

JC-41 Subcommittee Meetings

Feb. 6, 1979	562 Converter Task Group	Peabody, MA
Feb. 7, 1979	5200 Converter Task Group	Peabody, MA
May 1, 1979	5200 Converter Task Group	Pittsfield, MA
May 29, 1979	5200 Converter Task Group	Sturbridge, MA
Aug. 14, 1979	CMOS D/A Converter Task Group	San Jose, CA
Aug. 15, 1979	Sample/Hold; Voltage References Task Group	San Jose, CA
Nov. 27, 1979	BIFET Op Amp Task Group	San Jose, CA
April 15, 1980	562 Converter Task Group	Pittsfield, MA
April 16, 1980	5200 Converter Task Group	Pittsfield, MA
Aug. 11, 1980	5200 Converter Task Group	Sturbridge, MA

RADC/GE Meetings

Sept. 21, 1979	Contract Plans	Pittsfield, MA
Feb. 22, 1979	Contract Status	Pittsfield, MA
May 2, 1979	Contract Status	Pittsfield, MA
May 22, 1979	Contract Status	Rome, NY
Aug. 8, 1979	Contract Status	Pittsfield, MA
Nov. 8, 1979	Contract Plans	Rome, NY
Nov. 29, 1979	Contract Plans	Pittsfield, MA
Mar. 4, 1980	Contract Status & Plans	Rome, NY
Aug. 13, 1980	Contract Status	Pittsfield, MA

Vendor Visits

Jan. 15, 1979 re 5200/562,	Analog Devices,	Wilmington, MA
Jan. 16, 1979 re 5200,	Micro Networks,	Worcester, MA
Nov. 26, 1979 re BIFET Op Amps,	Fairchild Semiconductor,	Mountainview, CA
Nov. 27, 1979 re 198,	National Semiconductor,	Santa Clara, CA

SECTION II

AUTOMATIC TEST DEVELOPMENT

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SECTION II
AUTOMATIC TEST DEVELOPMENT

2.1 Introduction

All the linear characterization efforts required the accumulation and subsequent reduction of vast amounts of test data. For both of these tasks, GE made extensive use of a Tektronix S-3260/70 test system and a Tektronix software development system. This section will describe the test system and the general approach to expanding its capabilities. A few displays of raw and of reduced data, which have been developed for the device evaluations, will also be shown. Although several of the data displays are somewhat standardized, many of the linear device types required the development of unique data displays in order to effectively illustrate device performance in an easily digestible form.

2.2 Tektronix S-3260/70 Test System Features

The model number S-3260/70 indicates that the test system has characteristics found in both the 3260 and 3270 systems. However at the time this report was written, the system was undergoing an upgrade which gave it the full capability of an S-3270.
The test system is fully equipped to provide a state-of-the-art engineering tool for device characterization. The CP1162 System Controller has the Date/Time Option that gives the ability to store date and time information in the directory and data files. System peripherals include a 4014 Graphics Display Terminal, two CP110 Disk Drives, a CP220 Reader/Punch, and LA180 Decprinter I and a 4631 Hard Copy Unit.

For voltage and current measurement and device stimulation, the system contains:

1804 Test Station, which contains many test functions and all electronics to interface the device under test (DUT) to the system.

2943/44 Clock Generators, which provide 10 driving and 4 comparing programmable phases.
Option 20 Waveform Digitizer, which provides the capability of converting 1000 points on a waveform to 10-bit digital values.

Once the waveform is thus stored in memory, software can be used to determine such things as rise time, overshoot, settling time, etc.

Six programmable voltage sources.

Two programmable current sources.

Temptronix 450A Temperature Chamber, which allows programmable DUT temperatures from -60 deg C to + 160 deg C.

IEEE Bus Interface Card, which allows the addition of IEEE 488 compatible equipment to the system.

With these hardware components, the test system has the following features:

Accommodates up to 128 active pins (64 input, 64 output)
Functional testing at 20 MHz; force, compare, mask and store at 20 MHz

DC Tests: Differential voltage measurements; force V, measure I; force I, measure V

Dynamic Testing: Repetitive and one-shot time measurements; functional preconditioning

GO/NO-GO and analytical test capability

On-line interactive program development

Digital waveform analysis (1 sample/picosecond)

DUT environmental control (-60 deg C to 160 deg C)

Data logging and reduction. Computer graphics display

2.3 Tektronix System Accuracy

The linear test programs were developed to utilize the internal Tektronix measurement/stimulus hardware as much as as possible. However for many measurements, the Tektronix system could not provide the required accuracy. In these cases, more accurate external equipment was utilized via the IEEE 488 Bus. Two disadvantages in using external equipment are:

1) additional core is required to store the 488 bus control routines and,

2) execution time for external functions is significantly longer than time to execute internal Tektronix functions.

Table 2.1 lists instruments which are available for use with the S-3260/70.

Table 2.1 IEEE-488 Interfaced Instruments.

Manufacturer	Model	Description
Fluke	8502A	Precision Digital Multimeter
Hewlett Packard	3455A	Precision Digital Voltmeter
Hewlett Packard	4262A	LCR Meter
Hewlett Packard	5328A	Universal Counter
Fluke	5100A	Calibrator
Kepco	488-122	Power Supply Programmer
ICS Electronics	4880	Instrument Coupler
Hewlett Packard	2240A	Measurement and Control Processor
North Atlantic	225	Phase Angle Voltmeter

Figures 2-1 through 2-13 illustrate the accuracies of the internal Tektronix measurement and stimulus functions. Also, for certain internal functions, the accuracy of the external equipment that provides the same function, is displayed for comparison.

On many occasions, neither the internal Tektronix equipment nor the external equipment had sufficient accuracy, or response time. These cases required test adapter circuitry to interface the device under test (DUT) to the test equipment. These cases will be described in the appropriate chapters covering the individual linear device types.

2.4 Correlation

Testing linear devices on the Tektronix system has required the implementation of many new test techniques. Each new technique, whether in the form of adapter circuitry or software, must be verified as accurate. In general, the first step of verification was to determine that the technique is designed to provide a measurement that is at least 10 to 1 times more accurate than the tolerance of the parameters. For instance a parameter of 5.0 volts plus or minus 10% must be measured by a meter that is at least accurate to plus or minus 1% when measuring 5.0 volts.

Verification of accuracy also included comparison of data taken by the new technique to data taken by an alternate method - usually on a bench circuit. When data from the two techniques did not agree, an analysis of error contributions was performed and corrections made if it was felt that the error was significant.

Correlation of Tektronix data from the sample/hold devices to bench and vendor data uncovered many discrepancies and resulted in several test program modifications to improve test techniques.

2.5 Data Reduction

The presentation of test results is extremely important in any characterization effort. Raw data printouts are required for record, but are usually not organized in a manner that enables one to scan them to assess general parameter trends.

Data Tables

For the linear devices, the first step in data reduction was organizing raw data into tables. Figure 2-14 and 2-15 illustrate two variations of data tables. Figure 2-14 illustrates data taken from sample/hold devices. Figure 2-15 is the form of table used for the 584 Voltage Reference. The left hand entries indicate the test parameters and test conditions. In Figure 2-14 the data from a particular device is entered in the column beneath the serial number of that device. In Figure 2-15, the data taken at various temperatures, for a single device, is entered in columns. Note that in both figures the low test specification limit for each parameter is on the left of the device data and the high specification limit is on the right hand side of the data. This enables the reader to more easily determine if a measurement on a device lies mathematically between the specification limits.

Data Summaries, Line Graphs

A large quantity of devices, such as the sample/hold or for devices such as the D/A and A/D with a large number of data points, data tables are too voluminous for a reader to mentally reduce and detect trends. Therefore the large quantities of data must also be presented in a summarized form.

Figure 2-16 is a line graph of an LF156 Op-Amp input bias current vs. common mode voltage. With this plot, one can easily see the relationship between the two parameters.

Figure 2-17 is a plot of linearity error (in LSBs) for all codes between 0 and 800. The plot is one of five sheets developed for each 562 D/A device. The linearity plots were very instrumental in verifying the effectiveness of an abbreviated linearity test for 562 devices. Although five seperate sheets were required for each device under each set of operating conditions, one set of sheets allows one to quickly assess qualitatively, the linearity error of 4096 codes.

Histograms

Tektronix software included a basic histogram routine which was modified by GE to provide the variations shown in Figures 2-18 and 2-19. Figure 2-18 has grouped eighty-one op-amp devices according to input bias current. The histogram differs from the basic Tektronix histogram in that the bars are filled in and are separated by a narrow non-darkened region. Figure 2-19, another histogram variation, groups the codes from a single D/A device, according to the magnitude of each code's error. This type of plot is very useful in comparing general linearity error characteristics of one device to another.

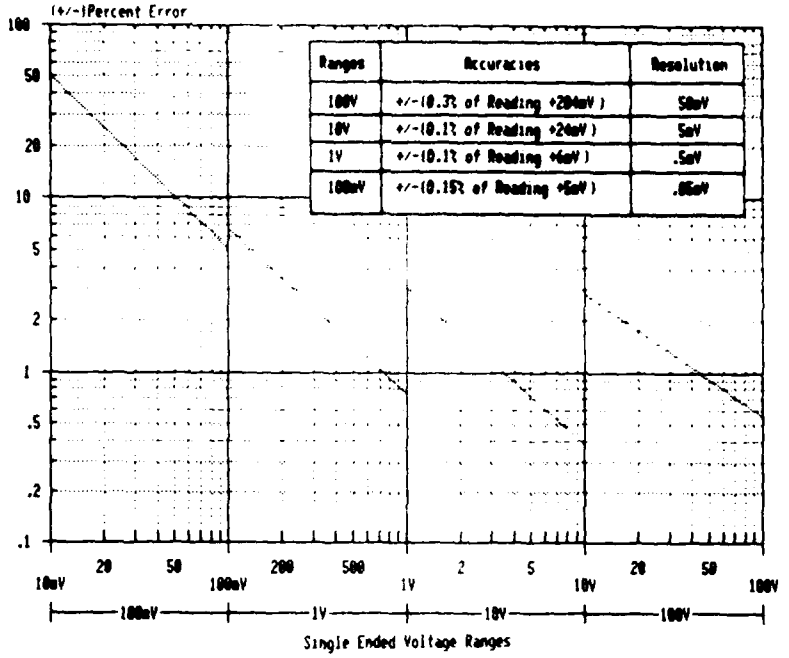

Figure 2-1. S3260/70 - Single Ended Voltage Accuracies

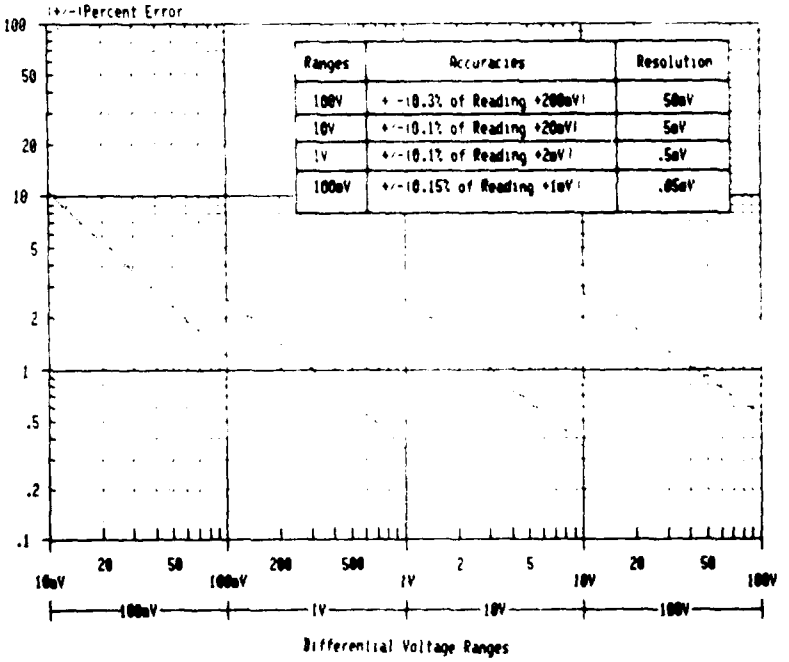

Figure 2-2. S3260/70 - Differential Voltage Accuracies

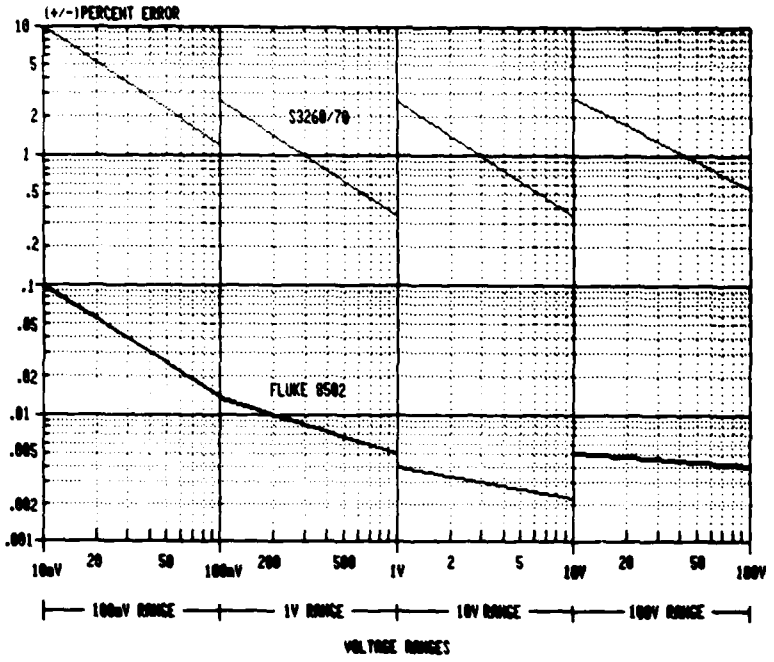

Figure 2-3a. S3260/70 - Diff. Meas. vs. Fluke 8502 DVM Accuracies

FLUKE DMM 8502A				
Range	Full Scale	Accuracies	Resolution	Settling Time
100mV	312mV	0.005% of Reading +8uV	1uV	2mS
1V	2.5V	0.004% of Reading +9uV	1uV	2mS
10V	20V	0.002% of Reading +90uV	10uV	2mS
100V	160V	0.004% of Reading +900uV	100uV	2mS

TEKTRONIX S3260/70 DIFF. VOLTAGE MEASUREMENTS				
Range	Full Scale	Accuracies	Resolution	Settling Time
100mV	102.2mV	+/-(0.15% of Reading+1mV)	0.05mV	4mS
1V	1.022V	+/-(0.1% of Reading+2mV)	0.5mV	.6mS
10V	10.22V	+/-(0.1% of Reading+6mV)	5mV	.6mS
100V	102.2V	+/-(0.3% of Reading+200mV)	50mV	1.2mS

Figure 2-3b. S3260/70 - 8502 DVM Specification Comparison

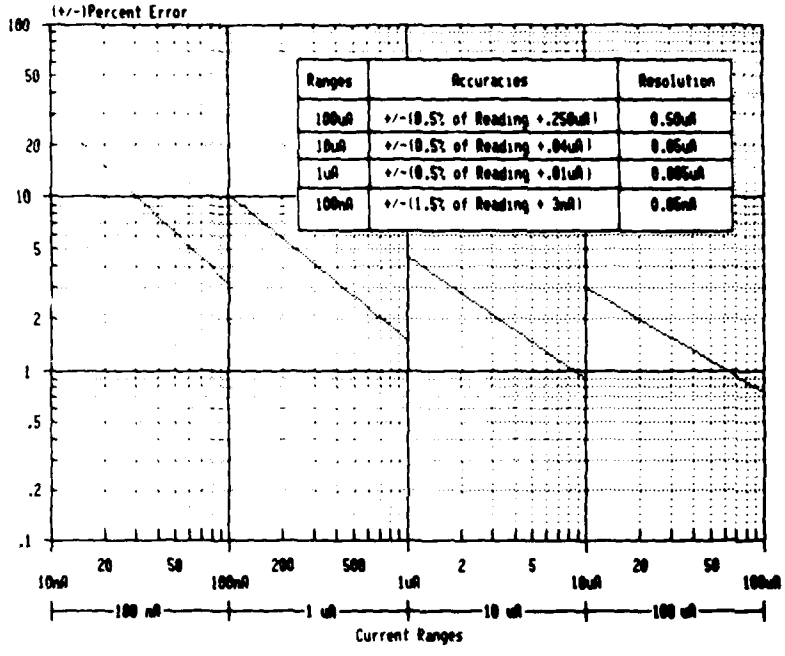

Figure 2-4. S3260/70 - Current Measurement Accuracies

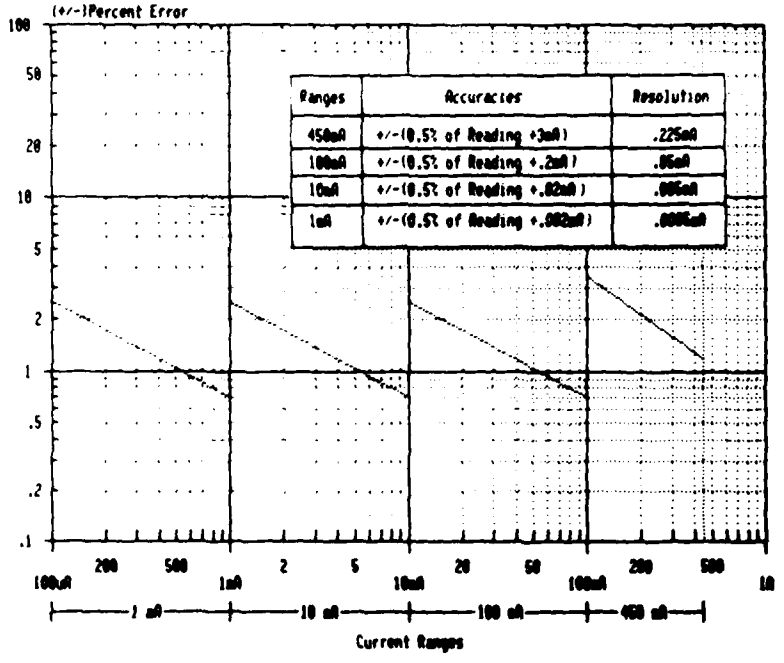

Figure 2-5. S3260/70 - Current Measurement Accuracies (Cont'd.)

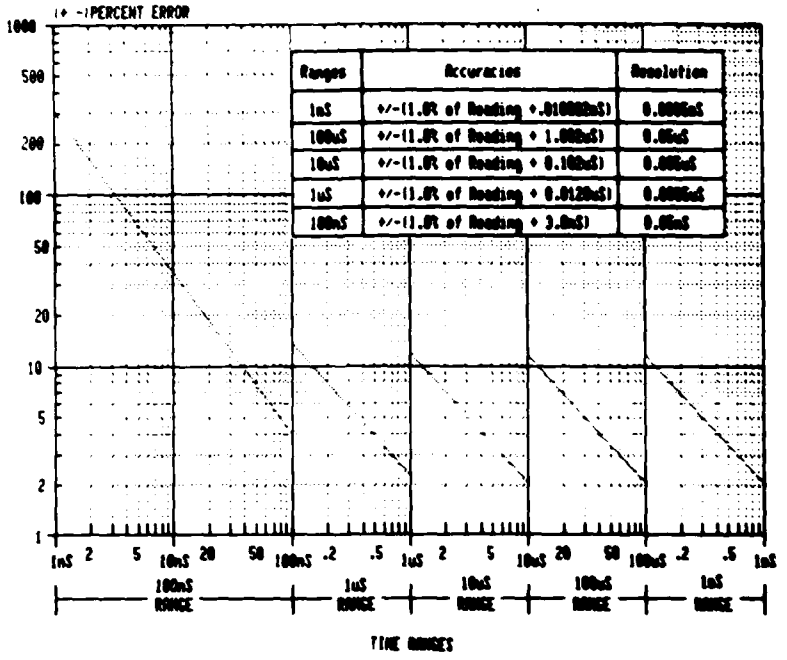

Figure 2-6. S3260/70 - Time Measurement Accuracies

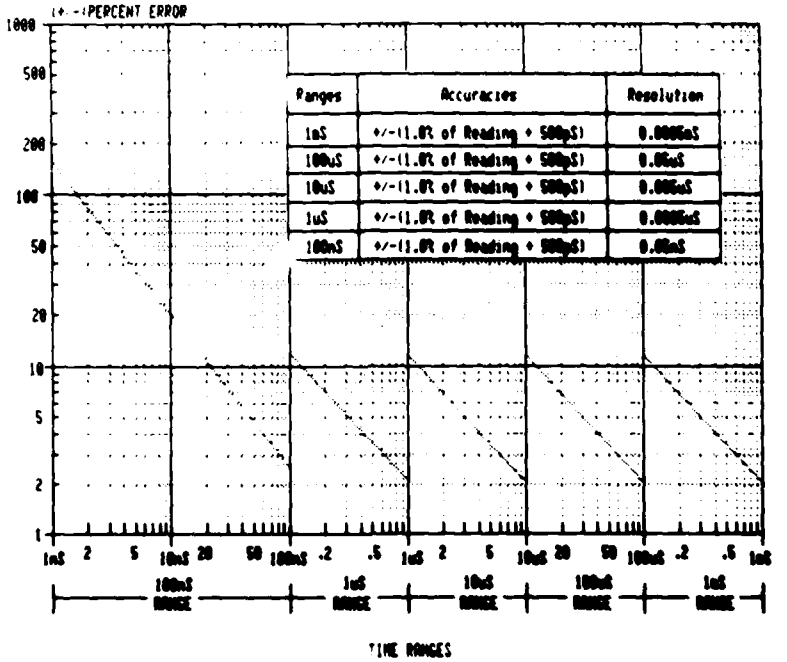

Figure 2-7. S3260/70 - Time Measurement Accuracies - HPO

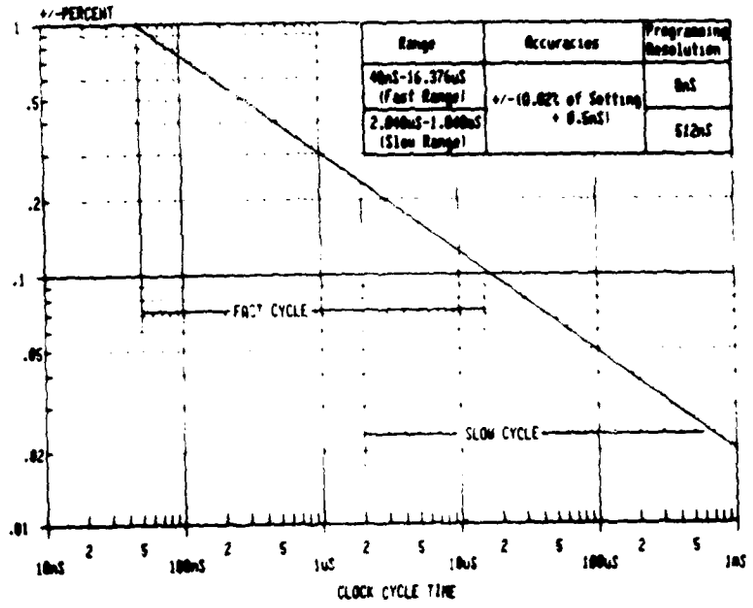

Figure 2-8. S3260/70 - Clock Cycle Accuracies

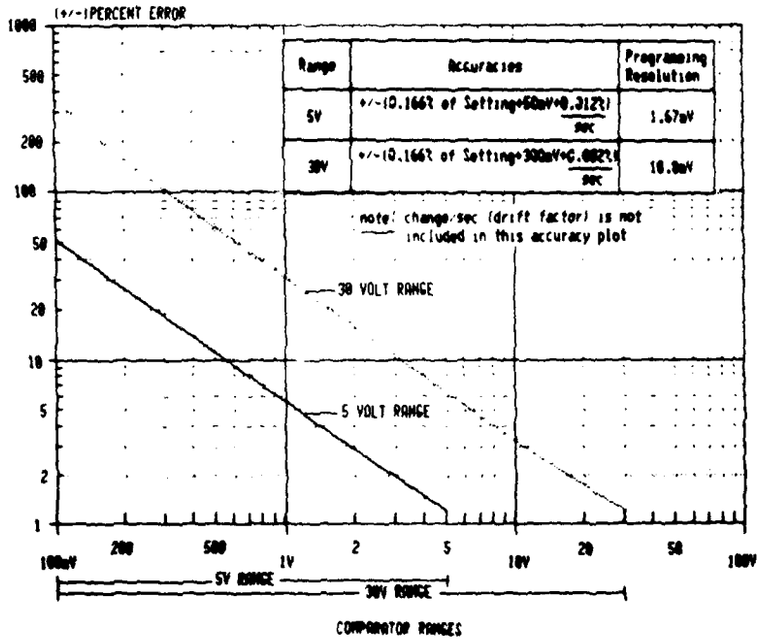

Figure 2-9. S3260/70 - D70 Pin Electronics Card Accuracies

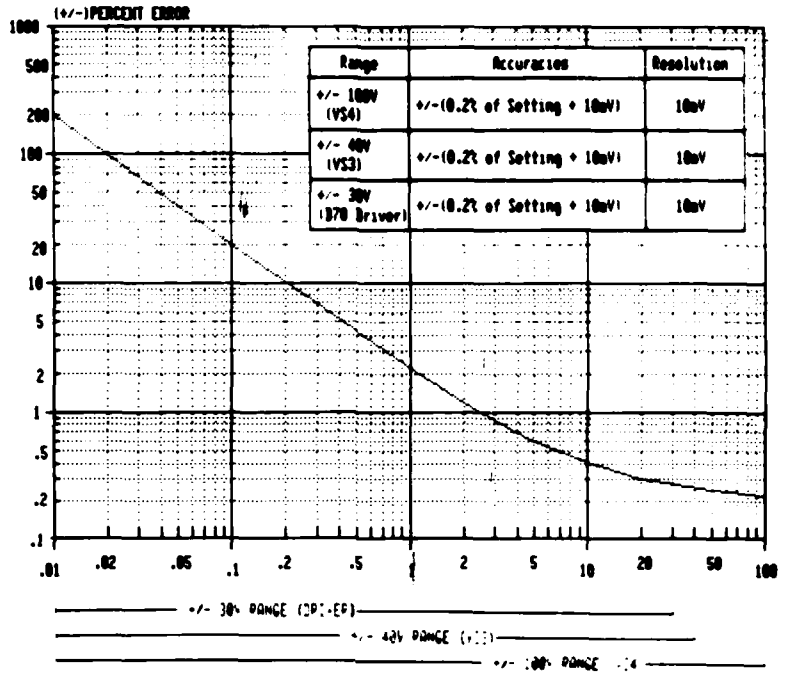

Figure 2-10. S3260/70 - Forcing Voltage Accuracies

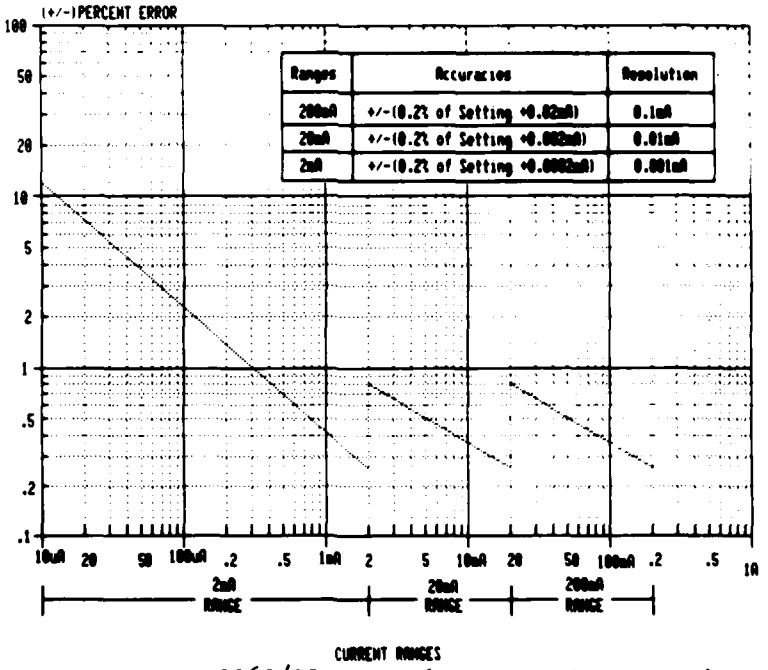

Figure 2-11. S3260/70 - Forcing Current Accuracies

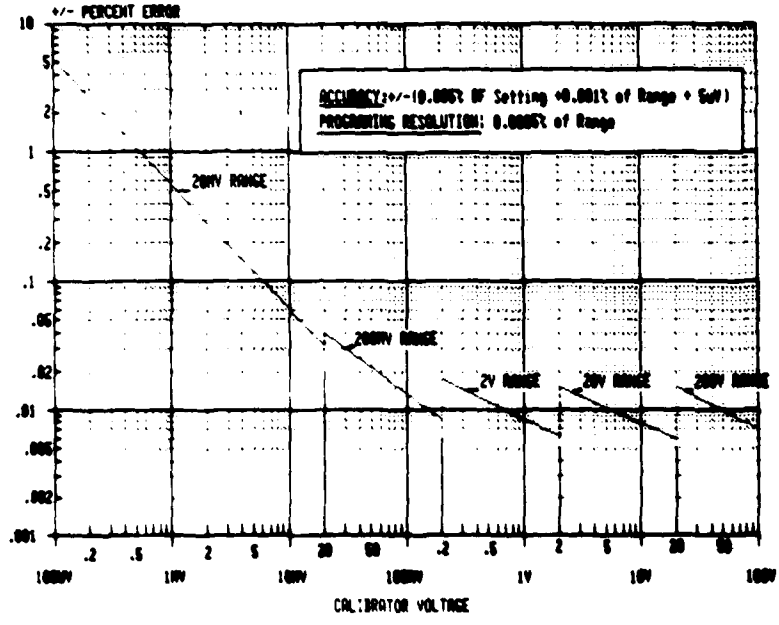

Figure 2-12. Fluke 8100B Meter Calibrator - Forcing Voltage Accuracies

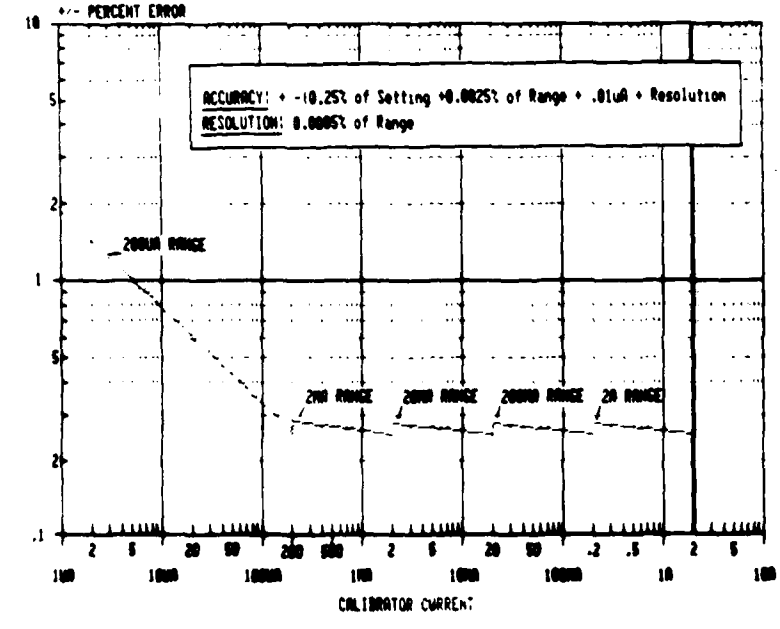

Figure 2-13. Fluke 8100B Meter Calibrator - Forcing Current Accuracies

MANUFACTURER CODE: A ; DEVICE TYPE: LF198; DATE CODE:7509 25 SEP 80 11:33:19

PARAMETER	LO-LIM	S/N 6	S/N 9	S/N19	S/N23	-55 DEG C S/N28	S/N34	S/N35	S/N41	S/N45	S/N48	HI-LIM	
VIO(+CM) AT 3.5V,-26.5V	-5.00	-2.00	131.M	23.3M	-268.M	-826.M	-934.M	-137.M	-957.M	1.31	213.M	5.00	MV
VIO(-CM) AT 26.5V,-3.5V	-5.00	-1.41	673.M	674.M	472.M	-116.M	-27.1M	685.M	2.94	1.64	1.02	5.00	MV
VIO(DCM) AT 15.0V,-15.0V	-5.00	-1.60	468.M	479.M	274.M	-405.M	-307.M	369.M	-592.M	1.48	-142. *	5.00	MV
VIO(-CM) AT 7.0V,-3.0V	-5.00	-1.71	363.M	384.M	82.3M	-384.M	-452.M	232.M	16.0 *	6.85 *	531.M	5.00	MV
VIO(+CM) AT 3.0V,-7.0V	-5.00	-2.31	-132.M	-229.M	-632.M	-933.M	-987.M	-376.M	-1.19	1.03	-228.M	5.00	MV
DELTA VIO/DELTA T (DCM)	-20.0	4.31	-2.02	1.13	1.21	-4.92	232.M	-7.24	11.9M	-3.10	1.77K*	20.0	UV/DEG C
IIB(+CM) AT 3.5V,-26.5V	-75.0	13.9	18.7	15.4	14.8	20.5	45.0	21.5	20.2	14.8	22.8	75.0	NA
IIB(-CM) AT 26.5V,-3.5V	-75.0	13.4	18.1	14.8	14.2	19.6	43.2	20.4	17.9	14.2	21.9	75.0	NA
IIB(DCM) AT 15.0V,-15.0V	-75.0	13.6	18.2	15.0	14.2	19.4	43.9	20.6	18.9	14.4	-1.40K*	75.0	NA
IIB(-CM) AT 7.0V,-3.0V	-75.0	13.7	18.2	15.2	14.3	20.5	44.1	21.4	14.3	12.9	20.9	75.0	NA
IIB(DCM) AT 3.0V,-7.0V	-75.0	14.0	18.7	15.6	14.4	21.4	45.7	22.3	21.9	15.4	21.7	75.0	NA
INPUT IMPEDANCE (ZI)	1.00	44.7	33.4	41.0	35.6	25.7	12.3	20.8	9.92	34.5	25.9	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	75.0M	305.M	50.0M	300.M	167.M	-49.2	175.M	200.M	-150.M	300.M	4.00	OHMS
RSC-SERIES CHG RESISTANCE	100.	287.	285.	275.	345.	275.	277.	268.	256.	1.00K*	324.	600.	OHMS
GAIN ERROR (+/-11.5V CM)	-20.0M	-2.83M	-2.83M	-3.07M	-3.35M	-3.65M	-4.04M	-4.02M	-18.6M	-1.91M	-3.78M	20.0M	%
GAIN ERROR (+/-2.0V CM)	-40.0M	-16.9M	-13.5M	-16.3M	-19.6M	-16.0M	-17.3M	-15.4M	-451.M*	-150.M*	-22.1M	40.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	12.4	14.3	15.2	14.4	13.6	15.5	14.3	14.6	15.1	15.0	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-7.09	-5.37 *	-5.19 *	-4.46 *	-5.32 *	-7.20	-3.81 *	-3.26 *	-3.64 *	-4.00 *	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	96.5	98.9	97.2	97.3	102.	95.6	95.1	100.	108.	96.9	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	106.	132.	114.	132.	98.7	112.	142.	122.	105.	200.	200.	dB
FEEDTHRU REJ 0V TO 11.5V	80.0	98.1	89.3	91.6	91.3	92.6	89.1	89.4	89.4	114.	90.4	200.	dB
FEEDTHRU REJ 11.5V TO 0V	80.0	90.6	92.7	98.0	95.7	95.7	95.0	93.3	107.	97.1	96.7	200.	dB
FEEDTHRU REJ 0V TO -11.5V	80.0	93.5	96.6	94.5	94.4	93.1	92.3	96.3	53.4 *	95.8	95.5	200.	dB
FEEDTHRU REJ -11.5V TO 0V	80.0	92.0	88.5	94.1	91.7	53.7 *	45.3 *	53.6 *	95.2	59.5 *	92.4	200.	dB
HOLD STEP VOLTAGE (VHS+)	-5.00	235.M	322.M	50.4M	215.M	160.M	175.M	45.4M	590.M	230.M	216.M	5.00	MV
HOLD STEP VOLTAGE (VHS-)	-5.00	-9.60M	-60.6M	-459.M	-173.M	-275.M	-34.6M	-300.M	-110.M	-154.M	-184.M	5.00	MV
ICC-SUPPLY CURRENT (@15V)	0.00	4.66	4.68	5.20	4.30	5.11	4.74	4.68	5.75	4.67	4.94	6.50	MA
IIH-LOGIC INPUT	0.00	1.77	2.19	2.28	3.31	2.09	4.55	2.66	3.18	2.09	2.47	20.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	950.M	1.04	1.08	1.32	1.35	2.11	1.18	1.48	885.M	1.18	20.0	UA
IIL-LOGIC INPUT	-3.00K	-1.70	-1.65	-700.M	-900.M	-650.M	-1.05	-1.70	-800.M	-650.M	-1.65	3.00K	NA
IIL-LOGIC REFERENCE INPUT	-3.00K	-450.M	-350.M	-800.M	-350.M	-1.00	-450.M	-200.M	-1.15	-1.15	-200.M	3.00K	NA
OUTPUT SHORT CIRCUIT (+)	-20.0	-13.8	-13.8	-15.9	-12.4	-13.8	-14.5	-13.9	-16.1	-14.6	-13.7	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	15.8	17.5	18.8	14.2	13.1	18.2	15.6	16.5	16.1	11.9	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	0.00	2.00	-1.50	3.50	5.00	-1.50	-2.50	-1.50	11.5	8.85	-1.25	0.00	PA
HOLD CAPACITOR LEAKAGE(-)	0.00	0.00	-1.10	2.50	1.00	-7.00	-3.00	-4.70	5.50	-5.75	-600.M	0.00	PA
HOLD CAP CHRG CURRENT(+)	-100.	-6.83	-6.83	-6.97	-5.60	-7.14	-7.03	-7.32	-8.07	-8.10	-6.01	-2.00	MA
HOLD CAP CHRG CURRENT(-)	2.00	5.12	5.63	6.34	4.42	5.09	5.23	5.49	6.45	5.07	5.11	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	1.49	1.43	1.48	1.48	1.17	1.44	1.54	1.54	1.47	1.48	2.00	V
TAO (VIN-0V TO 10V STEP)	0.00	24.8	23.1	22.6	28.2	23.7	22.6	21.7	17.9	23.5	25.7	50.0	USEC
TAO (VIN-0V TO -10V STEP)	0.00	22.7	24.0	24.6	28.2	21.6	21.5	20.8	20.3	22.0	28.3	50.0	USEC
TAO (VIN--10V TO 0V STEP)	0.00	22.7	22.7	22.4	27.5	22.6	23.5	20.9	29.7	38.3	25.9	50.0	USEC
TAO (VIN-10V TO 0V STEP)	0.00	22.5	22.3	21.2	28.1	21.5	21.9	20.4	20.0	21.6	25.7	50.0	USEC
TAP (VIN-0V TO 10V STEP)	0.00	60.0	45.0	45.0	45.0	60.0	35.0	60.0	70.0	55.0	50.0	400.	NSEC
TAP (VIN-0V TO -10V STEP)	0.00	25.0	15.0	25.0	25.0	30.0	495. *	35.0	45.0	310.	25.0	400.	NSEC
TAP (VIN--10V TO 0V STEP)	0.00	60.0	40.0	45.0	45.0	55.0	35.0	60.0	65.0	495. *	45.0	400.	NSEC
TAP (VIN-10V TO 0V STEP)	0.00	30.0	15.0	25.0	30.0	35.0	15.0	40.0	40.0	30.0	30.0	400.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Figure 2-14. Table of Characterization Data for Ten Sample/Hold Devices

AD584T PIN PROGRAMMABLE PRECISION VOLTAGE REFERENCE

S/N=2822 ;DATE=03 OCT 80

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	-55C	0C	25C	70C	125C	HI-LIMIT	UNITS
VOUT1	VIN=15V IO=0MA	VO=10V STB=1	1	9.95000	9.99308	10.0001	10.0037	10.0032	10.0098	10.0100	V
VOUT2	VIN=15V IO=0MA	VO=7.5V STB=1	1	7.49200	7.49517	7.50087	7.50364	7.50350	7.50872*	7.50800	V
VOUT3	VIN=15V IO=0MA	VO=5V STB=1	1	4.99400	4.99491	4.99910	5.00098	5.00099	5.00468	5.00600	V
VOUT4	VIN=15V IO=0MA	VO=2.5V STB=1	1	2.49650	2.49639*	2.49932	2.50040	2.50067	2.50290	2.50350	V
ICC1	VIN=15V IO=0MA	VO=10V STB=1	8	0.000	638.0U	719.5U	755.5U	819.5U	911.5U	1.000M	A
ICC2	VIN=15V IO=0MA	VO=10V STB=0	8	0.000	79.95U	50.40U	42.40U	30.50U	22.80U	1.000M	A
ICC3	VIN=40V IO=0MA	VO=10V STB=1	8	0.000	633.5U	718.0U	756.5U	824.0U	908.5U	1.000M	A
ICC4	VIN=40V IO=0MA	VO=10V STB=0	8	0.000	81.95U	51.15U	43.20U	32.35U	24.50U	1.000M	A
IOS1	VIN=15V IO=0MA	VO=0V STB=1	1	-30.00M	-14.00M	-13.50M	-12.80M	-11.20M	-9.550M	0.000	A
IOS2	VIN=15V IO=0MA	VO=15V STB=1	1	0.000	27.80M	25.85M	25.00M	23.25M	20.90M	30.00M	A
VRL1	VIN=15V IO=0MA	VO=10V STB=1	1	9.99000	9.99325	10.0001	10.0036	10.0032	10.0100	10.0100	V
VRL2	VIN=15V IO=-5MA	VO=10V STB=1	1	9.99000	9.99273	9.99909	10.0025	10.0019	10.0087	10.0100	V
VRL3	VIN=15V IO=0MA	VO=7.5V STB=1	1	7.49200	7.49558	7.50088	7.50363	7.50351	7.50897*	7.50800	V
VRL4	VIN=15V IO=-5MA	VO=7.5V STB=1	1	7.49200	7.49393	7.49985	7.50247	7.50217	7.50768	7.50800	V
VRL5	VIN=15V IO=0MA	VO=5V STB=1	1	4.99400	4.99503	4.99910	5.00096	5.00102	5.00491	5.00600	V

Figure 2-15. Table of Characterization Data for One Voltage Reference

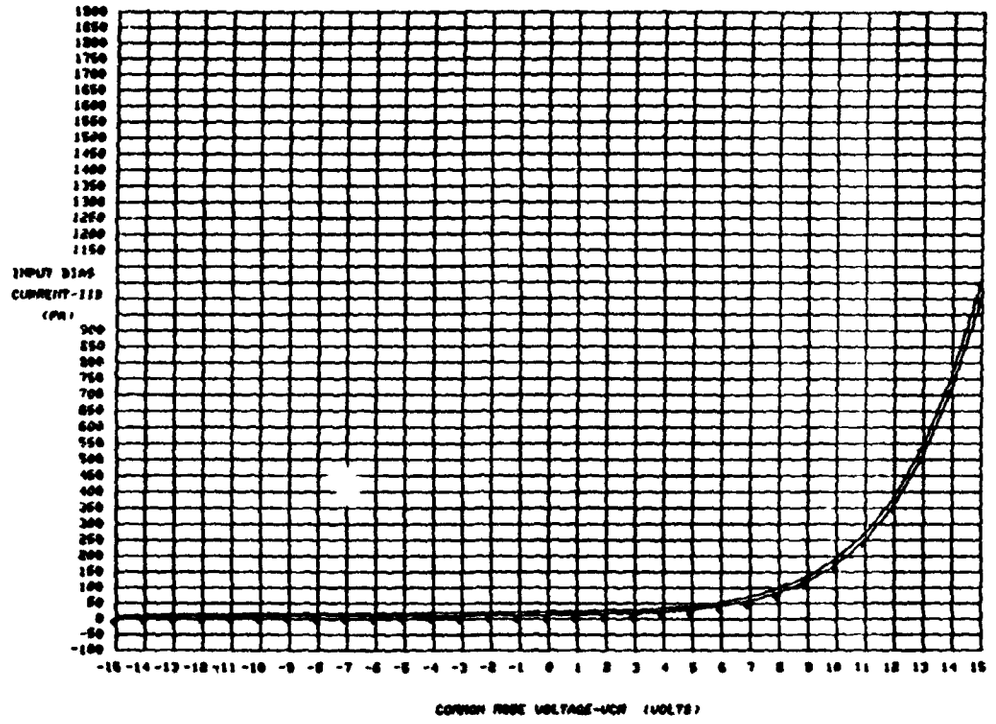

Figure 2-16. S3260/70 - Graphic Plotting Capability

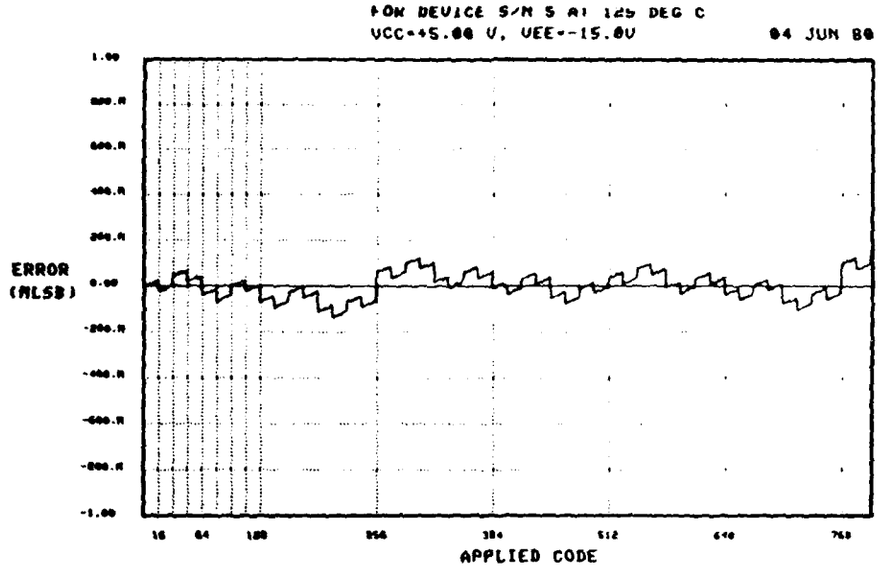

Figure 2-17. LINEARITY ERROR (ALL CODES)

562-12 BIT D/A CONVERTER

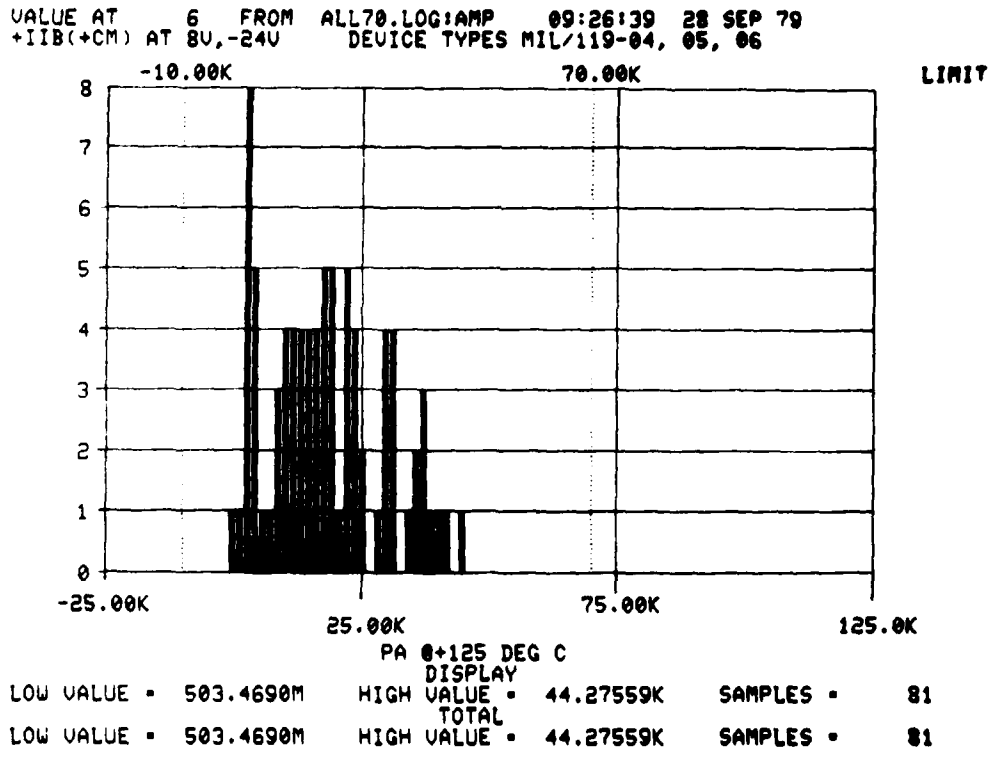

Figure 2-18. Histogram Representation of Characterization Data

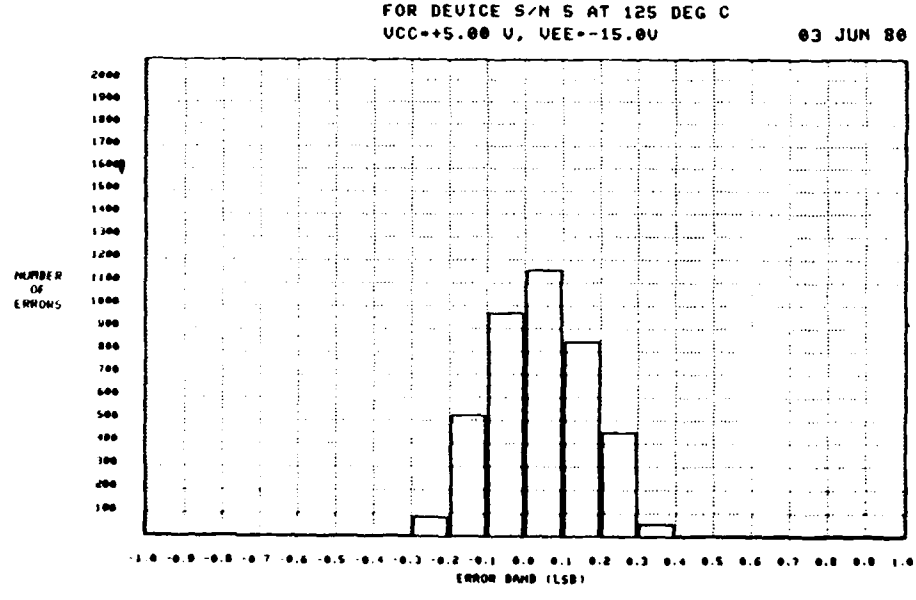

Figure 2-19. LINEARITY ERROR DISTRIBUTION

562-12 BIT D/A CONVERTER

SECTION III
BI-FET OPERATIONAL AMPLIFIERS, MIL-M-38510/114

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SECTION III
BI-FET OPERATIONAL AMPLIFIERS
MIL-M-38510/114A

3.1 Introduction

This report updates and completes the characterization work which was covered in an earlier RADC technical report. Table 3-1 gives some specifics on the devices tested and their relationship to the military slash sheet device types.

Table 3-1. Table of Device Types Specified.

Device Type	Generic Type	Manufacturer Symbol	BI-FET Op Amp Description
-	LF355	T	Low power (consumer grade)
11401	LF155	F, S	Low power
11402	LF156	A, F, S	Wideband
11403	LF157	A, S, N	Wideband, undercompensated
11404	LF155A	N, P	Low power, low offset
11405	LF156A	N, P, I	Wideband, low offset
11406	LF157A	P	Wideband, undercomp., low offset

A = Advanced Micro Devices
F = Fairchild
N = National Semiconductor
S = Signetics
I = Intersil
P = Precision Monolithics
T = Texas Instruments

The manufacturer symbol column reflects the source of the devices, which were characterized. Most manufacturers produce most of the generic types even though they are not listed for each category in the table. Since the characterization effort at GEOS has been completed several manufacturers have discontinued production of part or all of the LF155 series of BI-FET op amp devices. As of this writing (August 1980) only National, AMD and PMI remain as sources of these devices. It is suspected that manufacturing difficulties and market competition from these newer low cost family of multiple BI-FET op amps, reported in Section IV, has caused this to happen.

As the name implies, "BI-FET" stands for a mixed technology process in which bipolar and field effect transistors are combined on the same monolithic integrated circuit. Standard bipolar processing is used for most of the circuit elements except for the top gate and channel of the

J-FETs, which depend on the ion implantation process. Matched input J-FETs having low offset voltage and offset voltage drift is the big contribution of the ion implantation process.

With J-FET input transistors, the input bias currents are typically under 100 pA. Also, bandwidth and slew rate are not severely compromised by low input bias current as in the case with bipolar transistor front ends having low input bias currents. Obviously the BI-FET process enables the best features of bipolar and J-FET transistors to be incorporated into the design of the IC op amp.

A review of linear device applications in military systems as well as a JC-41 Committee priority list were factors in characterizing and developing a slash sheet for this multi-sourced family of devices.

3.2 Description of Device Types

A typical schematic circuit of a BI-FET op amp is shown in Figure 3-1. Matched J-FET transistors are used for the differential input gain stage, the input current source loads and the offset adjustment control. The drain outputs of the input P-channel J-FETs feed a differential bipolar transistor stage. Signal conversion from differential to single-ended is made at the collector of Q8. Since current sources exist at both the source and drain terminals of the input J-FETs, some mechanism must also exist to deal with the excess common mode current which is sourced from Q1, but not sunk by J10 and J11. Common mode feedback from the differential bipolar stage current source to the source terminals of J1 and J2 solves this problem.

With J-FET input transistors the op amp bias currents + IiB, and - IiB are much smaller than is possible with bipolar transistors. Since these currents are leakage currents, they are temperature sensitive and approximately double for every 10°C increase in temperature. Low noise and good high frequency response are other benefits of the J-FET front end transistors. The single-ended output signal from Q8 and its J3 current source load is further amplified by the class B output stage. This output stage is a little unusual in that a J-FET, J5, complements the other bipolar output transistors. Replacing the standard PNP output transistor with a J-FET increases the phase margin of the device and thus enhances the stability of the device for driving high capacitance loads.

Capacitor C2 is the compensation capacitor which establishes the dominant pole from which the open loop voltage gain is "rolled-off". This capacitor therefore affects the unity gain bandwidth and slew rate of the op amp. Another parameter which affects slew rate is the operating current which is available to drive the compensation capacitor. Both the operating current and the compensation capacitor are variables which the IC manufacturers can control in order to achieve a

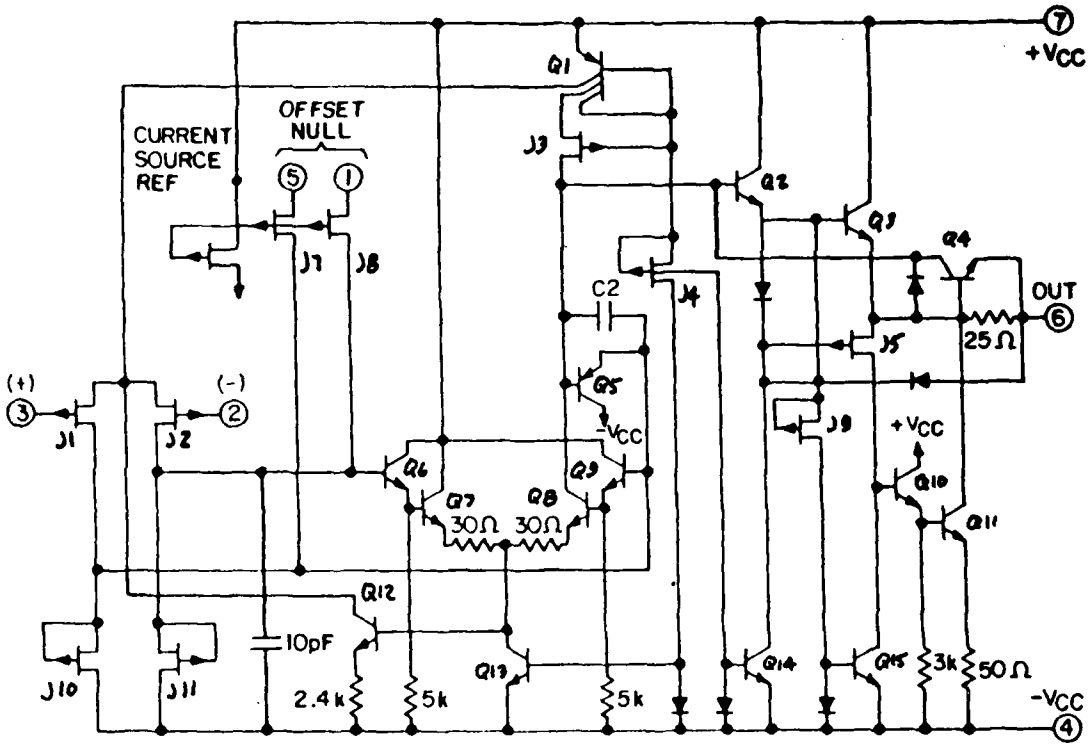


Figure 3-1. Typical BI-BET Op Amp Schematic (LF155/156/157)

desired speed/power tradeoff. Device types 01, 02, and 03 are basically the same device with different values of compensating capacitance and/or operating current.

Device types 04, 05, and 06 have a similar trend, but have lower input offset voltage and drift. Table 3-2 shows the significant differences in electrical parameters for the various device types over the 25°C to 125°C temperature range.

Table 3-2. Basic Device Type Parameter Differences.

Electrical Parameter	Device Type 01	02	03	04	05	06	Units
Input Offset Voltage	+/-7	+/-7	+/-7	+/-2.5	+/-2.5	+/-2.5	m/V
Offset Voltage Drift	+/-30	+/-30	+/-30	+/-10	+/-10	+/-10	uV/°C
Supply Current (max)	4	7	7	4	7	7	m/A
Slew Rate (min)	1	5	20	1.5	7	25	V/us
Gain Bandwidth (Typ)	2.5	5	20	2.5	5	20	MHz

All of the devices are packaged in an eight lead metal can (MIL-M-38510 case outline A-1).

3.3 Test Development

Op amp parameters and test circuits for their measurement are well known in the industry. As far as BI-FET op amps are concerned, the essential improvement in these devices is their low input bias currents. Measurements of these low bias currents was one of the more challenging aspects of BI-FET op amp test development.

Table 3-3 gives a listing of the standard op amp parameters which had to be measured in order to characterize these devices.

Table 3-3. Test Parameters for Characterization

Item	Symbol	Parameter (See Page for definitions)
1	V10	Input Offset Voltage
2	D-V10/D-T	Input Offset Voltage Temperature Sensitivity
3	I10	Input Offset Current
4	$+I_{1B}$-I_{1B}	Input Bias Current
5	+PSRR, -PSRR	Power Supply Rejection Ratio
6	CMR	Input Voltage Common Mode Rejection
7	V10 ADJ (+), V10 ADJ (-)	Adjustment for Input Offset Voltage
8	Ios (+)	Output Short Circuit Current (for positive output)
9	Ios (-)	Output Short Circuit Current (for negative output)
10	Icc	Power Supply Current
11	+Vop, - Vop	Output Voltage Swing
12	Avs (+), Avs (-)	Open Loop Voltage Gain
13	TR (tr)	Transient Response (Rise time)
14	TR (os)	Transient Response (Overshoot)
15	NI (BB)	Noise (referred to input) Broadband
16	NI (PC)	Noise (referred to input) Popcorn

These parameters are specified and measured over the -55°C to 125°C military temperature range for various input common mode voltage and output loading conditions. Initial test conditions and parameter limits were recommended by the JC-41 Committee on Linear Microcircuits.

Detailed test conditions and equations are shown in the Appendix, Table 3-4.

Test Philosophy

The approach to testing was to look at typical parameters on a Tektronix 577 curve tracer in parallel with developing the Tektronix S-3260 test system adapter and program software. The objective of this dual approach was to identify anomalies and trends early so that this information could be factored into the automatic test development.

Static Test Circuit Description

A schematic diagram of the static test circuit is shown in Figure 3-2. All relays are in the normal de-energized position. Operation of the test circuit is straight forward. The device under test (D.U.T.) and the nulling amplifier are cascaded within a closed loop gain of 1000. This is done so that millivolts of error voltage with respect to the op amp input are translated into volts D.C. at the nulling amplifier output to the automatic measurement system. The D.U.T. output can be commanded to any voltage in its operating range by applying the negative of the desired voltage to terminal 4. When the non-inverting input to the nulling amplifier is at zero volts, the loop has stabilized and the

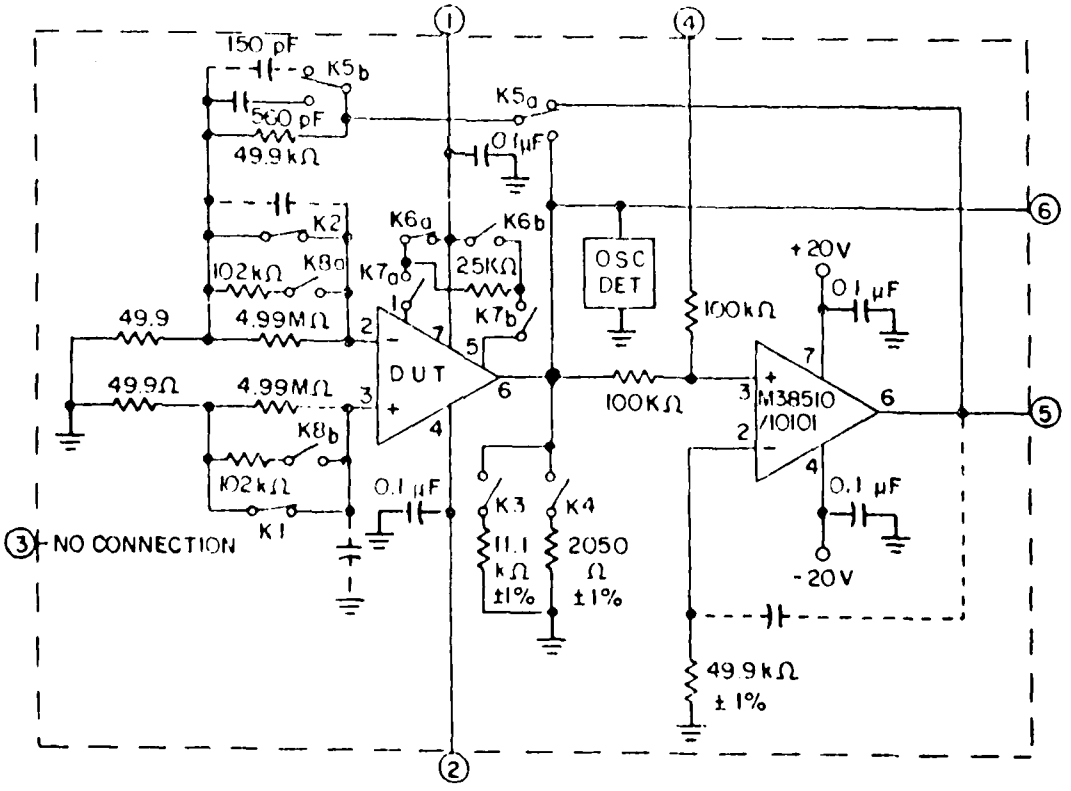


Figure 3-2. Test Circuit for Static Tests

correct output can be measured. Tests which require the D.U.T. to be exercised over the common mode range are mechanized by swinging the power supplies and commanding the D.U.T. inputs through 50 ohms. The basic measurement performed by the static test circuit is VIO or offset voltage. Most of the other parameters are derived from this basic measurement. Two photographic views of the test adapter are shown in Figure 3-4.

Parameter Tests for Special Consideration

Because BI-FET bias current can increase by a factor of 1000 in going from 25°C to 125°C, it is necessary to change the input sensing resistors from 5 Mohm to 100 Kohm. Relay K8 is programmed for the high temperature measurement in order to cause the resistor value to change. With the high value bias current resistors there was a tendency for test circuit instability. Good layout considerations and a bypass capacitor from the non-inverting input to ground kept the test circuit stable.

Although slew rate is not a static test, it was tested automatically with the parameters listed in Table 3-3. The test circuit for slew rate and transient response is shown in Figure 3-3.

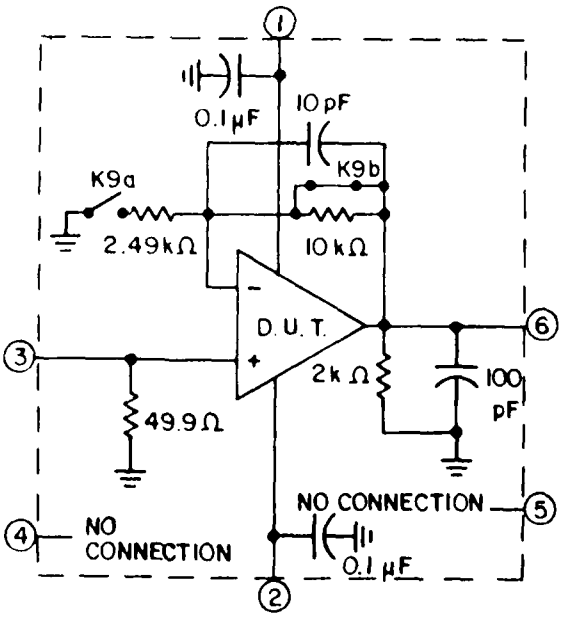


Figure 3-3. Test Circuit for Transient Response and Slew Rate.

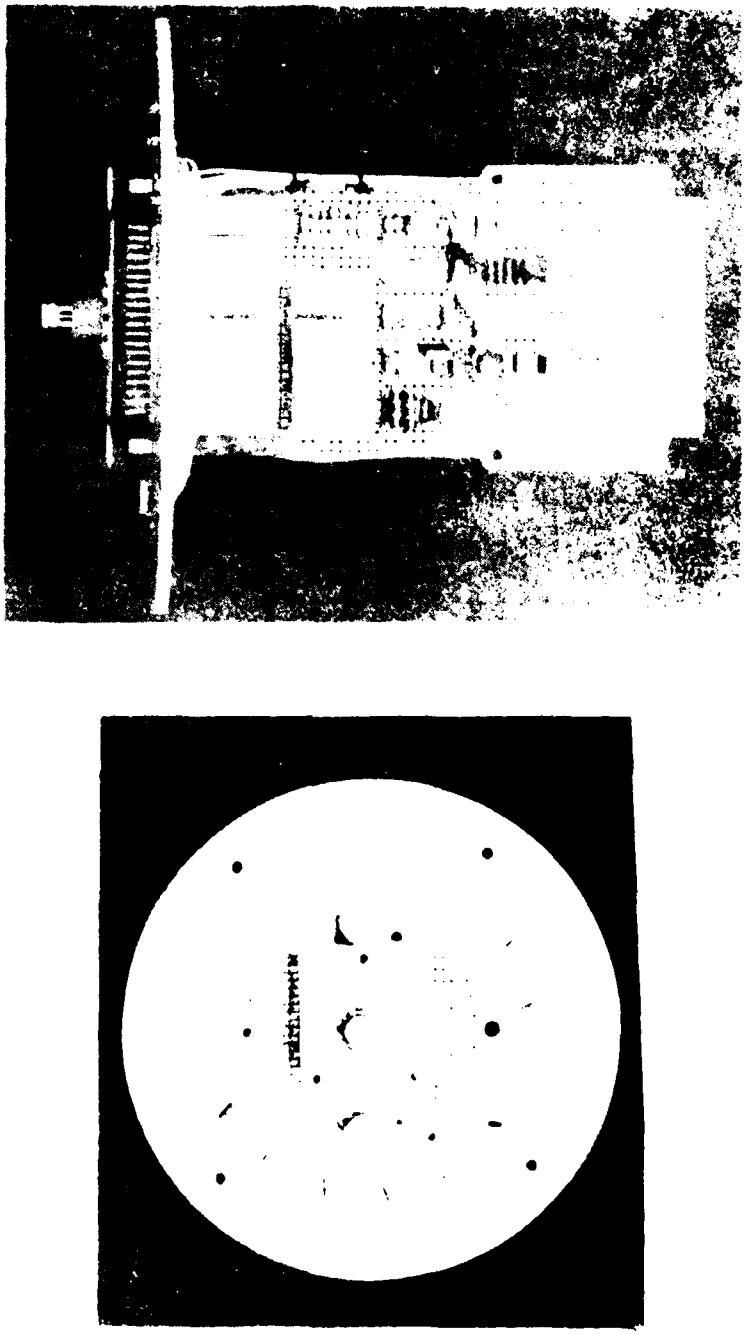
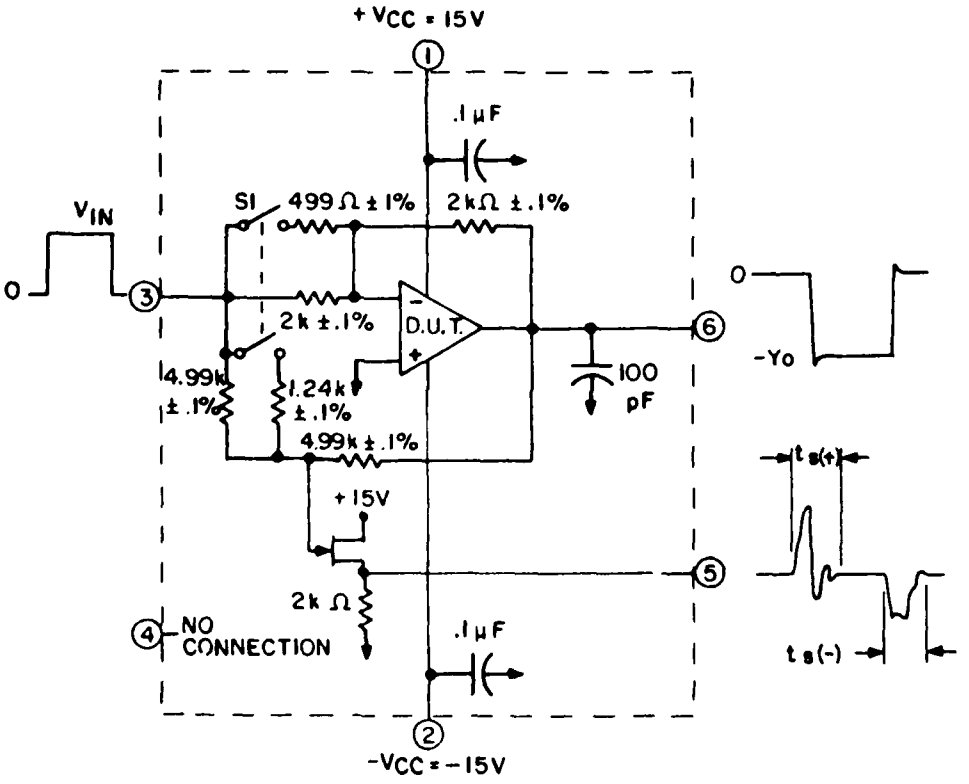


Figure 3-4. Bi-FET Op Amp Test Adapter.

It is an easy matter to incorporate this circuit into the static test circuit, however, care must be taken in routing the connections to the op amp inputs. Table 3-5 in Appendix shows the test conditions and equations for slew rate and transient response.

Because of limitations with the S-3260 measurement system it was not possible to measure noise and transient response automatically with the other op amp parameters. Bench tests had to be used for these measurements.

Another parameter which had to be tested manually using the circuit in Figure 3-5 is settling time.



NOTES:
1. Resistors are ±1.0% and capacitors are ±10% unless otherwise specified.
2. Precaution shall be taken to prevent damage to the D.U.T. during insertion into socket and in applying power.
3. For device types 01 and 02, S1 is open, AV = -1 and V_{IN} = 10 V.
4. For device type 03, S1 is closed, AV = -5 and V_{IN} = 2 V.
5. Settling time t_s, measured on pin 5, is the interval during which the summing node is not nulled.

Figure 3-5. Test Circuit for Settling Time.

3.4 Test Results and Data

A total of 204 BI-FET op amps were tested. These devices were tested in two groups with the distinction being A's or non-A's.

The LF355 devices were tested with the precision A parts, but the data was not statistically grouped with those devices.

A typical data sheet of an LF155 op amp in the first group of testing is shown in Table 3-6. All of the data is within the initial JC-41 Committee recommended limits, unless an asterisk (*) is displayed adjacent to the measured value. For this group, the data at all three temperatures (-55°C, 25°C and 125°C) is shown on a single table.

On the second group of devices (LF155A series), it was decided to change the format so that the data of up to ten devices could be displayed on a single sheet. Table 3-7 in Appendix shows this scheme for different devices at a single temperature. With this method it is easier to make device-to-device comparisons and to check for common peculiarities, etc.

A third form of data common to both groups of devices are histograms. Figure 3-7 shows a histogram of offset voltage VIO at zero common mode voltage and 25°C for all of the devices in group 2. The raw data is too extensive for inclusion in this report, since each test group contains 114 histograms and over 30 individual data sheets. Besides showing the data elements vs frequency of occurrence, the histograms also display the initial JC-41 parameter limits. Direct comparisons of the data to the proposed limits are useful in determining the relative test yields of the devices. The raw data was presented to industry representatives in two reports as follows:

1. Characterization Data for MIL-M-38510/114 BI-FET Op Amps (Commercial Types LF155, LF156, and LF157)(21 November 1978).

2. Characterization Data for MIL-M-38510/114 BI-FET Op Amps (Commercial Types LF155A, LF156A, and LF157A) (16 April 1979).

Within the static test parameters, the measurement and characterization of input bias current was the most difficult. Figure 3-7, shows how input bias current varies typically with common mode voltage and supply voltage. It should be noted that bias current increases significantly under positive common mode conditions.

MANUFACTURER CODE: A ; DEVICE TYPE: 155 ; S/N: 4 ; DATE CODE: 0 ; 28 NOV 78 22:38:31

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	125 DEG C LO-LIM	125 DEG C DATA	125 DEG C HI-LIM	UNITS
VIO(-CM) AT 35V,-5V	-6.00	-3.28	6.00	-4.00	-1.33	4.00	-6.00	-13.3M	6.00	MV
VIO(+CM) AT 5V,-35V	-6.00	-2.62	6.00	-4.00	-840.M	4.00	-6.00	401.M	6.00	MV
VIO(0CM) AT 20V,-20V	-6.00	-2.90	6.00	-4.00	-1.10	4.00	-6.00	153.M	6.00	MV
VIO(0CM) AT 5V,-5V	-6.00	-3.23	6.00	-4.00	-1.35	4.00	-6.00	-44.9M	6.00	MV
D-VIO/D-T FROM 25 OC	-30.0	22.5	30.0				-30.0	12.5	30.0	UV/OC
IIO(-CM) AT 35V,-5V	0.00	0.00	0.00	-20.0	4.46	20.0	-20.0K	285.	20.0K	PA
IIO(+CM) AT 5V,-35V	0.00	0.00	0.00	-400.	-148.	400.	-30.0K	-3.24K	30.0K	PA
IIO(0CM) AT 20V,-20V	0.00	0.00	0.00	-20.0	-16.5	20.0	-20.0K	-1.34K	20.0K	PA
IIO(+CM) AT 5V,-25V	0.00	0.00	0.00	-20.0	-34.5 x	20.0	-20.0K	-1.66K	20.0K	PA
+IIB(-CM) AT 35V,-5V	0.00	0.00	0.00	-100.	11.2	100.	-10.0K	7.79K	50.0K	PA
+IIB(+CM) AT 5V,-35V	0.00	0.00	0.00	-100.	1.07K	2.00K	-10.0K	18.1K	60.0K	PA
+IIB(0CM) AT 20V,-20V	0.00	0.00	0.00	-100.	49.9	100.	-10.0K	11.8K	50.0K	PA
+IIB(+CM) AT 5V,-25V	0.00	0.00	0.00	-100.	68.8	300.	-10.0K	12.1K	50.0K	PA
-IIB(-CM) AT 35V,-5V	0.00	0.00	0.00	-100.	6.71	100.	-10.0K	7.51K	50.0K	PA
-IIB(+CM) AT 5V,-35V	0.00	0.00	0.00	-100.	1.21K	2.00K	-10.0K	21.4K	60.0K	PA
-IIB(0CM) AT 20V,-20V	0.00	0.00	0.00	-100.	66.4	100.	-10.0K	13.1K	50.0K	PA
-IIB(+CM) AT 5V,-25V	0.00	0.00	0.00	-100.	103.	300.	-10.0K	13.8K	50.0K	PA
+PSRR AT 10V,-20V	85.0	120.	0.00	85.0	110.	0.00	85.0	115.	0.00	dB
-PSRR AT 20V,-10V	85.0	112.	0.00	85.0	108.	0.00	85.0	114.	0.00	dB
CMR AT 20V,-20V	85.0	93.4	0.00	85.0	95.7	0.00	85.0	97.2	0.00	dB
V-ADJ(+) AT 20V,-20V	8.00	13.0	20.0	8.00	13.0	20.0	8.00	13.1	20.0	MV
V-ADJ(-) AT 20V,-20V	-20.0	-14.3	-8.00	-20.0	-14.3	-8.00	-20.0	-14.2	-8.00	MV
IOS(+) AT 15V,-15V	-60.0	-32.3	0.00	-60.0	-24.6	0.00	-60.0	-15.0	0.00	NA
IOS(-) AT 15V,-15V	0.00	32.9	60.0	0.00	25.2	60.0	0.00	16.7	60.0	NA
ICC AT 15V,-15V	0.00	4.49	6.00	0.00	3.60	4.00	0.00	2.95	4.00	MA
ICC AT 20V,-20V	0.00	5.56	7.00	0.00	4.11	5.00	0.00	3.31	5.00	MA
+VOP AT RL=10K	16.0	18.2	20.0	16.0	18.5	20.0	16.0	18.8	20.0	V
-VOP AT RL=10K	-20.0	-18.3	-16.0	-20.0	-18.6	-16.0	-20.0	-18.9	-16.0	V
+VOP AT RL=2K	15.0	18.0	20.0	15.0	18.2	20.0	15.0	18.6	20.0	V
-VOP AT RL=2K	-20.0	-17.6	-15.0	-20.0	-17.8	-15.0	-20.0	-17.5	-15.0	V
AVS(+) AT RL=10K	25.0	1.50K	0.00	50.0	1.00K	0.00	25.0	965.	0.00	V/MV
AVS(-) AT RL=10K	25.0	3.00K	0.00	50.0	100.K	0.00	25.0	3.33K	0.00	V/MV
AVS(+) AT RL=2K	25.0	1.50K	0.00	50.0	1.50K	0.00	25.0	690.	0.00	V/MV
AVS(-) AT RL=2K	25.0	1.50K	0.00	50.0	600.	0.00	25.0	212.	0.00	V/MV
AVS AT 5V,-5V,RL=10K	10.0	400.	0.00	10.0	100.K	0.00	10.0	173.	0.00	V/MV
AVS AT 5V,-5V,RL=2K	10.0	400.	0.00	10.0	800.	0.00	10.0	800.	0.00	V/MV
SR(+) AT 20V,-20V	2.00	11.8	0.00	2.00	9.35	0.00	2.00	7.81	0.00	V/US
SR(-) AT 20V,-20V	2.00	20.4	0.00	2.00	25.0	0.00	2.00	20.0	0.00	V/US

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 3-6. Typical LF155 Op Amp Data Sheet.

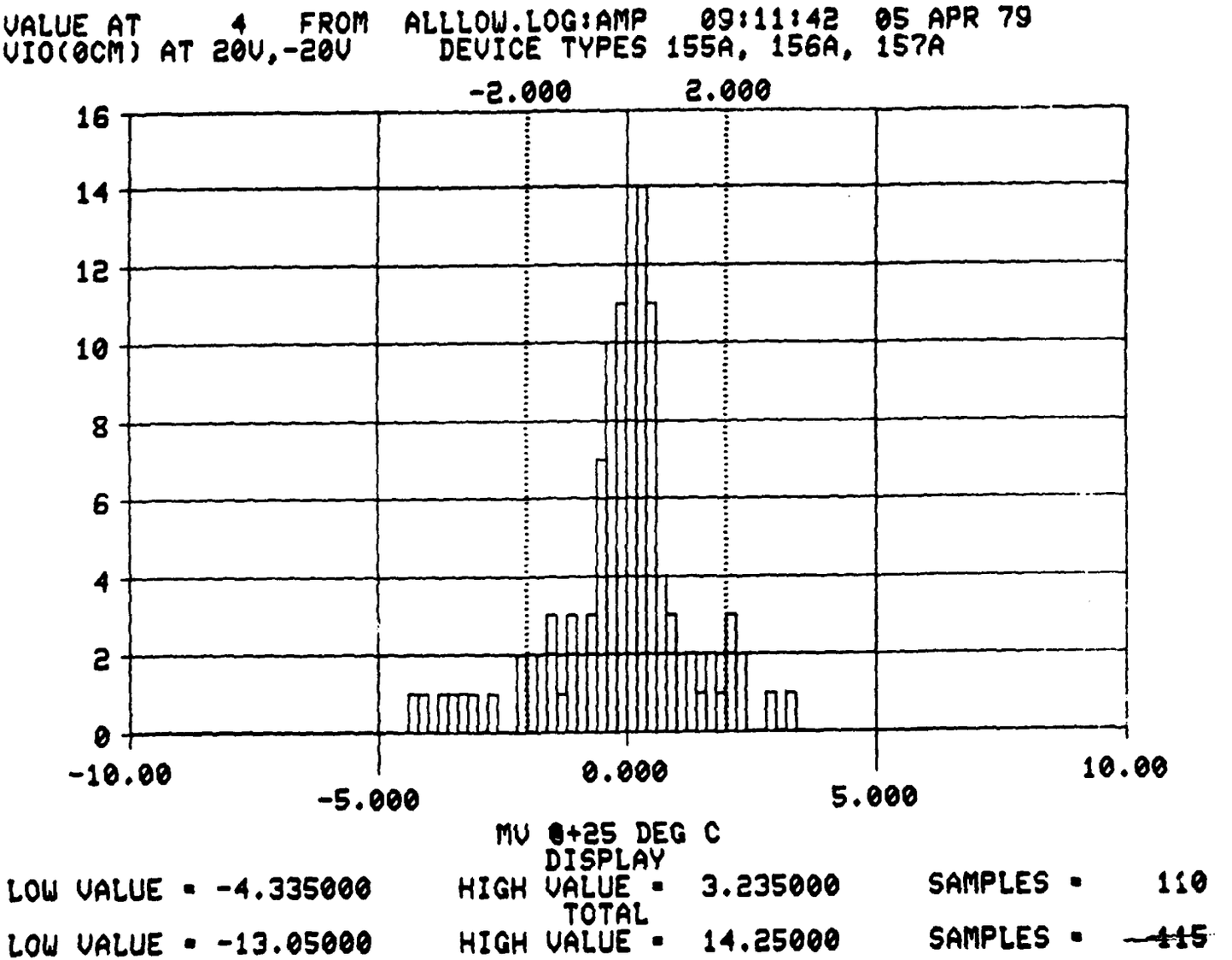
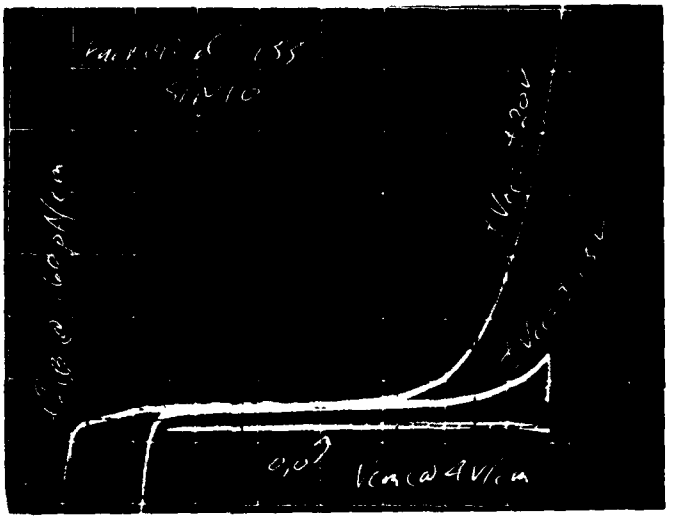


Figure 3-6. LF155A Series VIO Histogram.



+ I_{IB} @ 160 pA/CM

V_{CM} @ 4V/CM

Figure 3-7. BI-FET Input Bias Current vs. Common Mode Voltage.

The Appendix contains the following figures pertaining to test results and data.

Fig.	Title
3-8	BI-FET Input Bias Current vs Common Mode Voltage
3-9	BI-FET Input Bias Current vs Common Mode Voltage
3-10	BI-FET Input Bias Current vs Common Mode Voltage
3-11	BI-FET Input Bias Current vs Temperature
3-12	Worst Case Input Bias Current vs Ambient Temperature
3-13	Offset Voltage vs Common Mode Voltage
3-14	Offset Voltage vs Common Mode Voltage
3-15	LF155 and LF156 Transient Response
3-16	LF157 Transient Response
3-17	LF155 and LF156 Slew Rate
3-18	LF157 Slew Rate vs Closed Loop Gain
3-19	LF155 and LF156 Settling Time
3-20	Open Loop Voltage Gain vs Load
3-21	BI-FET Noise Voltage

These figures show the trends of individual devices as curve tracer displays, oscillographs and S-3260 curve plots. Statistical summaries of all device parameter data is contained within the following tables in the Appendix.

Table	Title
3-8	25°C Statistical Summary for LF155 Series Devices
3-9	-55°C Statistical Summary for LF155 Series Devices
3-10	125°C Statistical Summary for LF155 Series Devices
3-11	25°C Statistical Summary for LF155A Series Devices
3-12	-55°C Statistical Summary for LF155A Series Devices
3-13	125°C Statistical Summary for LF155A Series Devices
3-14	LF155 Dynamic Data at 25°C
3-15	LF156 Dynamic Data at 25°C
3-16	LF157 Dynamic Data at 25°C

Tables 3-17 and 3-18 shows the distribution of most parametric data in a cryptic histogram form. This comparison of data and limits is convenient for determining if limit changes should be considered.

3.5 Discussion of Results

On a parameter by parameter basis, a discussion of the device characteristics follows:

Input Offset Voltage (VIO)

(LF155/156/157 Family)

This family of devices had very good yields in passing the VIO tests over the common mode voltage and military temperature range. The screening limits for these devices were +/- 4 mV and +/- 6 mV at 25°C and over the military temperature range respectively. These limits were subsequently expanded to +/- 5 mV and +/- 7 mV respectively, as part of a decision to include the LF155A series op amps as separate device types with low offset voltage in the slash sheet. A 168 hour burn-in test at GE Ordnance Systems on the LF155 series group from vendor codes A, B, C and D revealed a maximum offset voltage shift of less than 0.8 mV. Most devices had less than 0.3 mV of offset drift.

A related problem is with short term power turn-on offset voltage shift. The 1/15/79 edition of Circuit News reported on this phenomenon. Some sample testing was also done at GE Ordnance Systems without finding any devices having this problem.

(LF155A/156A/157A Family)

The test yields of the LF155A series devices to the tighter limits of +/- 2 mV,+/- 2.5 mV were considerably lower than those for the non-A devices. Overall yields at 25°C, -55°C and 125°C were approximately 80%, 66% and 92% respectively.

Offset Voltage Temperature Sensitivity

(D-VIO/D-T)

(LF155/156/517 Family)

D-VIO/D-T is a very important parameter for applications having tight error specifications over a wide temperature range. Offset adjustment can not compensate for poor offset voltage drift. The user's only guarantee is to test for this parameter to screen out inferior devices. With limits of +/- 30 uV/°C, the non-A's had yields of 94% and 97% for the cold and hot excursions from 25°C.

(LF155A/56A/157A Family)

Even though the manufacturers' catalog limits of +/- 5 uV/°C were relaxed to +/- 10 uV/°C, the test yields for the A series devices were 43% and 90% for the cold and hot D-VIO/D-T measurements, respectively. It was later determined that the LF155A devices from vendor Code B were not prescreened to truly certify them as A's. Follow up tests with vendor Code B indicated that good yields could be achieved with the +/- 10 uV/°C limits. From 25°C to 125°C VIO is allowed to increase from +/- 2 mV to +/- 2.5 mV. This corresponds to an end point shift of 500 uV/100°C = 5 uV/°C.

Input Offset Current (IIO)

Since BI-FET op amp offset current is the difference between the two input leakage bias currents, it is very small and also difficult to measure. Only the zero common mode voltage condition is covered by the /114 specification. Test yields were 93.5% and 64% for the non-A's and A's respectively, against the +/- 20 pA limits. Most of the failures were traced to 156A's and 157A's from Vendor Code E. Test yields were worse for the "unspecified" -15V common mode condition because of front end matching considerations. At +15V common mode the test yield is better because the acceptance limit is raised to compensate for the higher input bias current.

Input Bias Current (+IIB, -IIB)

Figures 3-7 thru 3-10 show the sensitivity of input bias current to common mode voltage and power supply voltage. The slash sheet specification is based on +/- Vcc = +/- 20 V because of a precedent

established with previous military op amp specifications and a desire to maintain standards for comparison.

It should be obvious from these figures that if low IIB is a necessary application requirement, the supply voltages should be no higher than +/- 15 V. Also with the lower supply voltages, the common mode voltage range is more evenly centered about zero. As the common mode voltage approaches the negative power supply voltage, the P-N junction between the gate and channel of the input J-FETs becomes forward biased and forward current is pulled out of the gate. The input common mode voltage corresponding to this "forbidden" condition is within three volts of - Vcc.

Increasing the common mode voltage in the positive direction causes reverse leakage current to flow into the J-FET gate terminals. The common mode voltage range over which the input J-FETs are technically in the leakage mode varies according to diffusion characteristics, geometry and minority carries concentrations. Also the leakage current is almost independent of reverse voltage.

The typical diode shape increase in bias current with common mode voltage occurs as the junction enters the avalanche or zener voltage range. Series resistance prevents the classical zener constant voltage characteristic from occurring.

Process differences among the device manufacturers cause the bias current vs common mode voltage characteristics to vary accordingly. Since the input bias current is J-FET gate leakage it is not surprising that this current is highly temperature sensitive. Typically, leakage current doubles for every 10°C rise in temperature.

The test yields to the /114 specification limits were good except for the following:

1. Vendor Code E. LF155A series devices incorporating bias current compensation had a yield of only 16.6% for the negative common mode low limit of -100 pA. Bias current compensation uses negative PNP collector current to cancel positive J-FET gate current. At the negative common mode condition an over cancelled situation is more likely to occur. The JC-41 Committee has not asked for relief on this limit.

2. Vendor Code C. LF155 series devices had a yield of 30.7% for the 125°C input bias current limits of 50 mA and 60 mA at the zero and positive common mode conditions respectively. No relief has been asked for this limit.

Power Supply Rejection Ratio (+ PSRR, - PSRR)

All of the devices had good yields in meeting the 85 dB minimum limit.

Common Mode Rejection (CMR)

Good yields were obtained in meeting the 85 dB minimum limit. This parameter is calculated from the VIO change over the input common mode range. Consequently, there is a close relationship between VIO and CMR failures.

Input Offset Voltage Adjustment (V10 ADJ (+), V10 ADJ (-))

Traditionally, the requirement for offset voltage adjustment is that it be capable of driving the input offset voltage one millivolt beyond the minimum and maximum limits of offset voltage. All functional devices far exceeded this requirement with typical values of 13 mV and -14.3 mV for the positive and negative adjustments respectively.

Short Circuit Current (IOS (+), IOS (-))

The instantaneous short circuit current was considerably less than the 50 mA maximum requirement. The short circuit current magnitude decreases with increasing temperature for both output drive polarities. If the output is commanded to be at the positive swing limit and then a short circuit is made between the output and ground or the negative power supply, the short circuit current IOS (+), will be current limited by Q4 and R1 in Figure 3-1. Accordingly, typical IOS (+) =VBEQ4/R1 = 600 mV/25 = 24 mA. Since D-VBE/D-T = -2 mV/^{o}C, the self heating of the device and the output transistor, will cause the short circuit current to decrease by 80 uA/^{o}C.

Output short circuit protection cannot be guaranteed over the full -55^{o}C to 125^{o}C military temperature range.

Under worst case conditions, the maximum internal junction temperature of 175^{o}C will be exceeded at ambient temperatures far below 125^{o}C. The following equations apply:

1. $P_D = 2\ V_{cc}\ I_{cc} + |V_{cc} - V_o|\ I_{os}$
2. $T_J = T_A + P_D\ \theta_{J-A}$ where PD = device dissipation (mW)
   V_{cc} = power supply voltage (V)
   I_{cc} = power supply current (mA)
   V_o = output short circuit voltage (V)
   I_{os} = output shoprt circuit current (mA)
   T_J = junction temperature (^{o}C)
   T_A = ambient temperature (^{o}C)
   θ_{J-A} = device junction to ambient thermal resistance (^{o}C/mV)

Under worst case conditions and a "warmed-up" short circuit current of 30 mA, the devices have the following maximum safe ambient temperatures:

Device Type	Maximum Safe Ambient* Temperature "short" to ground	"short" to supply
01, 04	89.5°C	22°C
02, 03, 05, 06	76°C	9°C

*TA at TJ = 175°C

Several 02 and 03 devices were subjected to sustained output to power supply short circuits for several hours without incurring any damage. The real margin of safety depends on the differences between worst case and typical parameters.

Supply Current (Icc)

Supply current is one of the parameters which is different for each device type in the LF155 series family. The Icc limits are well chosen for the device data distribution.

Output Voltage Swing ($+V_{op}$, $-V_{op}$)

Maximum output voltage swing is generally well behaved with a tight histogram pattern and a mean value which is two volts or better than the specification limit.

Open Loop Voltage Gain (AVS (+), AVS (-)

But for one exception, the data distribution of open loop voltage gain far exceeded the minimum specification. Characteristically, the gain histograms have a scattered distribution. There were no wrong polarity gains, thus indicating better management of thermal effects than were observed on many op amps during previous characterization studies. LF155A devices from vendor Code B had many gain failures at -55°C. Vendor Code B test yields at -55°C were 50%, 15.8% and 16.6% for their LF155A, LF156A and LF157A devices respectively. These same devices had respectable gains at 25°C and 125°C.

Slew Rate (SR (+), SR (-))

Each of the six device types is characterized by a different slew rate specification. Within the non-A and A groups of devices, slew rate is traded off with supply current to offer the user three design options. In most cases negative slew rate was faster than positive slew rate by almost 2:1.

(LF155/156/157 Family)

All of the devices had good yields to their respective specification limits, except for LF156's from Vendor Code C, which had yields of 22% and 0% at 25°C and 125°C respectively.

(LF155A/156A/157A Family)

With the exception of Vendor Code F, 156A devices, which had a test yield of 50%, all of the data was well within the specification limits. The failed 156A devices would pass the 156 limits (i.e. 7 V/us vs 10 V/us). Compared with bipolar op amps, BI-FET op amps have a much better combination of high slew rate and low input bias current.

Transient Response (TR (tr), TR (OS))

With a closed loop gain of 1 V/V, the transient response data of the LF155 and LF156 devices was significantly faster than the initial JC-41 Committee recommended limits.

Also the LF157 devices at a closed loop gain of 5 V/V were slower than the JC-41 Committee recommended limits. The data and limits are summarized below:

Device Type	JC-41 Limits				Data 25°C				
	TR(tr) (ns)		TR(OS) (%)		TR(tr) (ns)		TR(OS) (%)		
AV	(min)	(max)	(min)	(max)	(min)	(max)	(min)	(max)	Sample Size
LF155 1V/V	-	300	-	40	41	55	33	47	15
LF156 1V/V	-	200	-	40	28	45	42	48	15
LF157 5V/V	-	100	-	40	240	310	0	0	15

In order to resolve the differences between the recommended limits and the data, a second referee circuit was built and several devices were tested again. The new data correlated with the original data.

After verifying that the data matched, the sensitivity of the data to the circuit components was investigated. Not surprisingly, the feedback capacitor has a dominant effect. For instance a change from 10 pf to 18 pf caused the overshoot of an LF156A to decrease from 44% to 32%. Figure 3-16 shows the typical response of an LF155 and LF156 device. The high TR(OS) overshoot failure rate was resolved by modifying the test circuit such that AV = 1 V/V, RF = 0 ohm. Normally closed K9 contacts in parallel with the 10 K ohm resistor of Figure 3-3 reduces the D.U.T. overshoot by making the device less susceptible to parasitic capacitance at the inverting input. Typically, depending on the D.U.T.'s characteristics, a reduction of 10% to 20% in overshoot was achieved.

Closed loop gain has a big effect on the transient response of an LF157 as can be seen in the Appendix, Figure 3-16.

Rise time and overshoot changed from 15 nanoseconds and 130% to 250 nanoseconds and 0%, respectively, when the closed loop gain was increased from 1 V/V to 5 V/V. In raising the closed loop gain, the open loop gain is reduced by 14 dB and the effect of the high frequency poles and zeros is greatly reduced.

The revised transient response specification limits are shown in Table 3-17.

Settling Time (ts(+), ts(-)

Settling time as defined in the /114 specification is a sampled large signal test for the time it takes the error voltage to settle within 0.1% of its final value. A phantom summing mode is monitored as shown in Figure 3-5 while the DUT is exercised to produce a 10 V output pulse. This summing node voltage VN is proportional to the error voltage difference VE between the input and output voltage as shown below:

$$VN = VIN * RF/(R1 + RF) + Vo * R1(R1 + RF)$$
$$VN = VIN * RF/(R1 + RF) - RF/(R1) * VIN * R1/(R1 + RF)$$
$$VN = VE * RF/(R1 + RF)$$

Thus for circuit gains of - 1 V/V and - 5 V/V, the null voltage is .5 VE and .833 VE, respectively. For a 10 V output and 0.1% error, the corresponding null voltage thresholds are 5 mV and 8.33 mV at AV = 1 V/V and 5 V/V respectively.

Figure 3-19 shows the dynamic null error voltage of several typical devices. The settling time is composed of a slewing interval and transient response interval, which depend on different parameters and conditions. For a given device the slewing interval is proportional to the output step change, whereas the transient response interval is dependent on the damping ratio of the device in the test circuit.

The circuit closed loop gain has a big effect on both the slewing interval and the transient response interval. Depending on how the response oscillations dampen, the difference between 0.1% and .01% settling time can vary from a fractional part of cycle to several cycles.

The relationship between the data and the proposed limits is tabulated below:

Device Type AV	Data @ 25°C ts in (ns) (min)	(max)	Sample Size	/114A ts in (ns) (min)	(max)
LF155 1V/V	700	1300	15	-	1500
LF156 1V/V	900	1300	15	-	1500
LF157 5V/V	300	650	15	-	800

Noise (NI (BB), NI (PC))

Broadband and pop corn noise was measured with a Tektronix Type 577 curve tracer. Typical data displays are shown in Figure 3-21 in the Appendix.

Broadband noise was measured with a source resistance of 50 ohms and the observed peak-to-peak readings were divided by six to yield Gaussian rms values.

This factor of six is used because op amp noise voltage is random and has a normal statistical distribution. One of the properties of a normal Gaussian distribution is that the ratio of the peak-to-peak value over the rms value is six with a probability of 99.7%.

The data is summarized as follows:

Broadband Noise (u Vrms)	Data Frequency
0.3	1
0.7	5
0.8	3
1.0	10
1.2	1
1.3	3
1.7	1
Total:	24 data values

The data distribution is conservatively within the 10 u Vrms maximum limits of the /114 specification.

For the popcorn noise test only one device had an observed "pop" of 10 uPK. The remaining 23 devices had no trace of popcorn noise.

Burn-in Circuit Evaluation

After the initial characterization data was taken, sixty non-A devices were burned-in using two different circuit configurations. Twenty-eight devices were exercised in the original voltage follower circuit which uses a 2000 ohm load. During this 168 hour burn-in test, the input was changed from + 5 V to - 5 V after approximately half of the time had elapsed. The remaining 32 devices were exercised on a new simplified circuit which has the inputs grounded and the outputs open. Maximum supply voltage of +/- 22 VDC were applied to these devices, whereas only +/- 20 VDC was applied to the first group. The two sample populations were chosen such that they equal representation with regard to vendor and date code.

At the conclusion of the 168 hours, 125°C test, the devices were cooled down before power was removed. The serialized devices were again tested on the S-3260. The following observations were made after comparing the before and after test data:

1. For both test circuits the post burn-in data total failures did not exceed the total pre burn-in failures. In other words good devices, in general, are not harmed by either test circuit.

2. Quite often on particular devices pre burn-in failures did not appear at post burn-in. These were mainly IIO and IIB technical limit failures.

It was concluded that the new simplified burn-in circuit was equally effective with the old standard test circuit. Subsequently, it was recommended that the supply voltages be reduced to +/- 20 V and the pin 5 offset adjust pin be connected to + Vcc.

GEOS uses many LF156's for signal conditioning and processing in automatic test equipment for measuring guidance system parameters. Because of high failure rates in the prototype test system, it was decided to burn-in all LF156's to be used in that program. Succeeding systems had much better reliability. At this time (August 1980) it is not conclusive if the original high failure rate was primarily caused by induced system failures or defective devices.

In three 50-device lots, the percentage of catastrophic burn-in failures were 16%, 6% and 18%. Most of the failures tend to be output oriented. Daily monitoring of the devices in a burn-in rack has shown that some defective devices experience a gradual degradation in negative output swing toward zero, followed by a burn-out which leaves the output stuck at -Vcc.

The most recent burn-in lot included devices from three sources. No catastrophic failures were observed, although final data is not yet available for analysis. The manufacturer of the previous lots has recently stated that a device problem was present and that a mask change is planned to eliminate the problem.

Testing Problems

Input bias current was the most difficult parameter to measure because of its small magnitude (pA range). Using the standard op amp test circuit with input bias current dropping resistor of 5 meg ohms each, the bias current effect on offset voltage was typically less than 10%. Also high value input resistors tend to de-stabilize the test circuit because parasitic capacitance feedback coupling from the output to the non-inverting input is relatively unattenuated. Had the scope of these problems been fully recognized at the beginning of the characterization program, a different test technique would have been developed. Experience with the LF198 sample and hold, which is also a BI-FET, and discussions with several manufacturers indicate that a charge integration method is more practical.

3.6 Slash Sheet Development

The military specification (MIL-M-38510 slash sheet) on the BI-FET op amps was developed in parallel with the characterization effort. As the test circuits and procedures were proofed out in the taking of device data, they were also incorporated into the slash sheet. The original slash sheet Table I parameters and limits were recommended by the JC-41 Committee on Linear Integrated Circuits. With few exceptions, the device testing and screening was done against these parameters and limits. As progress was being made on the device characterization, a dialogue was maintained with the manufacturers over the phone and at meetings. One of the more significant developments that happened was in the specification of input bias current over the common mode voltage range. The end result in the specification shows that the maximum input bias current changes from 3500 pA to 300 pA for a power supply change from +/- 20 V to +/- 15 V at the positive common voltage. For both conditions, + Vcm is five volts below + Vcc.

3.7 Conclusions and Recommendations

204 generic LF155 series op amps were tested on GEOS' S-3263 to characterize their electrical parameters. Sampled bench test data was taken to characterize noise and some of the dynamic electrical characteristics, which could not be tested on the S-3263. It should be noted that the electrical characteristics are oriented toward automatic testing. With the exceptions of input bias current, input offset current, and output short circuit current, the effects of device self heating will not cause the specification values to differ from application values.

In order to minimize input bias currents and device power dissipation it is recommended that the power supply voltage be kept no higher than +/- 16 V. Although these BI-FET op amps are guaranteed to operate at 125°C ambient temperature, high temperature operation will cause the benefits of low input bias currents to be lost.

The LF155 series of BI-FET op amps have several advantages over bipolar devices including a more optimum combination of low bias current and high slew rate, plus the ability to drive high capacitance loads.

Final recommended electrical specifications for the generic LF155 series op amps in MIL-M-38510/114 are shown in Table 3-17.

3.8 Bibliography

1. Author R. Russell and T. Frederiksen, "How the BI-FET process benefits linear circuits", Electronics, June 8, 1980.

2. Linear Applications Handbook, National Semiconductor (1978).

3. Linear Databook, National Semiconductor (1978).

Table 3-17. LF155/6/7 Data Summary.

LF155/6/7 PARAMETER DISTRIBUTIONS & LIMITS

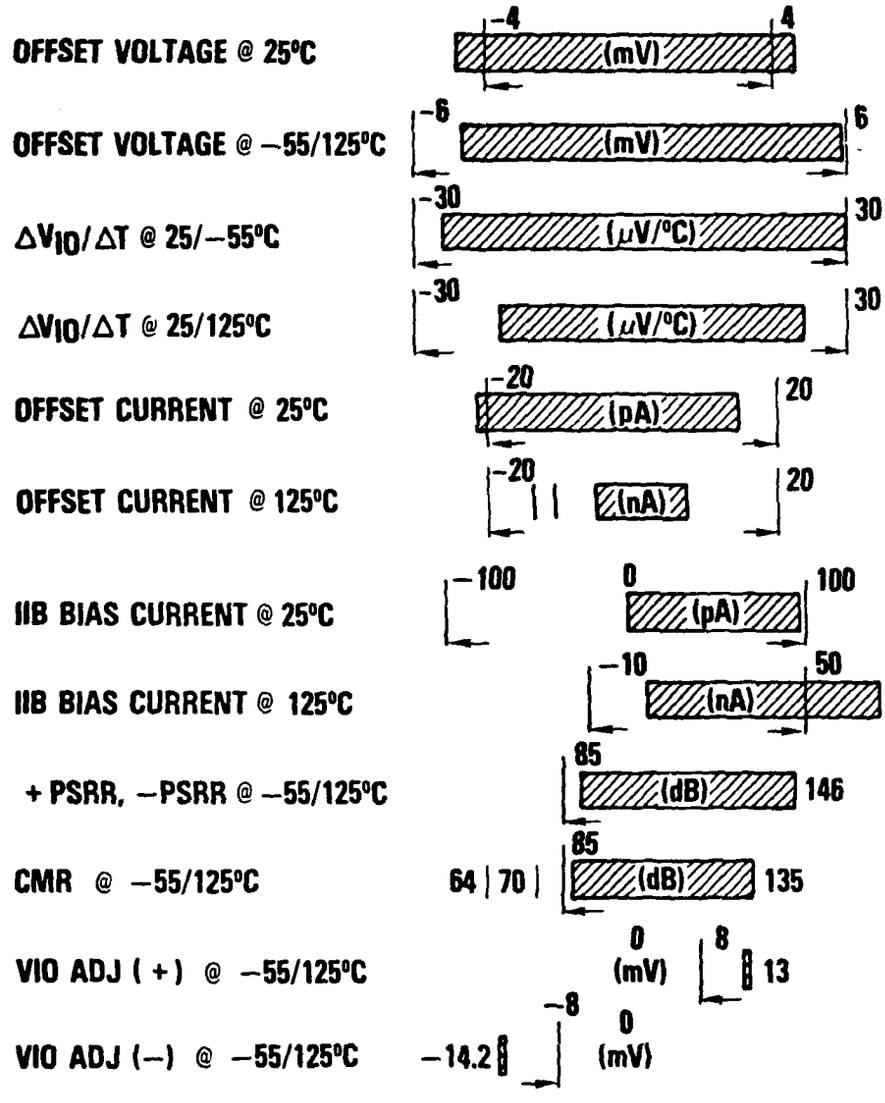


Table 3-17. LF155/6/7 Data Summary (Cont'd)

LF 155/6/7 PARAMETER DISTRIBUTIONS & LIMITS

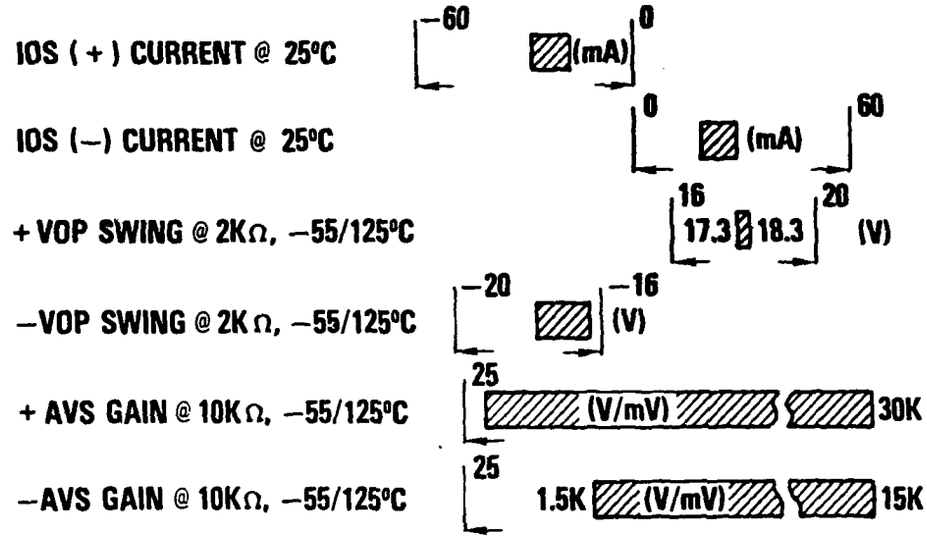
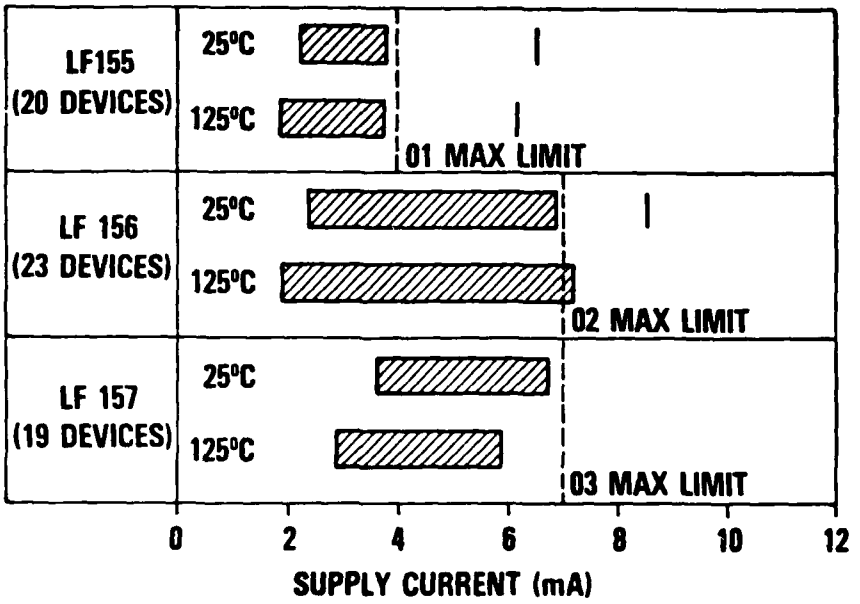
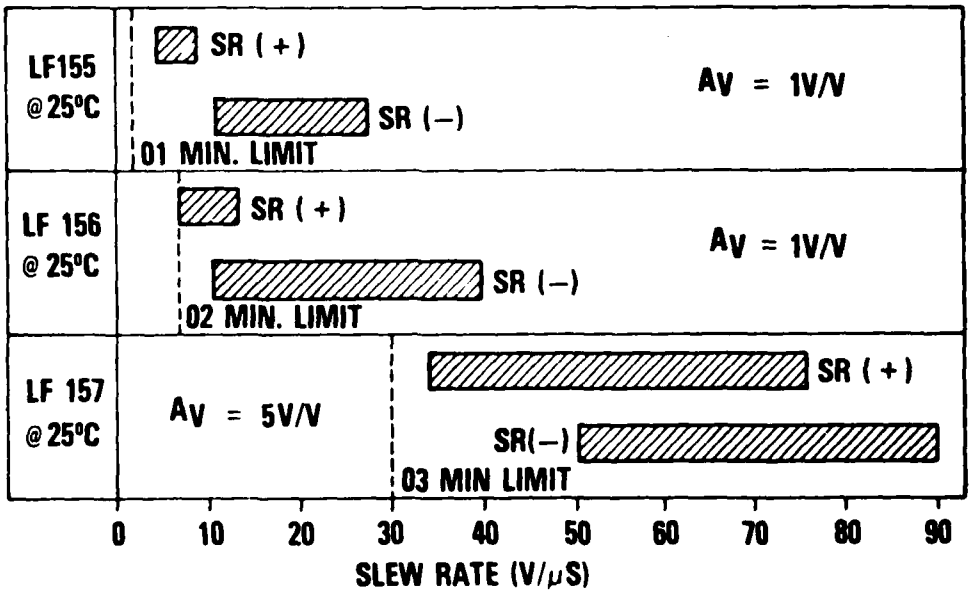


Table 3-18. LF155/6/7 Supply Current & Slew Rate vs. Device Type.

SUPPLY CURRENT vs DEVICE TYPE @ $\pm V_{CC} = \pm 15V$



SLEW RATE RANGE vs DEVICE TYPE



Characteristics	Symbol	Conditions ($\pm V_{CC} = \pm 20$ V unless otherwise specified)	Device	Limits Min.	Limits Max.	Units
Input offset voltage	V_{IO}	$\pm V_{CC} = \pm 5$ V, $V_{CM} = 0$ V, $T_A = 25°C$	04,05,06	- 2	2	mV
			01,02,03	- 5	5	mV
		$\pm V_{CC} = \pm 20$ V, $V_{CM} = \pm 15$ V, 0 V, $-55°C \leq T_A \leq +125°C$	04,05,06	-2.5	2.5	mV
			01,02,03	- 7	7	mV
Input offset voltage temperature sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{CC} = \pm 20$ V, $V_{CM} = 0$ V	01,02,03	-30	30	uV/°C
			04,05,06	-10	10	
Input offset current	I_{IO}	$\pm V_{CC} = \pm 20$ V, $T_J = 25°C$	all	-20	20	pA
		$V_{CM} = 0$ V, $t \leq 25$ ms, $T_J = 125°C$	all	-20	20	nA
Input bias current	+ I_{IB}	$\pm V_{CC} = \pm 20$ V, $T_J = 25°C$	all	-100	3500	pA
		$V_{CM} = +15$ V, $t \leq 25$ ms, $T_J = 125°C$	all	-10	60	nA
	- I_{IB} 1/	$\pm V_{CC} = \pm 15$ V, $T_J = 25°C$	all	-100	300	pA
		$V_{CM} = +10$ V, $t \leq 25$ ms, $T_J = 125°C$	all	-10	50	nA
	2/	$\pm V_{CC} = \pm 20$ V, $T_J = 25°C$	all	-100	100	pA
	3/	-15 V $\leq V_{CM} \leq 0$ V, $t < 25$ ms, $T_J = 125°C$	all	-10	50	nA
Power supply	+PSRR	$+V_{CC} = 10$ V, $-V_{CC} = -20$ V	all	85	---	dB
	-PSRR	$+V_{CC} = 20$ V, $-V_{CC} = -10$ V	all	85	---	dB
Input voltage common mode rejection 4/	CMR	$\pm V_{CC} = \pm 20$ V, $V_{IN} = \pm 15$ V	all	85	---	dB

See footnotes at end of table.

Table 3-19. Proposed electrical performance characteristics for MIL-M-38510/114.

Characteristics	Symbol	Conditions ($\pm V_{CC} = \pm 20$ V unless otherwise specified)		Device	Limits Min.	Limits Max.	Units
Adjustment for input offset voltage	$V_{IO\ ADJ(+)}$	$\pm V_{CC} = \pm 20$ V		all	+ 8	---	mV
	$V_{IO\ ADJ(-)}$	$\pm V_{CC} = \pm 20$ V		all	---	- 8	mV
Output short circuit current (for positive output) 5/	$I_{OS(+)}$	$\pm V_{CC} = \pm 15$ V $t \leq 25$ mS (Short circuit to ground)		all	-50	---	mA
Output short circuit current (for negative output) 5/	$I_{OS(-)}$	$\pm V_{CC} = \pm 15$ V $t \leq 25$ mS (Short circuit to ground)		all	---	50	mA
Supply current	I_{CC}	$\pm V_{CC} = \pm 15$ V	$T_A = -55°C$	01,04 02,03,05,06	--- ---	6 11	mA
			$T_A = +25°C$	01,04 02,03,05,06	--- ---	4 7	
			$T_A = +125°C$	01,04 02,03,05,06	--- ---	4 7	
Output voltage swing (maximum)	V_{OP}	$\pm V_{CC} = \pm 20$ V, $R_L = 10$ KΩ		all	±16	---	V
		$\pm V_{CC} = \pm 20$ V, $R_L = 2$ KΩ		all	±15	---	
Open loop voltage gain (single ended) 6/	$A_{VS(\pm)}$	$\pm V_{CC} = \pm 20$ V $R_L = 2$ KΩ $V_{OUT} = \pm 15$ V	$T_A = 25°C$	all	50	---	V/mV
			$-55°C \leq T_A \leq +125°C$	all	25	---	
Open loop voltage gain (single ended) 6/	A_{VS}	$\pm V_{CC} = \pm 5$ V $R_L = 2$ KΩ $V_{OUT} = \pm 2$ V		all	10	---	V/mV

See footnotes at end of table.

Table 3-19. Proposed Electrical Performance Characteristics For MIL-M-38510/114.

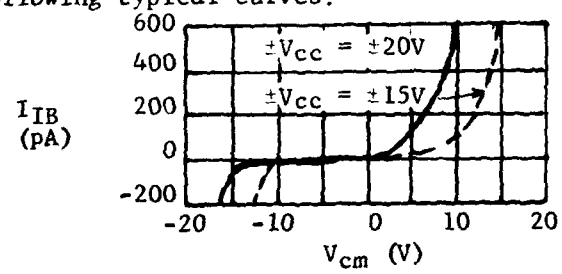
Characteristics	Symbol	Conditions ($\pm V_{CC} = \pm 20$ V unless otherwise specified)		Device	Limits Min.	Limits Max.	Units
Transient response rise time	TR(tr)	$\pm V_{CC} = \pm 15$ V $R_L = 2$ KΩ $C_L = 100$ pf See Figure 8	$A_V = 1$	01,04 02,05	--- ---	150 100	ns
			$A_V = 5$	03,06	---	450	
Transient response overshoot	TR(OS)		$A_V = 1$	01,02,04,05	---	40	%
			$A_V = 5$	03,06	---	25	
Slew rate	SR(+) and SR(-)	$V_{IN} = \pm 5$ V $\pm V_{CC} = \pm 15$ V $A_V = 1$ see Figure 8	$T_A = 25°C$	01 02 04 05	2 7.5 3 10	--- --- --- ---	V/us
			$T_A = -55°C, 125°C$	01 02 04 05	1 5 1.5 7	--- --- --- ---	
		$V_{IN} = \pm 5$ V $\pm V_{CC} = \pm 15$ V $A_V = 5$ See Figure 8	$T_A = 25°C$	03 06	30 40	--- ---	
			$T_A = -55°C, 125°C$	03 06	20 25	--- ---	
Settling time	ts(+) and ts(-)	$\pm V_{CC} = \pm 15$ V (0.1% error) $T_A = 25°C$ See Figure 9	$A_V = 1$	01,02,04,05	---	1500	ns
			$A_V = 5$	03,06	---	800	
Noise (referred to input) broad-band	N_I(BB)	$\pm V_{CC} = 20$ V Bandwidth = 5kHz	$T_A = 25°C$	all	---	10	uV_{rms}
Noise (referred to input) popcorn	N_I(PC)		$T_A = 25°C$	all	---	80	uV_{pk}

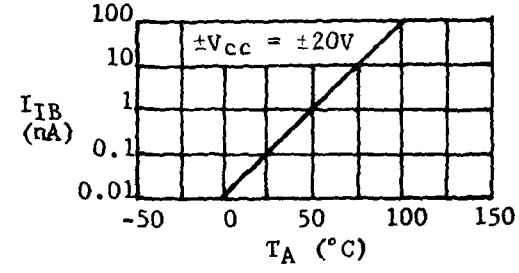
Table 3-19. Proposed Electrical Performance Characteristics For MIL-M-38510/114.

NOTES:

1/ Bias currents are actually junction leakage currents which double (approximately) for each 10°C increase in junction temperature T_J. Measurement of bias current is specified at T_J rather than T_A, since normal warmup thermal transients will affect the bias currents. The measurements for bias currents must be made within 25 ms after power is first applied to the device for test. Measurement at T_A = -55°C is not necessary since expected values are too small for typical test systems.

2/ Bias current is sensitive to power supply voltage, common mode voltage and temperature as shown by the following typical curves:





3/ Negative I_{IB} minimum limits reflect the characteristics of devices with bias current compensation.

4/ CMR is calculated from V_{IO} measurements at V_{CM} = + 15 V and - 15 V.

5/ Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that T_J (max) $\leq$ 175°C.

6/ Because of thermal feedback effects from output to input, open loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

Table 3-19. *Proposed* Electrical Performance Characteristics For MIL-M-38510/114.

SECTION III
APPENDIX

BIFET OP AMPS

MIL-M-38510/114

Parameter Symbol	Notes	Applied Voltages Adapter pin numbers 1	2	3	4	Energized Relays	Measured pin No.	Value	Units	Equation	Units
V_{IO}	2/	35 V	- 5 V	Open	-15 V	None	5	E_1	V	$V_{IO} = E_1$	mV
		5 V	-35 V		15 V			E_2		$V_{IO} = E_2$	
		20 V	-20 V		0 V			E_3		$V_{IO} = E_3$	
		5 V	- 5 V		0 V			E_4		$V_{IO} = E_4$	
$+I_{IB}$		5 V	-35 V		15 V	K1, K8		E_5		$-I_{IB} = 10{,}000\ (E_2 - E_5)$	pA
	8/	5 V	-25 V		10 V	None		E_6		$+I_{IB} = 200\ (E_6 - E_7)$	
		5 V	-25 V		10 V	K1		E_7			
		20 V	-20 V		0 V	K1		E_8		$+I_{IB} = 200\ (E_3 - E_8)$	
		35 V	- 5 V		-15 V	K1		E_9		$-I_{IB} = 200\ (E_1 - E_9)$	
$-I_{IB}$		5 V	-35 V		15 V	K2, K8		E_{10}		$-I_{IB} = 10{,}000\ (E_{10} - E_2)$	
	8/	5 V	-25 V		10 V	None		E_{11}		$-I_{IB} = 200\ (E_{12} - E_{11})$	
		5 V	-25 V		10 V	K2		E_{12}			
		20 V	-20 V		0 V	K2		E_{13}		$-I_{IB} = 200\ (E_{13} - E_3)$	
		35 V	- 5 V		-15 V	K2		E_{14}		$-I_{IB} = 200\ (E_{14} - E_1)$	
I_{IO}	Calculate value using V_{IO}, $+I_{IB}$ and $-I_{IB}$ data									$I_{IO} = 200\ (2E_3 - E_8 - E_{13})$	pA

Table 3-4. Test Table For Static Tests.

Parameter Symbol	Notes	Applied Voltages Adapter pin numbers 1	2	3	4	Energized Relays	Measured pin No.	Value	Units	Equation	Units
+PSRR		10 V	-20 V	Open	0 V	None	5	E_{15}	V	$+PSRR = 20 \log \frac{10^4}{(E_3 - E_{15})}$	dB
-PSRR		20 V	-10 V	Open	0 V	None		E_{16}		$-PSRR = 20 \log \frac{10^4}{(E_3 - E_{16})}$	
CMR	3/	Calculate value using V_{IO} data								$CMR = 20 \log \frac{3 \times 10^4}{(E_1 - E_2)}$	dB
$V_{IO\ ADJ(+)}$		20 V	-20 V	Open	0 V	K7	5	E_{17}	V	$V_{IO\ ADJ(+)} = E_3 - E_{17}$	mV
$V_{IO\ ADJ(-)}$		20 V	-20 V		0 V	K6, K7		E_{18}		$V_{IO\ ADJ(-)} = E_3 - E_{18}$	
$I_{OS(+)}$	5/	15 V	-15 V		-10 V	None	6	I_1	mA	$I_{OS(+)} = I_1$	mA
$I_{OS(-)}$		15 V	-15 V		10 V	None		I_2		$I_{OS(-)} = I_2$	
I_{CC}		15 V	-15 V		0 V	None	2	I_3	mA	$I_{CC} = I_3$	mA
$+V_{OP}$		20 V	-20 V	Open	-20 V	K3	6	$(E_0)_1$	V	$+V_{OP} = (E_0)_1$	V
$-V_{OP}$					20 V	K3		$(E_0)_2$		$-V_{OP} = (E_0)_2$	
$+V_{OP}$					-20 V	K4		$(E_0)_3$		$+V_{OP} = (E_0)_3$	V
$-V_{OP}$					20 V	K4		$(E_0)_4$		$-V_{OP} = (E_0)_4$	

Table 3-4. Test Table For Static Tests. (cont'd)

Table 3-4. Test Table For Static Tests. (cont'd.)

Parameter Symbol	Notes	Applied Voltages Adapter pin numbers 1	2	3	4	Energized Relays	Measured pin No.	Value	Units	Equation	Units
$A_{VS(+)}$	4/	20 V	-20 V	Open	-15 V	K4	5	E_{19}	V	$A_{VS(+)} = 15/(E_3 - E_{19})$	V/mV
$A_{VS(-)}$					15 V			E_{20}		$A_{VS(-)} = 15/(E_{20} - E_3)$	
A_{VS}		5 V	- 5 V		- 2 V			E_{21}		$A_{VS} = 4/(E_{22} - E_{21})$	V/mV
		5 V	- 5 V		2 V			E_{22}			
NI(BB)	6/	20 V	-20 V		0 V	K5	6	$(E_0)_5$	mVrms	NI(BB) = $(E_0)_5/1000$	uVrms
NI(PC)		20 V	-20 V		0 V	K1,K2,K5,K8		$(E_0)_6$	mVpk	NI(PC) = $(E_0)_6/1000$	uVpk
$\Delta V_{IO}/\Delta T$	7/	$\Delta V_{IO}/\Delta T = (V_{IO}$ @ 125°C - V_{IO} @ 25°C$)/100°C$									uV/°C

NOTES:

1/ The equations take into account both the closed loop gain of 1,000 and the scale factor multiplier so that the calculated value is in Table I units. The measured value units should, therefore, be used in the equation. (For example: If E_1 = 2 V and $V_{IO} = E_1$, then V_{IO} = 2 mV.)

2/ Each device shall be tested over the common mode range as specified in Table 2-1. V_{cm} conditions are achieved by grounding the inputs and algebracially subtracting V_{cm} from each supply. (For example: If V_{cm} = - 15 V, then + V_{cc} = + 20 V - (- 15) = + 35 V and - V_{cc} = - 20 V - (- 15) = - 5 V.

3/ Common mode rejection is calculated using the offset voltage values measured at the common mode range end points.

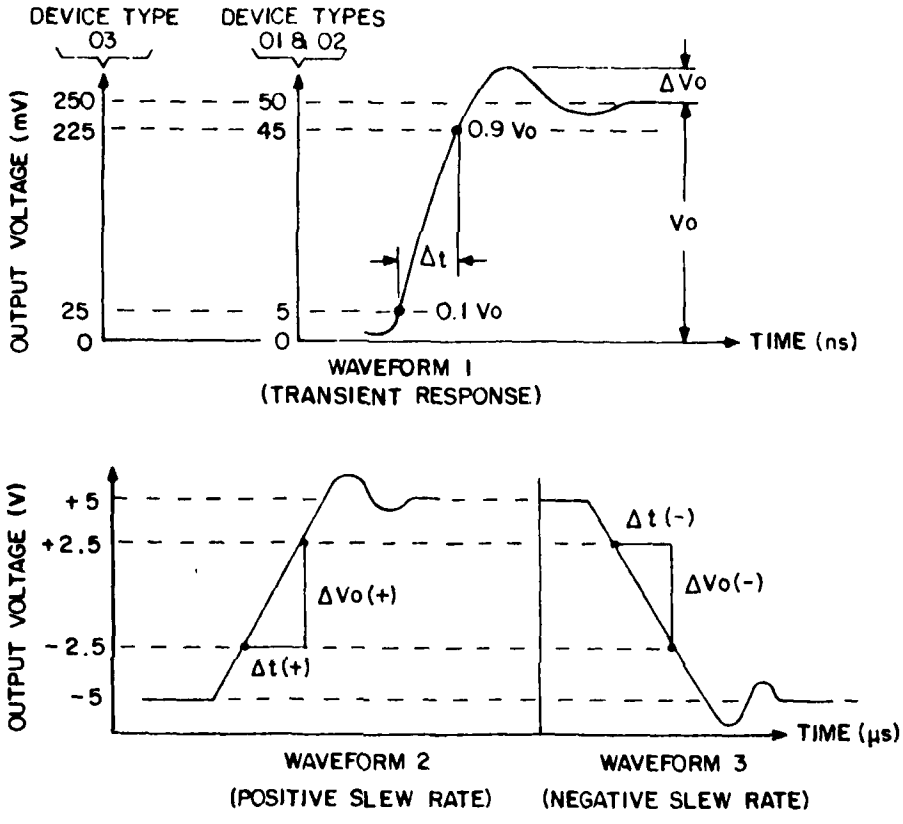
4/ To minimize thermal drift the reference voltage for the gain measurement (E_3) shall be taken immediately prior to or after the reading corresponding to device gain (E_{19}, E_{20}).

5/ The output shall be shorted to ground for 25 ms or less.

6/ Broadband noise NI(BB) shall be measured using an RMS voltmeter with a bandwidth of 10 Hz to 5 kHz. "Popcorn" noise NI(PC) shall be measured for 15 seconds.

7/ $\Delta V_{io}/\Delta T$ drift between 125°C and 25°C is shown. $\Delta V_{io}/\Delta T$ drift between - 55°C and 25°C is calculated in a similar manner.

8/ For tests at 125°C, K8 is energized and the equation coefficient changes from 200 to 10,000.



Parameter symbol	Device type	Input pulse signal @ $t_r \leq 50$ ns	Output pulse signal	Equation
TR (t_r)	all	+50 mV	Waveform 1	TR (t_r) = Δt
TR (o_s)	all	+50 mV	Waveform 1	$TR_{(o_s)} = 100\ (^{\Delta Vo}/_{Vo})$
SR (+)	01,02	-5 V to +5 V step	Waveform 2	$SR(+) = {}^{\Delta Vo(+)}/_{\Delta t(+)}$
	03	-1 V to +1 V step	Waveform 2	
SR (-)	01,02	+5 V to -5 V step	Waveform 3	$SR(-) = {}^{\Delta Vo(-)}/_{\Delta t(-)}$
	03	-1 V to +1 V step	Waveform 3	

Table 3-5. Test Table For Transient Response and Slew Rate.

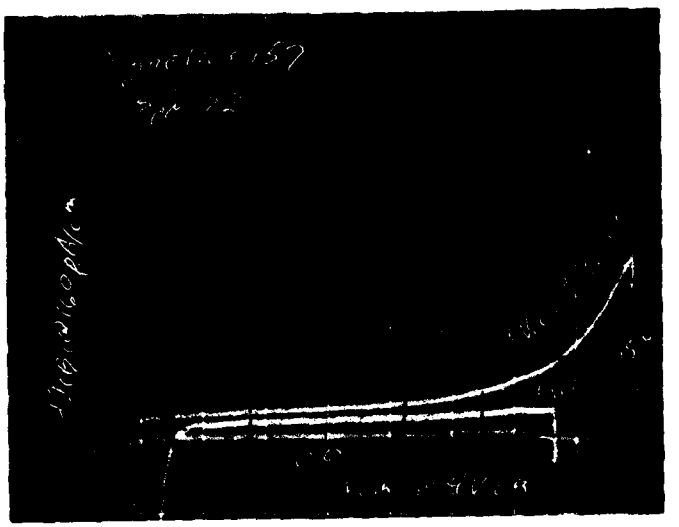
BI-FET OPERATIONAL AMPLIFIERS - 155A ; TEMPERATURE: +25 DEG C ; 04 APR 79 14:46:16

Vendor Code A

PARAMETER	LO-LIM	85	86	87	88	89	90	91	92	93	94	HI-LIM	UNIT
VIO(-CM) AT 35V,-5V	-8.00	-1.68	1.36	3.47 *	436.M	-3.45 *	-678.M	8.69 *	-1.27	-3.93 *	675.M	2.00	MV
VIO(+CM) AT 5V,-35V	-8.00	-1.37	1.07	3.06 *	518.M	-3.22 *	-1.78	8.11 *	-2.00	-3.46 *	-45.8M	2.00	MV
VIO(0CM) AT 20V,-20V	-8.00	-1.43	1.13	3.23 *	488.M	-3.37 *	-1.86	8.33 *	-1.85	-3.59 *	49.4M	2.00	MV
VIO(0CM) AT 5V,-5V	-8.00	-1.88	1.34	3.41 *	515.M	-3.60 *	-618.M	2.64 *	-1.30	-4.06 *	589.M	2.00	MV
D-VIO/D-T FROM 25 OC	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	UV/C
IIO(-CM) AT 35V,-5V	-20.0	12.7	8.36	24.0 *	10.2	22.8 *	10.2	10.6	23.0 *	2.18	959.M	20.0	PA
IIO(+CM) AT 5V,-35V	-400.	-168.	-121.	-22.3	-91.2	-57.2	-96.4	-65.9	9.36	-208.	-101.	400.	PA
IIO(0CM) AT 20V,-20V	-20.0	1.28	809.M	19.4	-6.71	9.63	-7.70	5.98	18.5	-24.4 *	-8.91	20.0	PA
IIO(+CM) AT 5V,-25V	-20.0	-8.58	-3.38	18.3	-16.2	-235.M	-17.1	4.75	22.3 *	-35.4 *	-13.0	20.0	PA
+IIB(-CM) AT 35V,-5V	-100.	6.56	14.6	33.3	26.0	54.6	16.8	12.3	46.1	8.81	16.2	100.	PA
+IIB(+CM) AT 5V,-35V	-100.	1.64K	1.40K	856.	1.04K	1.17K	1.37K	1.27K	754.	1.65K	1.62K	3.50K	PA
+IIB(0CM) AT 20V,-20V	-100.	66.4	46.1	72.6	41.5	85.9	43.5	39.8	83.0	37.0	38.5	100.	PA
+IIB(+CM) AT 5V,-25V	-100.	128.	91.7	103.	74.1	118.	86.9	85.0	114.	93.7	82.7	300.	PA
-IIB(-CM) AT 35V,-5V	-100.	-6.14	12.2	8.36	15.7	31.8	6.58	1.76	23.1	6.62	15.2	100.	PA
-IIB(+CM) AT 5V,-35V	-100.	1.80K	1.52K	878.	1.13K	1.23K	1.47K	1.33K	745.	1.86K	1.62K	3.50K	PA
-IIB(0CM) AT 20V,-20V	-100.	65.1	45.3	53.2	48.2	76.2	51.2	33.9	64.5	61.3	47.4	100.	PA
-IIB(+CM) AT 5V,-25V	-100.	135.	95.1	84.8	90.3	119.	104.	80.3	91.9	129.	95.7	300.	PA
+PSRR AT 10V,-20V	85.0	117.	120.	111.	108.	108.	132.	109.	114.	115.	110.	0.00	dB
-PSRR AT 20V,-10V	85.0	110.	122.	108.	109.	106.	107.	106.	106.	200.	142.	0.00	dB
CMR AT 20V,-20V	85.0	99.7	100.	97.3	111.	102.	88.1	94.1	92.3	96.2	92.4	0.00	dB
IOS(+) AT 15V,-15V	-50.0	-19.0	-19.5	-20.9	-21.5	-20.9	-17.4	-20.4	-21.3	-19.9	-20.5	0.00	MA
IOS(-) AT 15V,-15V	0.00	18.7	19.5	21.1	21.2	18.7	17.3	20.5	20.7	19.4	20.0	50.0	MA
ICC AT 15V,-15V	0.00	3.23	3.16	3.25	3.23	2.30	3.32	3.74	3.60	2.75	3.43	4.00	MA
ICC AT 20V,-20V	0.00	3.66	3.58	3.64	3.61	2.47	3.76	4.26	4.12	3.09	3.81	5.00	MA
+VOP AT RL=10K	16.0	18.4	18.4	18.4	18.4	18.4	18.4	18.5	18.4	18.4	18.4	20.0	V
-VOP AT RL=10K	-20.0	-18.5	-18.5	-18.6	-18.5	-18.5	-18.4	-18.5	-18.6	-18.5	-18.5	-16.0	V
+VOP AT RL=2K	15.0	18.1	18.1	18.0	18.1	18.1	18.1	18.1	17.9	18.1	18.1	20.0	V
-VOP AT RL=2K	-20.0	-17.4	-17.4	-16.9	-17.1	-17.1	-17.2	-17.4	-16.5	-17.4	-17.4	-15.0	V
AVS(+) AT RL=10K	50.0	1.50K	3.00K	1.00K	1.76K	3.00K	1.50K	1.50K	750.	1.50K	968.	0.00	V/MV
AVS(-) AT RL=10K	50.0	3.00K	100.K	1.50K	6.00K	3.00K	100.K	100.K	100.K	100.K	30.0K	0.00	V/MV
AVS(+) AT RL=2K	50.0	3.00K	1.50K	1.50K	15.0K	3.00K	1.00K	1.00K	750.	1.50K	1.20K	0.00	V/MV
AVS(-) AT RL=2K	50.0	500.	800.	800.	429.	750.	429.	800.	273.	500.	508.	0.00	V/MV
AVS AT 5V,-5V,RL=10K	10.0	267.	800.	267.	148.	800.	258.	160.	114.	800.	471.	0.00	V/MV
AVS AT 5V,-5V,RL=2K	10.0	800.	800.	400.	400.	800.	1.14K	800.	267.	800.	667.	0.00	V/MV
SR(+) AT 20V,-20V	3.00	7.14	6.58	8.55	9.01	8.00	7.87	7.84	10.1	6.37	7.84	0.00	V/US
SR(-) AT 20V,-20V	3.00	10.2	14.6	21.3	23.8	21.3	18.5	18.9	21.3	13.9	16.9	0.00	V/US
V-ADJ(+) AT 20V,-20V	8.00	13.0	13.1	13.1	13.1	13.0	13.0	13.1	13.0	13.0	226.MS	20.0	MV
V-ADJ(-) AT 20V,-20V	-20.0	-14.3	-14.2	-14.2	-14.2	-14.3	-14.3	-14.2	-14.3	-14.3	-14.2	-8.00	MV

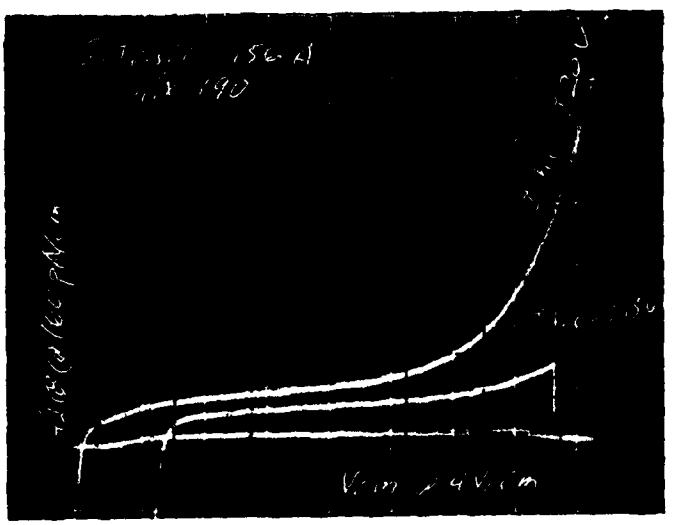
NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 3-7. Typical LF155A Op Amp Data Sheet



$+I_{iB}$ @ 160 pA/cm

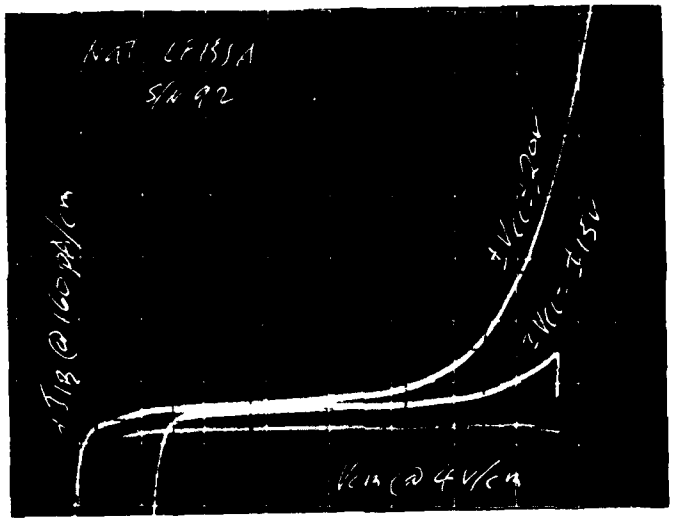
Vcm @ 4V/cm



$+I_{iB}$ @ 160 pA/cm

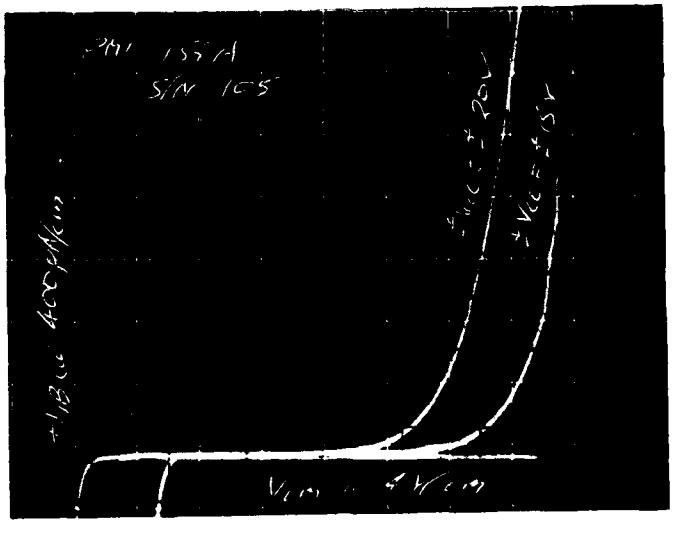
Vcm @ 4V/cm

Figure 3-8. Bi-FET Input Bias Current vs. Common Mode Voltage



$+I_{IB}$ @ 160 pA/cm

V_{cm} @ 4V/cm



$+I_{IB}$ @ 400 pA/cm

V_{cm} @ 4V/cm

Figure 3-9. Bi-FET Input Bias Current vs. Common Mode Voltage

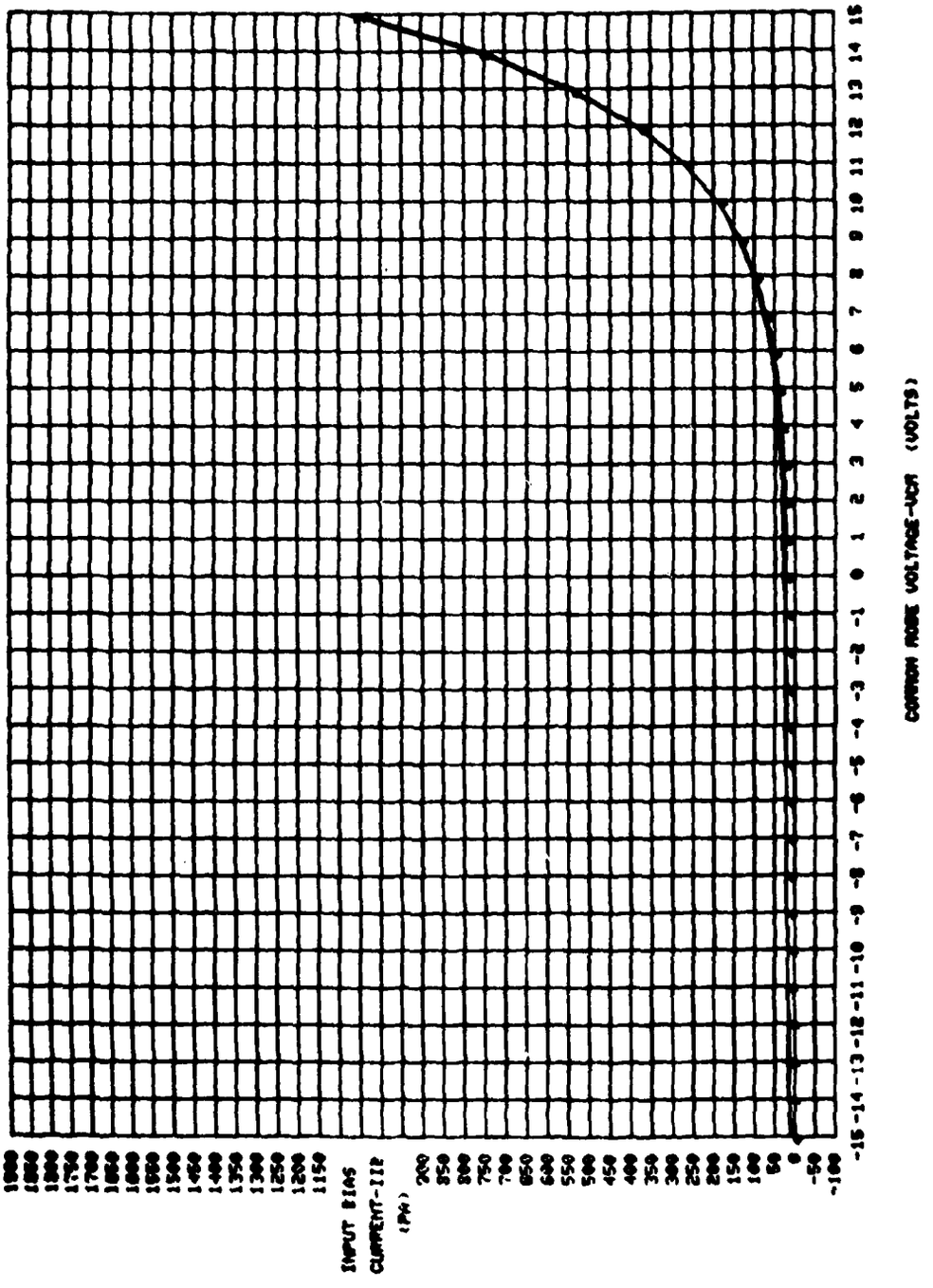
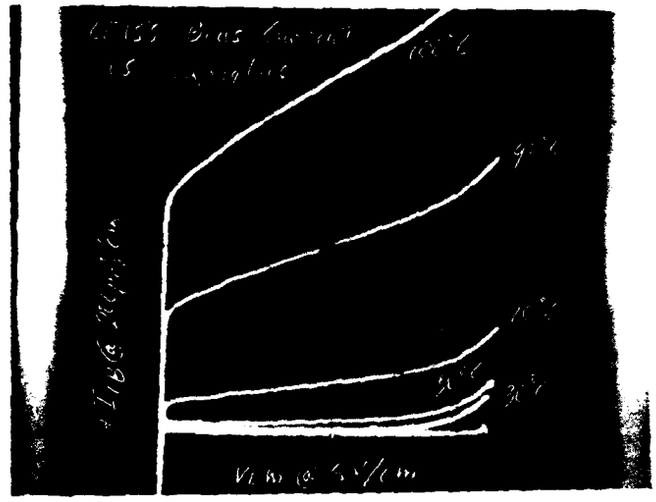


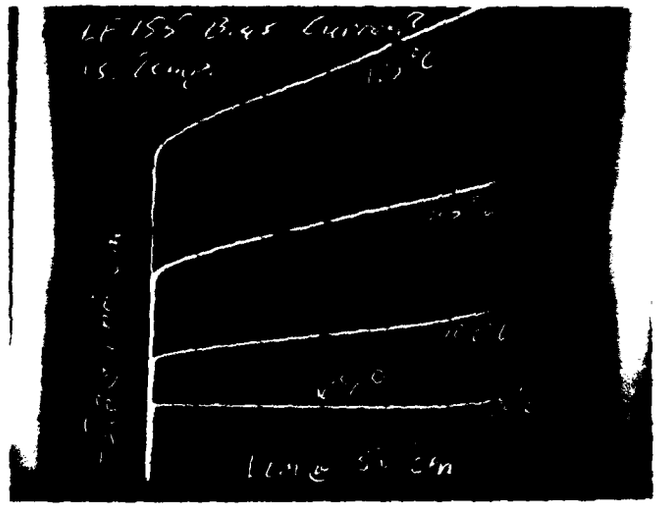
Figure 3-10. Bi-FET Input Bias Current vs. Common Mode Voltage



$+I_{iB}$ @ 200 pA/cm

$+I_{iB}$ = 1120 pA

@ 100°C, V_{cm} = 0V



$+I_{iB}$ @ 1 nA/cm

$+I_{iB}$ = 5.2 nA

@ 125°C, V_{cm} = 0V

V_{cm} @ 5V/cm

LF155 Bias Current from 30°C to 125°C

Figure 3-11. Bi-FET Input Bias Current vs. Temperature

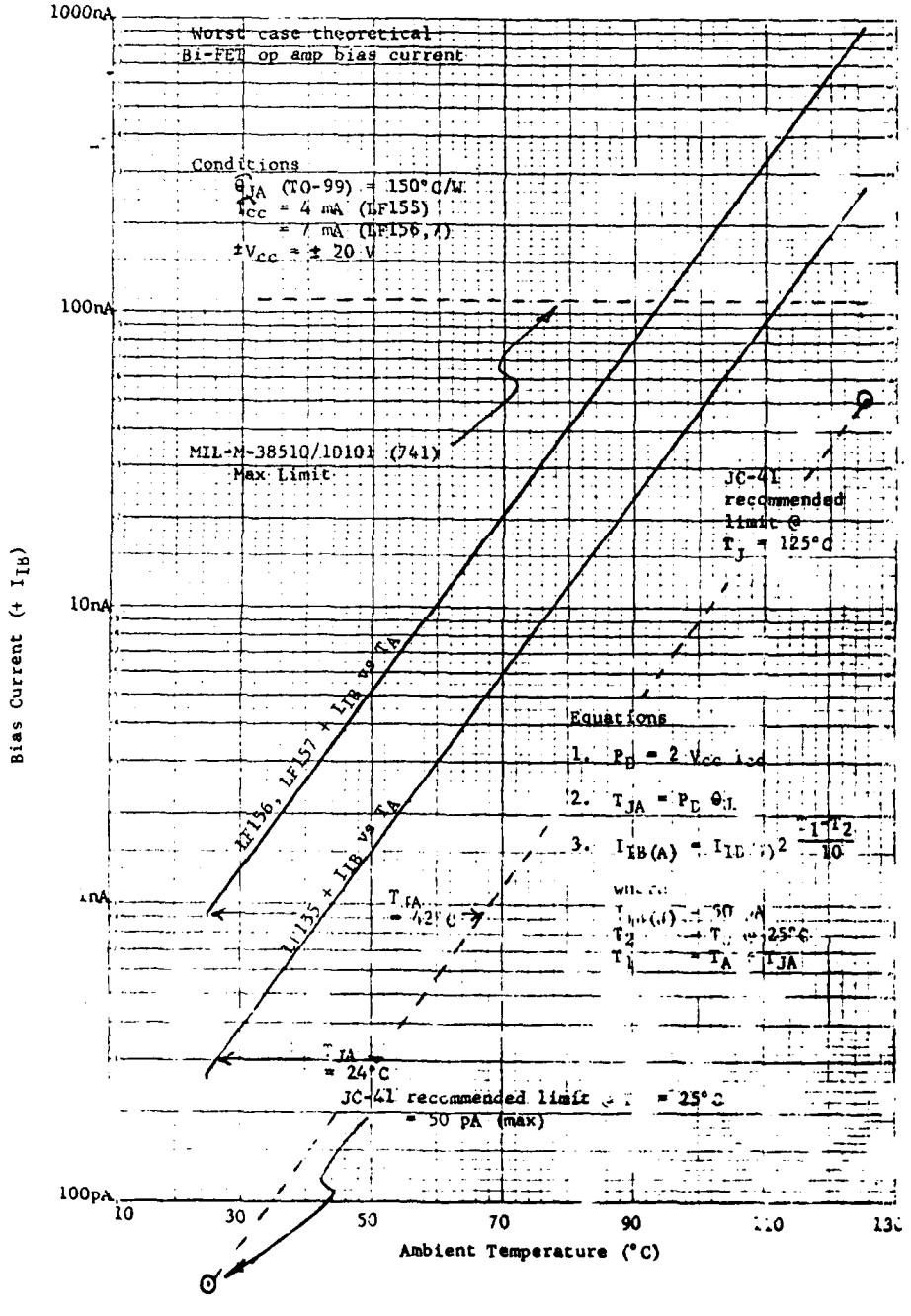


Figure 3-12. Worst Case Input Bias Current vs. Ambient Temperature.

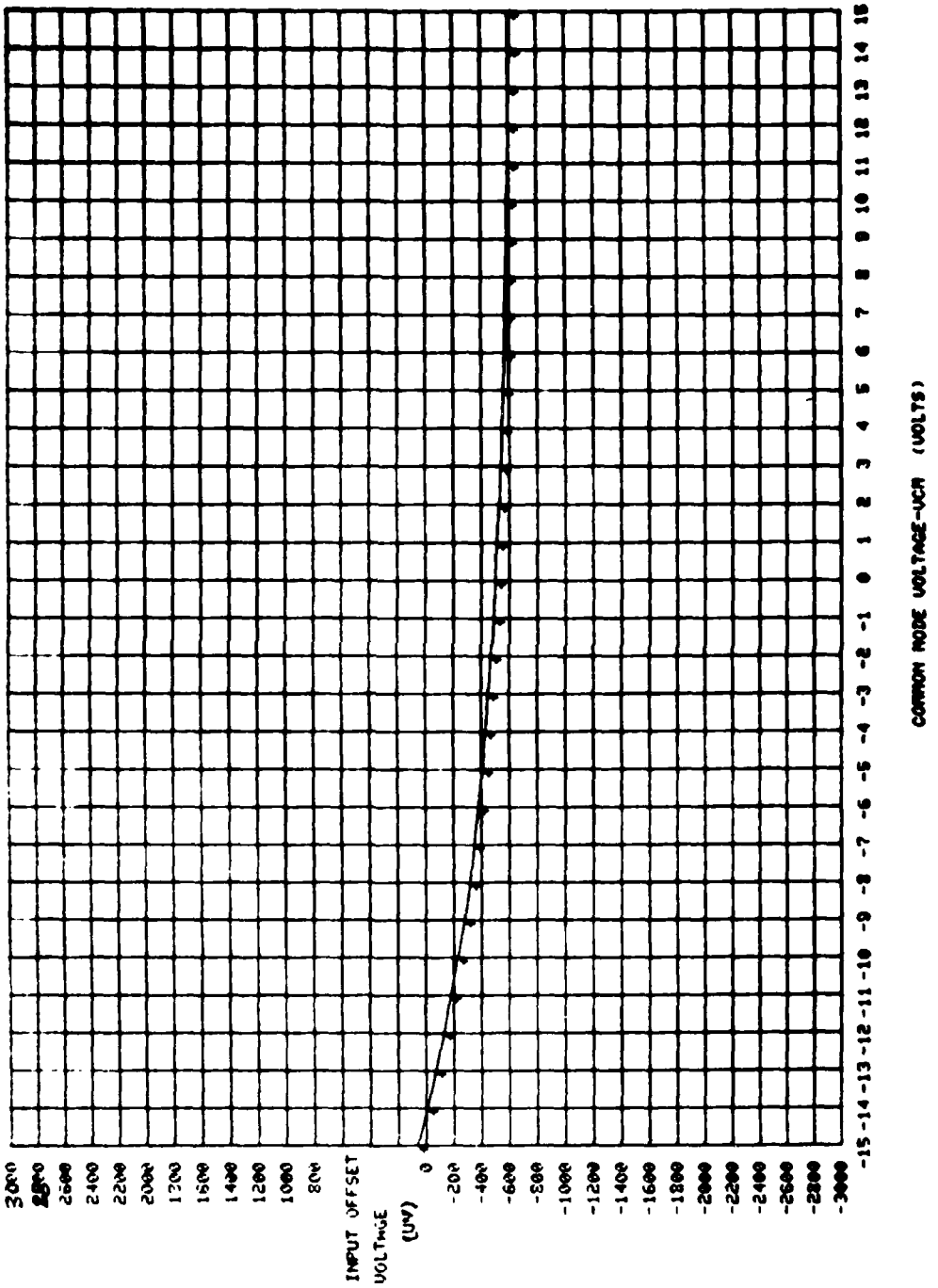


Figure 3-13. Offset Voltage vs Common Mode Voltage.

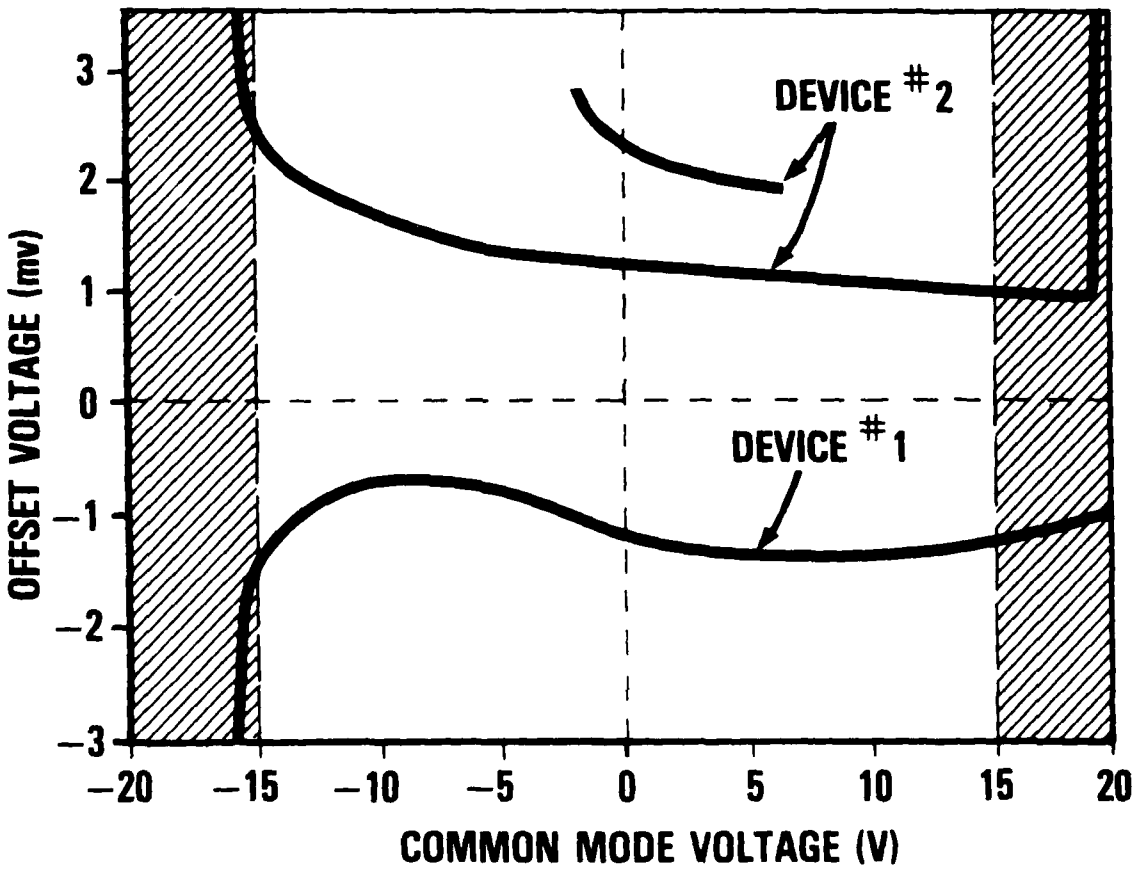
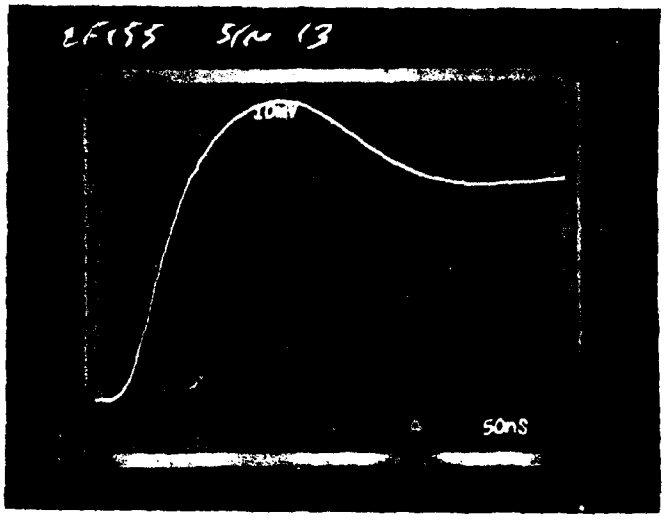
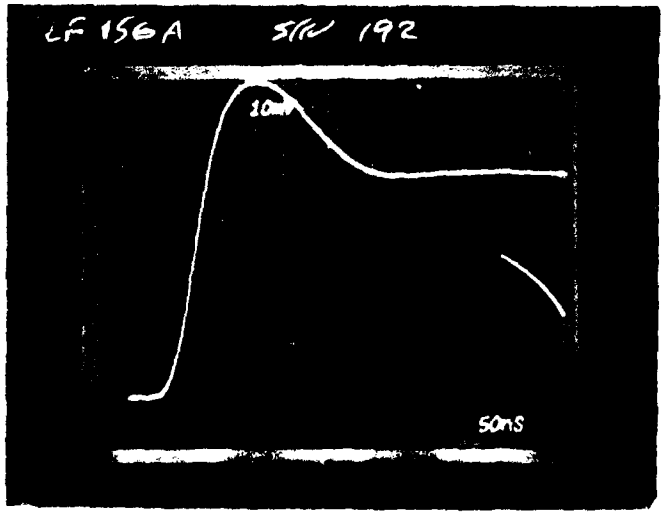


Figure 3-14. Offset Voltage vs Common Mode Voltage.

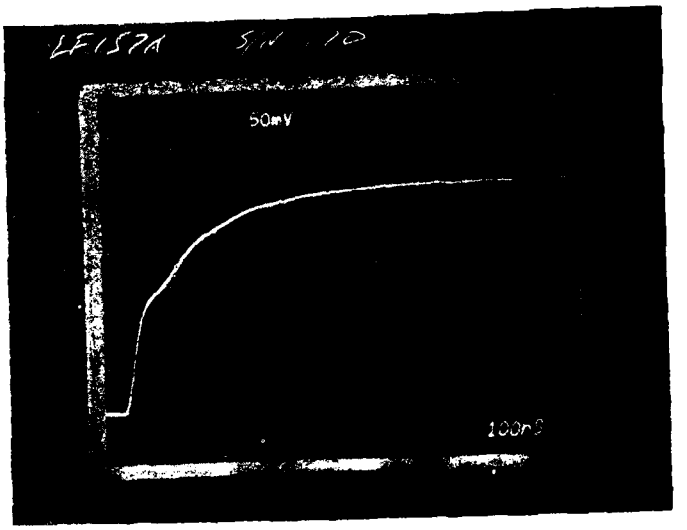


Typical LF155
TR (tr) = 60 ns
TR (OS) = 34%
GBW = 5.8 MHz
A_V = 1 V/V
TR (tr) x GBW = .348



Typical LF156A
TR (tr) = 40 ns
TR (OS) = 38%
GBW = 7 MHz
A_V = 1 V/V
TR (tr) x GBW = .350

Fig. 3-15. LF155 & LF156 Transient Response.



TR (tr) = 300 ns
TR (OS) = 0%
GBW = 1.1 MHz
A_V = 5 V/V
TR (tr) x GBW = .330

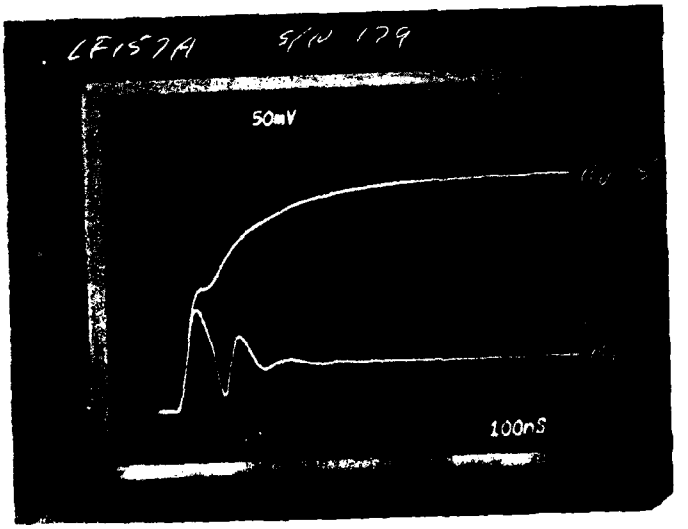
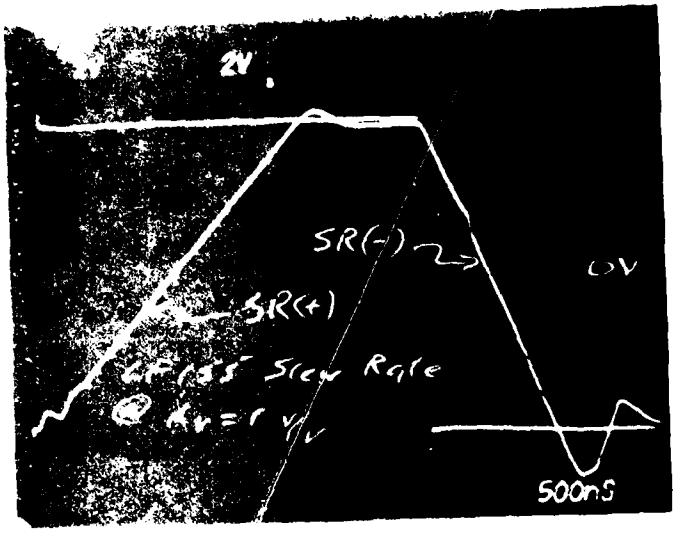


Fig. 3-16. LF157 Transient Response.



2 V/cm

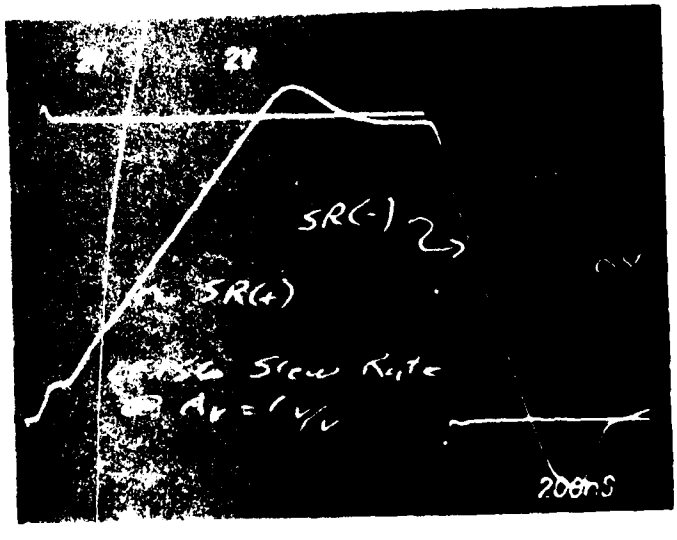
500 ns/cm

SR(+) = 4.7 V/us

SR(-) = 10 V/us

(SR = ΔV/ΔT @ V from -2.5 V to + 2.5 V)

LF155 slew rates @ AV = 1 V/V



2 V/cm

500 ns/cm

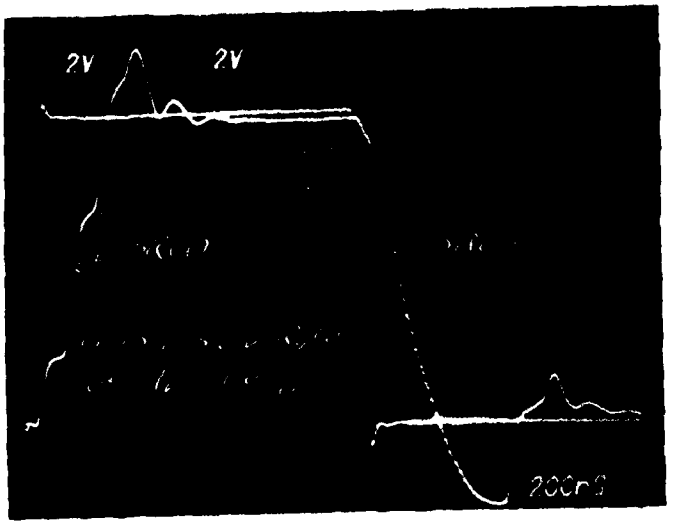
SR(+) = 14.3 V/us

SR(-) = 33.3 V/us

(SR = Δ V/ ΔT @ V from -2.5 V to + 2.5 V)

LF156 slew rates @ AV = 1V/V

Figure 3-17. LF155 and LF156 Slew Rates.

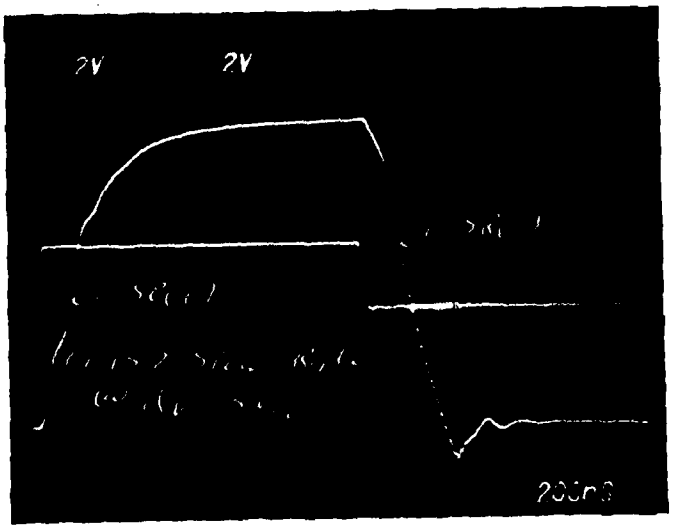


SR(+) = 40 V/us

SR(-) = 50 V/us

(SR = ΔV/ΔT @ V from - 2.5 V to + 2.5 V)

LF157 slew rates @ AV = 1 V/V



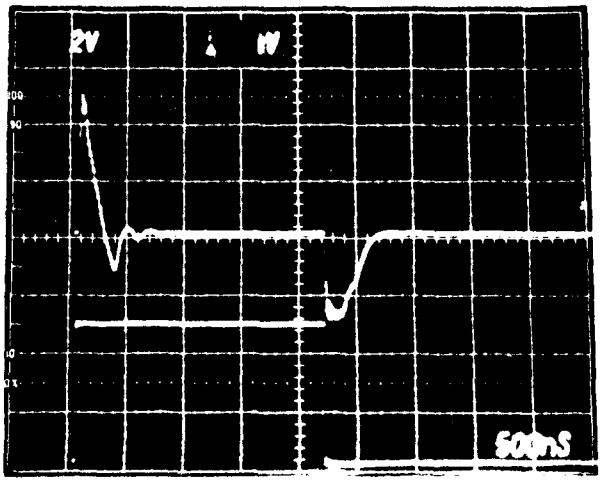
SR(+) = 33 V/us

SR(-) = 50 V/us

(SR = ΔV/ΔT @ V from - 2.5 V to + 2.5 V)

LF157 slew rates @ AV = 5 V/V

Figure 3-18. LF157 Slew Rate vs Gain.



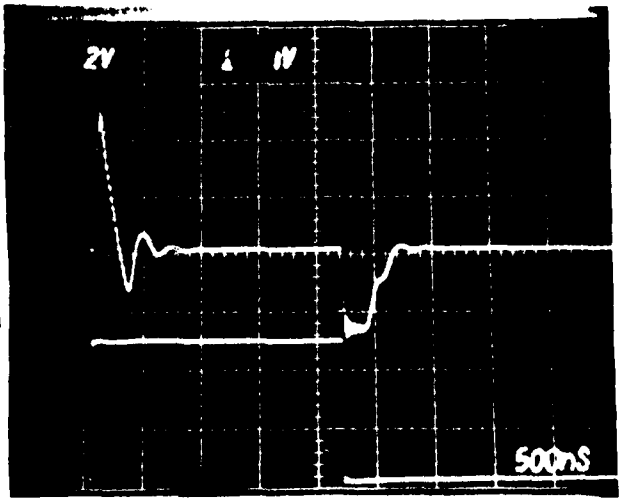
Null Error @ 20 mV/cm

V_{in} @ 2 V/cm

LF155A
S/N 112
t_s = 750 ns

AV = 1 V/V
V_{in} = 5 V

Time @ 500 ns/cm



Null Error @ 20 mV/cm

V_{in} @ 2 V/cm

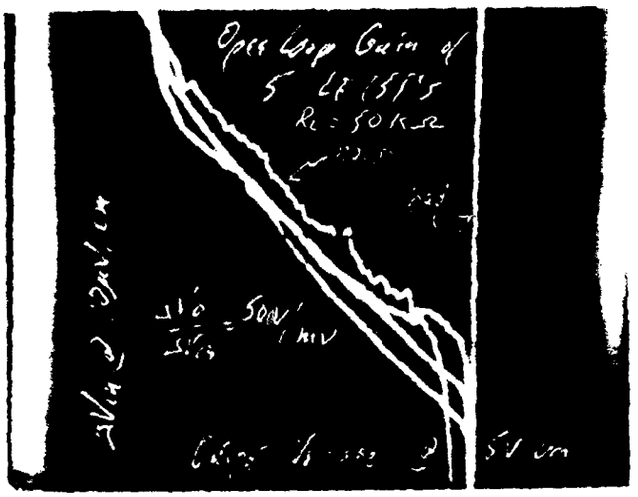
LF156

t_s = 750 ns

AV = 1 V/V
V_{in} = 5 V

Time @ 500 ns/cm

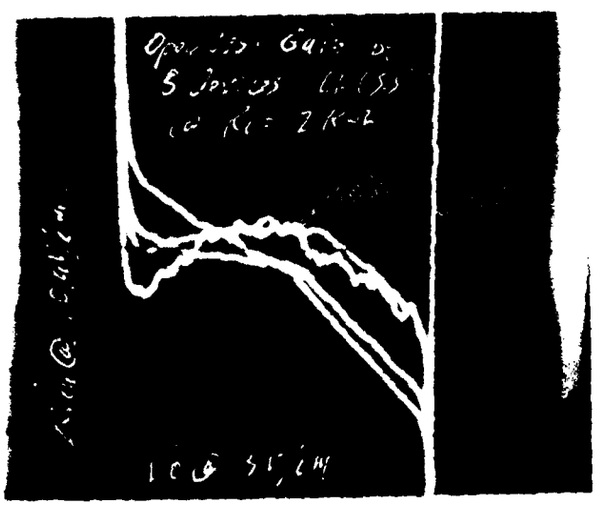
Figure 3-19. LF155 Series Bi-FET Settling Time.



V_{in} @ 10 uV/cm

V_o @ 5 V/cm

LF155 Open loop voltage gain A_{VS} (±) @ R_L = 50 KΩ

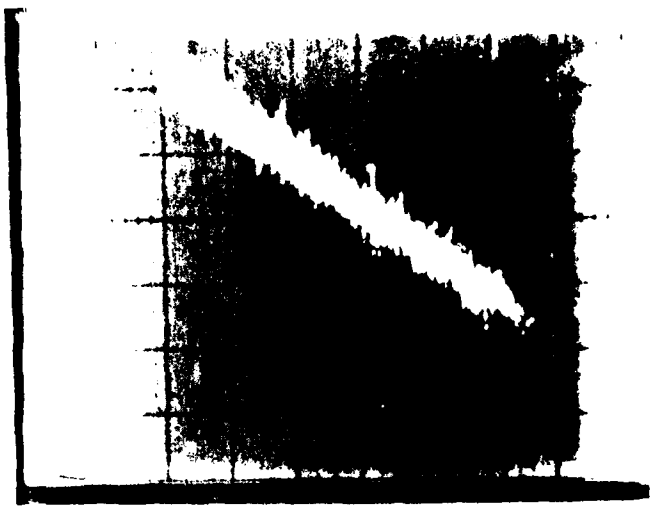


V_{in} @ 10 mV/cm

V_o @ 5 V/cm

LF155 Open loop voltage gain A_{VS} (±) @ R_L = 2 KΩ

Figure 3-20. Open Loop Voltage Gain vs Load.



ΔV_{in} @ 10 uV/cm

Vo @ 5V/cm

LF155
S/N 19
R_S = 50 Ω

NI(BB) = 10 uV_{pp}

= 1.67 uV_{rms}

* Note: Random noise has a Gaussian amplitude distribution such that the ratio of (peak to peak) over (rms) is 6 and will not be exceeded 99.37% of the time.

ΔV_{in} @ 10 uV/cm

Vo @ 5 V/cm

LF155
S/N 19
R_S = 50 KΩ

NI(PC) = 0 uV_{pp}

= 0 uV_{rms}

Figure 3-21. LF155 Series Bi-FET Noise Voltage.

STATISTICAL DATA FOR MIXED LOT FET OP AMP @ +25 DEGREES C 27 JUN 79 16:29:19

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN $\bar{X}$ *	SIGMA σ *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW 2/	LOW LIMIT	LOW REJ	LO-FM 3/ *	% FAIL HIGH 2/	HIGH LIMIT	HIGH REJ	HI-FM 3/ *	UNITS
VIO(-CM) AT 35V,-5V	-4.60	4.37	57A.M	2.08	62	95.2	100.	0.00	-5.00	-10.0	2.68	0.00	5.00	10.0	2.12	MV
VIO(+CM) AT 5V,-35V	-4.45	7.32	701.M	2.18	62	93.5	98.4	0.00	-5.00	-10.0	2.62	1.61	5.00	10.0	1.97	MV
VIO(0CM) AT 20V,-20V	-4.45	4.59	579.M	2.04	62	95.2	100.	0.00	-5.00	-10.0	2.74	0.00	5.00	10.0	2.17	MV
VIO(0CM) AT 5V,-5V	-4.37	4.40	588.M	2.09	62	95.2	100.	0.00	-5.00	-10.0	2.65	0.00	5.00	10.0	2.13	MV
IIO(-CM) AT 35V,-5V	-28.2	47.A	10.A	11.1	60	91.9	95.2	1.61	-20.0	-60.0	2.77	(17.)	20.0	60.0	A33.M	PA
IIO(+CM) AT 5V,-35V	-596.	412.	-A7.9	134.	61	93.5	93.5	(4.84)	-400.	-600.	2.33	1.61	400.	600.	3.64	PA
IIO(0CM) AT 20V,-20V	-37.7	81.2	-7.1A	10.9	60	91.9	95.2	(6.45)	-20.0	-60.0	1.1A	3.23	20.0	60.0	2.50	PA
IIO(+CM) AT 5V,-25V	-46.2	14.2	-20.5	11.1	60	A8.7	95.2	(56.5)	-20.0	-60.0	-41.2M	1.61	20.0	60.0	3.64	PA
+IIB(-CM) AT 35V,-5V	-23.5	134.	9.23	21.4	62	96.A	98.4	0.00	-100.	-100.	5.11	1.61	100.	200.	4.25	PA
+IIB(+CM) AT 5V,-35V	129.	2.93K	967.	717.	62	95.2	100.	0.00	-100.	-300.	1.49	0.00	3.50K	5.00K	3.54	PA
+IIB(0CM) AT 20V,-20V	1.10	97.9	27.4	19.9	60	91.9	93.5	0.00	-100.	-100.	6.00	3.23	100.	200.	3.64	PA
+IIB(+CM) AT 5V,-25V	16.9	2A8.	55.2	46.A	61	93.5	96.A	0.00	-100.	-100.	3.32	1.61	300.	400.	5.23	PA
-IIB(-CM) AT 35V,-5V	-20.7	36.5	-2.02	13.1	61	90.3	98.4	1.61	-100.	-100.	7.46	0.00	100.	200.	7.A3	PA
-IIB(+CM) AT 5V,-35V	159.	3.01K	1.07K	764.	62	98.4	100.	0.00	-100.	-300.	1.53	0.00	3.50K	5.00K	3.19	PA
-IIB(0CM) AT 20V,-20V	-40.1	172.	36.A	25.A	61	95.2	96.8	0.00	-100.	-100.	5.30	3.23	100.	200.	2.45	PA
-IIB(+CM) AT 5V,-25V	34.1	206.	73.8	38.5	61	91.9	95.2	0.00	-100.	-100.	4.57	1.61	300.	400.	5.88	PA
+PSRR AT 10V,-20V	100.	136.	118.	7.46	59	90.3	95.2	0.00	A5.0	60.0	4.38	0.00	2.00K	140.	252.	DB
-PSRR AT 20V,-10V	98.0	140.	117.	A.52	59	90.3	95.2	0.00	A5.0	60.0	3.71	0.00	2.00K	140.	221.	DB
CMR AT 20V,-20V	74.0	130.	102.	9.69	62	96.A	100.	1.61	A5.0	60.0	1.40	0.00	2.00K	140.	196.	DB
V-ADJ(+) AT 20V,-20V	13.0	13.1	13.1	2.04M	62	95.2	100.	0.00	A.00	0.00	2.48K	0.00	200.	20.0	91.7K	MV
V-ADJ(-) AT 20V,-20V	-13.3	-13.2	-13.2	2.04M	62	95.2	100.	0.00	-200.	-20.0	91.1K	0.00	-A.00	0.00	3.07K	MV
IOS(+) AT 15V,-15V	-27.9	-18.1	-22.1	1.A4	62	93.5	98.4	0.00	-50.0	-60.0	15.2	0.00	1.00K	0.00	556.	MA
IOS(-) AT 15V,-15V	2.50	28.6	22.7	3.13	62	98.4	98.4	0.00	-1.00K	0.00	327.	0.00	50.0	60.0	A.72	MA
ICC AT 15V,-15V	2.24	6.75	A.37	1.21	61	98.4	98.4	----	----	2.00	----	59.1 4/	A.00	8.00	-308.M	MA
+VOP AT RL=10K	14.4	14.5	14.4	38.5M	62	100.	100.	0.00	16.0	16.0	63.A	0.00	200.	20.0	A.71K	V
-VOP AT RL=10K	-14.7	-14.7	-14.5	152.M	62	96.A	98.4	0.00	-200.	-20.0	1.19K	0.00	-16.0	-16.0	16.A	V
+VOP AT RL=2K	14.1	14.3	14.2	A7.6M	62	100.	100.	0.00	15.0	15.0	66.7	0.00	200.	20.0	3.A2K	V
-VOP AT RL=2K	-17.A	-17.3	-17.6	114.M	61	96.A	98.4	0.00	-200.	-20.0	1.60K	1.61	-15.0	-15.0	22.A	V
AVS(+) AT RL=10K	375.	6.00K	1.A2K	1.07K	58	90.3	91.9	0.00	50.0	0.00	1.66	A.84	100.K	10.0K	92.0	V/MV
AVS(-) AT RL=10K	1.50K	10.0K	3.29K	1.72K	39	54.5	59.7	0.00	50.0	0.00	1.A8	29.0 5/	100.K	10.0K	56.2	V/MV
AVS(+) AT RL=2K	210.	A.29K	1.53K	918.	60	93.5	96.A	0.00	50.0	0.00	1.41	3.23	100.K	10.0K	107.	V/MV
AVS(-) AT RL=2K	1.0A	6.00K	930.	1.00K	60	A7.1	95.2	1.61	50.0	0.00	A7A.M	0.00	100.K	10.0K	98.A	V/MV
AVS AT 5V,-5V,RL=10K	38.1	1.00K	271.	19A.	57	85.5	A8.7	0.00	10.0	0.00	1.32	A.84	10.0K	1.00K	A9.1	V/MV
AVS AT 5V,-5V,RL=2K	80.0	A00.	A56.	286.	A6	74.2	74.2	0.00	10.0	0.00	1.56	16.1	10.0K	1.00K	33.3	V/MV
SR(+) AT 20V,-20V	A.20	11.A	7.50	1.A9	A3	67.7	69.A	0.00	2.00	2.00	2.90	30.6 5/	25.0	25.0	9.25	V/US
SR(-) AT 20V,-20V	A.13	25.0	17.9	5.0A	26	50.0	53.2	0.00	2.00	2.00	3.13	61.3	25.0	25.0	1.A0	V/US

NOTES: 1/ * Excludes population outside of low rej and high rej

2/ % fail values $\geq$ 5% are circled (○)

3/ Figure of merit definitions:

$$LO - FM = \frac{\bar{X} - \text{low limit}}{\sigma}$$

$$HI - FM = \frac{\text{High limit} - \bar{X}}{\sigma}$$

4/ The % fail for I_{CC} and SR on this table are not valid since all device types are compared to type 01 limits.

5/ There is no maximum fail limit for gain and slew rate.

Table 3-8. 25°C Statistical Summary For LF155 Series Devices.

STATISTICAL DATA FOR MIXED LOT FET OP AMP @ -55 DEGREES C 27 JUN 79 14:35:27

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN $\bar{X}$ *	SIGMA σ *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW 2/	LOW LIMIT	LOW REJ	LO-FM 3/ *	% FAIL HIGH 2/	HIGH LIMIT	HIGH REJ	HI-FM 3/ *	UNITS
VIO(-25°) AT 15V,-5V	-4.74	4.24	501.M	2.71	62	98.4	100.	0.00	-7.00	-10.0	2.76	0.00	7.00	10.0	2.39	MV
VIO(+25°) AT 5V,-15V	-4.37	5.68	522.M	2.41	61	95.2	98.4	0.00	-7.00	-10.0	3.12	1.61	7.00	10.0	2.68	MV
VIO(0C°) AT 20V,-20V	-4.59	4.11	493.M	2.56	62	98.4	100.	0.00	-7.00	-10.0	2.93	0.00	7.00	10.0	2.54	MV
VIO(0C°) AT 5V,-5V	-5.78	7.00	516.M	2.83	62	95.2	100.	0.00	-7.00	-10.0	2.66	1.61	7.00	10.0	2.29	MV
V-ADJ(+) AT 20V,-20V	13.0	13.1	13.1	2.56M	62	98.4	100.	0.00	8.00	0.00	1.97K	0.00	200.	20.0	73.0K	MV
V-ADJ(-) AT 20V,-20V	-14.3	-14.2	-14.2	2.56M	62	98.4	100.	0.00	-200.	-20.0	72.6K	0.00	-8.00	0.00	2.44K	MV
IOS(+) AT 15V,-15V	-35.1	-23.0	-28.8	2.49	62	95.2	100.	0.00	-50.0	-60.0	8.53	0.00	1.00K	0.00	414.	NA
IOS(-) AT 15V,-15V	2.90	36.4	20.4	4.11	62	98.4	98.4	0.00	-1.00K	0.00	251.	0.00	50.0	60.0	5.01	NA
ICC AT 15V,-15V	2.44	7.32	5.18	1.40	54	90.3	98.4	----	----	2.00	----	38.7 4/	6.00	8.00	589.M	NA
+VOP AT RL=10K	18.1	18.3	18.2	30.9M	62	93.5	100.	0.00	16.0	16.0	70.6	0.00	200.	20.0	5.89K	V
-VOP AT RL=10K	-18.4	-18.0	-18.3	80.3M	62	95.2	98.4	0.00	-200.	-20.0	2.26K	0.00	-16.0	-16.0	28.3	V
+VOP AT RL=2K	17.9	18.0	17.9	27.3M	62	90.3	100.	0.00	15.0	15.0	108.	0.00	200.	20.0	6.66K	V
-VOP AT RL=2K	-17.7	-17.3	-17.5	88.1M	61	96.8	98.4	0.00	-200.	-20.0	2.07K	1.61	-15.0	-15.0	28.3	V
AVS(+) AT RL=10K	273.	5.26K	1.72K	988.	51	80.4	80.4	0.00	25.0	0.00	1.75	0.00	105.K	10.0K	107.	V/MV
AVS(-) AT RL=10K	375.	10.0K	3.00K	1.75K	42	64.5	66.1	0.00	25.0	0.00	1.75	0.00	105.K	10.0K	58.8	V/MV
AVS(+) AT RL=2K	211.	4.29K	1.08K	949.	54	82.3	87.1	0.00	25.0	0.00	1.47	0.00	105.K	10.0K	105.	V/MV
AVS(-) AT RL=2K	1.01	7.50K	1.44K	1.52K	56	85.5	87.3	1.61	25.0	0.00	938.M	0.00	105.K	10.0K	68.3	V/MV
AVS AT 5V,-5V,RL=10K	27.6	400.	196.	118.	45	72.6	72.6	0.00	10.0	0.00	1.57	0.00	105.K	500.	887.	V/MV
AVS AT 5V,-5V,RL=2K	53.3	400.	258.	110.	34	54.8	54.8	0.00	10.0	0.00	2.25	0.00	105.K	500.	949.	V/MV
SR(+) AT 20V,-20V	8.15	14.9	9.00	2.78	43	67.7	69.4	0.00	1.00	0.00	2.88	19.4 5/	50.0	25.0	14.8	V/US
SR(-) AT 20V,-20V	9.71	25.0	16.8	4.87	16	30.6	46.8	0.00	1.00	0.00	3.24	33.9	50.0	25.0	6.82	V/US

NOTES: 1/ * Excludes population outside of low rej and high rej

2/ % fail values $\geq$ 5% are circled ◯.

3/ Figure of merit definitions:

$$LO - FM = \frac{\bar{X} - \text{low limit}}{\sigma}$$

$$HI - FM = \frac{\text{High limit} - \bar{X}}{\sigma}$$

4/ The % fail for I_{CC} and SR on this table are not valid since all device types are compared to type 01 limits.

5/ There is no maximum fail limit for gain and slew rate.

Table 3-9. -55°C Statistical Summary For LF155 Series Devices.

STATISTICAL DATA FOR MIXED LOT FET OP AMP @ +125 DEGREES C 27 JUN 79 16:39:49

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN $\bar{X}$ *	SIGMA σ *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW 2/	LOW LIMIT	LOW REJ	LO-FM 3/ *	% FAIL HIGH 2/	HIGH LIMIT	HIGH REJ	HI-FM 3/ *	UNITS
VIO(-CM) AT 35V,-5V	-4.59	7.48	940.M	2.36	62	93.5	100.	0.00	-7.00	-10.0	3.36	1.61	7.00	10.0	2.56	MV
VIO(+CM) AT 5V,-35V	-4.53	5.20	829.M	2.27	60	90.3	96.8	1.61	-7.00	-10.0	3.45	1.61	7.00	10.0	2.72	MV
VIO(OCM) AT 20V,-20V	-5.12	4.73	689.M	2.23	61	93.5	98.4	0.00	-7.00	-10.0	3.44	1.61	7.00	10.0	2.82	MV
VIO(OCM) AT 5V,- 5V	-4.72	8.14	844.M	2.26	62	95.2	98.4	0.00	-7.00	-10.0	3.48	1.61	7.00	10.0	2.72	MV
IIO(-CM) AT 35V,-5V	-36.1K	37.9K	2.34K	8.52K	61	91.9	95.2	1.61	-20.0K	-40.0K	2.62	0.84	20.0K	40.0K	2.07	PA
IIO(+CM) AT 5V,-35V	-39.6K	24.3K	149.	8.14K	59	88.7	90.3	(6.45)	-30.0K	-40.0K	3.69	1.61	30.0K	40.0K	3.65	PA
IIO(OCM) AT 20V,-20V	-32.4K	30.6K	1.00K	7.46K	61	93.5	93.5	1.61	-20.0K	-40.0K	2.82	0.84	20.0K	40.0K	2.54	PA
IIO(+CM) AT 5V,-25V	-31.2K	36.1K	176.	7.18K	60	91.9	93.5	1.61	-20.0K	-40.0K	2.81	0.84	20.0K	40.0K	2.76	PA
+IIB(-CM) AT 35V,-5V	2.01K	78.3K	20.8K	21.6K	59	90.3	96.8	0.00	-10.0K	-10.0K	1.43	(17.7)	50.0K	80.0K	1.35	PA
+IIB(+CM) AT 5V,-35V	-2.21	77.0K	21.1K	18.4K	48	72.6	75.8	0.00	-10.0K	-10.0K	1.69	(27.4)	60.0K	80.0K	2.12	PA
+IIB(OCM) AT 20V,-20V	3.04K	76.6K	22.4K	22.3K	55	80.6	90.3	0.00	-10.0K	-10.0K	1.45	(24.2)	50.0K	80.0K	1.24	PA
+IIB(+CM) AT 5V,-25V	3.10K	77.6K	20.4K	19.2K	56	83.9	90.3	0.00	-10.0K	-10.0K	1.59	(21.0)	50.0K	80.0K	1.54	PA
-IIB(-CM) AT 35V,-5V	2.30K	72.9K	19.1K	19.1K	60	91.9	96.8	0.00	-10.0K	-10.0K	1.52	(11.3)	50.0K	80.0K	1.62	PA
-IIB(+CM) AT 5V,-35V	6.45K	78.8K	24.4K	19.4K	51	75.8	82.3	0.00	-10.0K	-10.0K	1.77	(25.8)	60.0K	80.0K	1.83	PA
-IIB(OCM) AT 20V,-20V	3.66K	71.0K	21.8K	20.7K	56	82.3	90.3	0.00	-10.0K	-10.0K	1.54	(24.2)	50.0K	80.0K	1.37	PA
-IIB(+CM) AT 5V,-25V	3.76K	78.5K	22.3K	20.5K	58	88.7	95.2	0.00	-10.0K	-10.0K	1.57	(21.0)	50.0K	80.0K	1.35	PA
+PSRR AT 10V,-20V	84.0	146.	119.	9.79	41	93.5	96.8	1.61	85.0	50.0	3.47	0.00	2.00K	150.	192.	DB
-PSRR AT 20V,-10V	84.7	148.	119.	11.8	61	91.9	100.	3.23	85.0	50.0	2.90	0.00	2.00K	150.	159.	DB
CMR AT 20V,-20V	63.9	126.	97.8	11.8	62	91.9	100.	(4.84)	85.0	50.0	1.08	0.00	2.00K	150.	161.	DB
V-ADJ(+) AT 20V,-20V	13.0	13.1	13.1	2.81M	62	95.2	98.4	0.00	8.00	0.00	1.80K	0.00	200.	20.0	66.6K	MV
V-ADJ(-) AT 20V,-20V	-14.3	-14.2	-14.2	2.81M	62	95.2	98.4	0.00	-200.	-20.0	66.2K	0.00	-8.00	0.00	2.23K	MV
IOS(+) AT 15V,-15V	-18.1	-11.6	-13.7	1.21	62	95.2	98.4	0.00	-50.0	-60.0	30.2	0.00	1.00K	0.00	841.	MA
IOS(-) AT 15V,-15V	2.55	19.8	15.4	2.07	62	96.8	98.4	0.00	-1.00K	0.00	492.	0.00	50.0	60.0	16.8	MA
ICC AT 15V,-15V	2.43	6.96	3.91	1.13	58	95.2	100.	----	----	2.00	----	35.5 4/	4.00	7.00	80.1M	MA
+VOP AT RL=10K	18.4	18.9	18.7	91.1M	62	95.2	98.4	0.00	16.0	16.0	30.1	0.00	200.	20.0	1.99K	V
-VOP AT RL=10K	-19.0	-17.9	-18.7	265.M	62	96.8	98.4	0.00	-200.	-20.0	685.	0.00	-16.0	-16.0	10.2	V
+VOP AT RL=2K	17.8	18.5	18.2	221.M	62	98.4	100.	0.00	15.0	15.0	14.6	0.00	200.	20.0	822.	V
-VOP AT RL=2K	-17.8	-16.5	-17.2	277.M	61	93.5	98.4	0.00	-200.	-20.0	661.	1.61	-15.0	-15.0	7.89	V
AVS(+) AT RL=10K	65.2	5.00K	1.31K	1.11K	59	90.3	93.5	0.00	25.0	0.00	1.16	0.00	105.K	10.0K	93.5	V/MV
AVS(-) AT RL=10K	32.3	10.0K	2.05K	2.15K	51	77.4	79.0	0.00	25.0	0.00	943.M	0.00	105.K	10.0K	47.9	V/MV
AVS(+) AT RL=2K	48.4	8.33K	1.05K	1.42K	59	91.9	91.9	0.00	25.0	0.00	722.M	0.00	105.K	10.0K	73.4	V/MV
AVS(-) AT RL=2K	1.07	1.67K	308.	317.	62	95.2	95.2	1.61	25.0	0.00	893.M	0.00	105.K	10.0K	330.	V/MV
AVS AT 5V,-5V,RL=10K	3.92	800.	183.	198.	62	93.5	95.2	3.23	10.0	0.00	872.M	0.00	105.K	1.00K	530.	V/MV
AVS AT 5V,-5V,RL=2K	6.90	889.	292.	310.	53	85.5	85.5	1.61	10.0	0.00	910.M	0.00	105.K	1.00K	337.	V/MV
SR(+) AT 20V,-20V	4.27	9.43	6.52	1.31	43	67.7	69.4	0.00	1.00	0.00	4.21	11.3 5/	50.0	25.0	33.2	V/US
SR(-) AT 20V,-20V	7.63	22.7	16.9	3.57	41	64.5	69.4	0.00	1.00	0.00	4.45	27.4	50.0	25.0	9.26	V/US

NOTES:

1/ * Excludes population outside of low rej and high rej

2/ % fail values $\geq$ 5% are circled (○).

3/ Figure of merit definitions:

$$LO - FM = \frac{\bar{X} - \text{low limit}}{\sigma}$$

$$HI - FM = \frac{\text{High limit} - \bar{X}}{\sigma}$$

4/ The % fail for I_{CC} and SR on this table are not valid since all device types are compared to type 01 limits.

5/ There is no maximum fail limit for gain and slew rate.

Table 3-10. 125°C Statistical Summary For LF155 Series Devices.

STATISTICAL DATA FOR WAFER LOT FET OP AMP @ +25 DEGREES C 26 JUN 79 15:14:59

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN $\bar{X}$ *	SIGMA σ *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW 2/	LOW LIMIT	LOW REJ	LO-FM 3/ *	% FAIL HIGH 2/	HIGH LIMIT	HIGH REJ	HI-FM 3/ *	UNITS
VIO(-CM) AT 35V,-5V	-4.45	3.47	-21.4M	1.33	111	89.6	94.8	(10.1)	-2.00	-10.0	1.48	3.48	2.00	10.0	1.52	MV
VIO(+CM) AT 5V,-35V	-4.21	3.06	-64.8M	1.36	110	87.8	94.8	(12.7)	-2.00	-10.0	1.43	(6.96)	2.00	10.0	1.52	MV
VIO(0CM) AT 20V,-20V	-4.34	3.23	-72.1M	1.32	110	87.8	93.9	(11.9)	-2.00	-10.0	1.46	(6.96)	2.00	10.0	1.57	MV
VIO(0CM) AT 5V,-5V	-4.12	3.41	-45.3M	1.36	111	90.4	94.8	(9.57)	-2.00	-10.0	1.43	4.35	2.00	10.0	1.50	MV
IIO(-CM) AT 35V,-5V	-48.4	51.0	1.18	21.2	74	60.9	65.2	(23.0)	-20.0	-60.0	1.00	(35.7)	20.0	60.0	89.4M	PA
IIO(+CM) AT 5V,-35V	-557.	124.	-136.	151.	112	92.2	97.4	(9.57)	-400.	-600.	1.75	0.00	400.	600.	3.54	PA
IIO(0CM) AT 20V,-20V	-33.5	49.5	3.72	17.8	105	83.5	89.6	(10.1)	-20.0	-60.0	1.33	(2.86)	20.0	60.0	915.M	PA
IIO(+CM) AT 5V,-25V	-56.8	56.2	-2.07	23.0	103	80.0	88.7	(22.2)	-20.0	-60.0	766.M	(20.0)	20.0	60.0	943.M	PA
+IIB(-CM) AT 35V,-5V	-91.7	151.	13.1	57.1	82	67.8	87.0	(26.1)	-100.	-100.	1.98	(2.86)	100.	200.	1.52	PA
+IIB(+CM) AT 5V,-35V	-471.M	2.77K	1.77K	823.	115	95.7	100.	0.00	-100.	-300.	2.27	0.00	3.50K	5.00K	2.10	PA
+IIB(0CM) AT 20V,-20V	-94.1	197.	25.3	66.6	110	91.3	96.5	0.00	-100.	-100.	1.88	(3.48)	100.	200.	1.12	PA
+IIB(+CM) AT 5V,-25V	-454.M	372.	119.	54.7	112	89.6	96.5	0.00	-100.	-100.	0.00	3.48	300.	400.	3.32	PA
-IIB(-CM) AT 35V,-5V	-93.8	106.	-21.4	37.4	87	73.9	87.0	(23.5)	-100.	-100.	2.10	1.74	100.	200.	3.25	PA
-IIB(+CM) AT 5V,-35V	-9.62	3.11K	1.92K	914.	115	95.7	100.	0.00	-100.	-300.	2.21	0.00	3.50K	5.00K	1.72	PA
-IIB(0CM) AT 20V,-20V	-77.7	169.	21.5	58.9	115	95.7	98.3	0.00	-100.	-100.	2.21	(3.57)	100.	200.	1.43	PA
-IIB(+CM) AT 5V,-25V	-240.M	400.	120.	59.8	111	89.6	94.8	0.00	-100.	-100.	3.75	(5.22)	300.	400.	2.83	PA
+PSRR AT 10V,-20V	77.8	140.	118.	8.90	100	84.3	88.7	870.M	85.0	60.0	3.74	0.00	2.00K	140.	211.	DB
-PSRR AT 20V,-10V	77.7	137.	116.	8.59	106	86.1	91.3	870.M	85.0	60.0	3.60	0.00	2.00K	140.	218.	DB
CMR AT 20V,-20V	65.0	136.	100.	9.78	110	89.6	93.9	870.M	85.0	60.0	1.55	0.00	2.00K	140.	193.	DB
V-ADJ(+) AT 20V,-20V	226.M	13.1	12.9	1.20	114	98.3	98.3	1.74	8.00	0.00	4.11	0.00	200.	20.0	154.	MV
V-ADJ(-) AT 20V,-20V	-14.3	-11.8	-14.1	1.18	111	95.7	95.7	0.00	-200.	-20.0	158.	4.35	-9.00	0.00	5.21	MV
IOS(+) AT 15V,-15V	-28.3	0.00	-21.7	5.35	115	96.5	97.4	0.00	-50.0	-60.0	5.28	0.00	1.00K	0.00	191.	MA
IOS(-) AT 15V,-15V	10.8	24.9	17.5	3.06	115	97.4	100.	0.00	-1.00K	0.00	333.	0.00	50.0	60.0	11.6	MA
ICC AT 15V,-15V	2.78	6.45	4.16	1.28	112	99.3	100.	----	----	2.00	----	00.9 4/	4.00	8.00	-125.M	MA
+VOP AT RL=10K	-14.3	18.5	18.4	57.84	111	96.1	96.5	3.48	16.0	16.0	41.1	0.00	200.	20.0	3.14K	V
-VOP AT RL=10K	-18.7	-18.4	-18.5	70.04	114	97.4	99.1	0.00	-200.	-20.0	2.59K	870.M	-16.0	-16.0	36.1	V
+VOP AT RL=2K	17.2	18.1	17.9	213.4	111	91.3	93.0	3.48	15.0	15.0	13.7	0.00	200.	20.0	457.	V
-VOP AT RL=2K	-18.0	-16.5	-17.5	348.M	114	93.0	99.1	0.00	-200.	-20.0	524.	870.M	-15.0	-15.0	7.25	V
AVS(+) AT RL=10K	300.	10.0K	2.44K	1.86K	91	75.7	78.3	0.00	50.0	0.00	1.39	7.83	100.K	10.0K	52.3	V/MV
AVS(-) AT RL=10K	652.	10.0K	3.27K	2.06K	84	67.8	69.6	0.00	50.0	0.00	1.56	20.0 5/	100.K	10.0K	47.0	V/MV
AVS(+) AT RL=2K	158.	10.0K	2.64K	2.26K	103	82.6	87.0	0.00	50.0	0.00	1.15	5.22	100.K	10.0K	43.1	V/MV
AVS(-) AT RL=2K	273.	7.50K	1.22K	1.17K	109	92.2	93.0	0.00	50.0	0.00	1.00	4.35	100.K	10.0K	45.3	V/MV
AVS AT 5V,-5V,RL=10K	30.2	1.00K	233.	217.	105	83.5	90.4	0.00	10.0	0.00	1.03	5.22	10.0K	1.00K	45.0	V/MV
AVS AT 5V,-5V,RL=2K	24.7	920.	293.	259.	102	87.0	89.6	0.00	10.0	0.00	1.09	6.09	10.0K	1.00K	37.5	V/MV
SR(+) AT 20V,-20V	5.00	22.7	12.9	4.43	92	74.8	80.0	0.00	3.00	2.00	2.23	20.0 5/	25.0	25.0	2.71	V/US
SR(-) AT 20V,-20V	10.4	20.8	19.4	3.52	32	59.1	55.7	0.00	3.00	2.00	4.66	72.2	25.0	25.0	1.59	V/US

NOTES: 1/ * Excludes population outside of low rej and high rej

2/ % fail values $\geq$ 5% are circled (○).

3/ Figure of merit definitions:

$$\text{LO - FM} = \frac{\bar{X} - \text{low limit}}{\sigma}$$

$$\text{HI - FM} = \frac{\text{High limit} - \bar{X}}{\sigma}$$

4/ The % fail for I_{CC} and SR on this table are not valid since all device types are compared to type 01 limits.

5/ There is no maximum fail limit for gain and slew rate.

Table 3-11. 25°C Statistical Summary For LF155A Series Devices.

STATISTICAL DATA FOR MIXED LOT FET OP AMP @ -55 DEGREES C 26 JUN 79 15:22:19

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN $\bar{X}$ *	SIGMA σ *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW 2/	LOW LIMIT	LOW REJ	LO-FM 3/ *	% FAIL HIGH 2/	HIGH LIMIT	HIGH REJ	HI-FM 3/ *	UNITS
VIO(+CM) AT 35V,-5V	-7.48	5.20	-1.24	2.17	109	87.8	94.8	(28.7)	-2.50	-10.0	578.M	(5.22)	2.50	10.0	1.72	MV
VIO(+CM) AT 5V,-35V	-6.23	4.69	-832.M	1.85	110	87.8	95.7	(18.1)	-2.50	-10.0	902.M	(5.22)	2.50	10.0	1.80	MV
VIO(0CM) AT 20V,-20V	-6.63	4.88	-1.21	2.12	110	88.7	95.7	(25.7)	-2.50	-10.0	606.M	(5.22)	2.50	10.0	1.75	MV
VIO(0CM) AT 5V,-5V	-7.46	9.26	+300.M	2.13	111	88.7	94.8	(13.9)	-2.50	-10.0	1.03	(6.09)	2.50	10.0	1.32	MV
V-ADJ(+) AT 20V,-20V	1.40	13.1	12.9	1.09	114	98.3	98.3	1.74	8.00	0.00	4.53	0.00	200.	20.0	171.	MV
V-ADJ(-) AT 20V,-20V	-14.3	-1.70	-14.1	1.19	111	95.7	95.7	0.00	-200.	-20.0	154.	4.35	-8.00	0.00	5.15	MV
IOS(+) AT 15V,-15V	-37.0	0.00	-28.2	6.95	115	96.5	97.4	0.00	-50.0	-60.0	3.14	0.00	1.00K	0.00	148.	NA
IOS(-) AT 15V,-15V	13.3	33.1	21.7	4.85	115	98.3	100.	0.00	-1.00K	0.00	211.	0.00	50.0	60.0	5.83	NA
ICC AT 15V,-15V	2.59	7.51	4.69	1.20	82	68.7	77.4	----	----	2.00	----	38.8 4/	4.00	8.00	1.09	MA
+VOP AT RL=10K	14.0	14.2	14.1	36.7M	111	94.8	95.7	3.48	14.0	14.0	57.7	0.00	200.	20.0	4.96K	V
-VOP AT RL=10K	-14.8	-14.8	-14.2	366.M	113	87.0	97.4	0.00	-200.	-20.0	496.	1.74	-16.0	-16.0	5.95	V
+VOP AT RL=2K	17.5	18.0	17.8	110.M	111	95.7	96.5	3.48	15.0	15.0	25.0	0.00	200.	20.0	1.65K	V
-VOP AT RL=2K	-17.7	-16.6	-17.4	194.M	114	97.4	98.3	0.00	-200.	-20.0	940.	870.M	-15.0	-15.0	12.2	V
AVS(+) AT RL=10K	4.40	10.0K	1.37K	1.61K	103	85.2	88.7	(22.6)	25.0	0.00	837.M	0.00	105.K	10.0K	64.3	V/MV
AVS(-) AT RL=10K	34.7	10.0K	1.66K	2.08K	92	74.8	79.1	0.00	25.0	0.00	788.M	0.00	105.K	10.0K	49.8	V/MV
AVS(+) AT RL=2K	1.86	10.0K	1.33K	1.72K	105	87.0	88.7	(24.7)	25.0	0.00	760.M	0.00	105.K	10.0K	60.4	V/MV
AVS(-) AT RL=2K	3.11	6.00K	736.	1.07K	109	87.0	93.0	(24.5)	25.0	0.00	662.M	0.00	105.K	10.0K	97.0	V/MV
AVS AT 5V,-5V,RL=10K	545.M	444.	172.	130.	84	73.9	75.7	2.61	10.0	0.00	1.24	0.00	105.K	500.	804.	V/MV
AVS AT 5V,-5V,RL=2K	8.66	471.	171.	129.	74	63.5	64.3	870.M	10.0	0.00	1.25	0.00	105.K	500.	811.	V/MV
SR(+) AT 20V,-20V	419.M	25.0	15.5	5.44	93	77.4	92.2	1.74	1.50	0.00	2.57	4.09 5/	50.0	25.0	6.36	V/US
SR(-) AT 20V,-20V	11.5	25.0	21.3	3.73	29	50.4	61.7	0.00	1.50	0.00	5.31	17.4	50.0	25.0	7.70	V/US

NOTES:

1/ * Excludes population outside of low rej and high rej

2/ % fail values $\geq$ 5% are circled (○).

3/ Figure of merit definitions:

$$LO - FM = \frac{\bar{X} - \text{low limit}}{\sigma}$$

$$HI - FM = \frac{\text{High limit} - \bar{X}}{\sigma}$$

4/ The % fail for I_{CC} and SR on this table are not valid since all device types are compared to type 01 limits.

5/ There is no maximum fail limit for gain and slew rate.

Table 3.12 -55°C Statistical Summary For LF155A Series Devices.

STATISTICAL DATA FOR MIXED LOT FET OP AMP @ +125 DEGREES C 25 JUN 79 09:41:03

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN $\bar{X}$ *	SIGMA σ *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW 2/	LOW LIMIT	LOW REJ	LO-FM 3/ *	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM 3/ *	UNITS
VIO(+CM) AT 35V,-5V	-4.44	2.97	48.4M	1.31	102	92.2	99.0	(5.88)	-2.50	-10.0	1.94	2.94	2.50	10.0	1.87	MV
VIO(+CM) AT 5V,-35V	-3.94	6.34	59.4M	1.50	102	94.1	99.0	3.90	-2.50	-10.0	1.70	4.90	2.50	10.0	1.62	MV
VIO(0CM) AT 20V,-20V	-4.43	3.60	-638.M	1.36	102	92.2	99.0	3.90	-2.50	-10.0	1.84	3.92	2.50	10.0	1.84	MV
VIO(0CM) AT 5V,- 5V	-4.10	3.05	-25.4M	1.33	102	92.2	99.0	(5.88)	-2.50	-10.0	1.86	2.94	2.50	10.0	1.90	MV
IIO(+CM) AT 35V,-5V	-1.96K	19.3K	830.	2.44K	102	98.0	98.0	0.00	-20.0K	-40.0K	8.54	0.00	20.0K	40.0K	7.85	PA
IIO(+CM) AT 5V,-35V	-2.17K	18.4K	830.	2.31K	102	98.0	98.0	0.00	-20.0K	-40.0K	13.3	0.00	20.0K	40.0K	12.6	PA
IIO(0CM) AT 20V,-20V	-5.24K	14.7K	505.	1.77K	102	97.1	98.0	0.00	-20.0K	-40.0K	11.6	0.00	20.0K	40.0K	11.0	PA
IIO(+CM) AT 5V,-25V	-1.35K	16.1K	529.	1.78K	102	98.0	99.0	0.00	-20.0K	-40.0K	11.5	0.00	20.0K	40.0K	10.9	PA
+IIB(-CM) AT 35V,-5V	-258.	48.4K	6.08K	7.92K	102	94.1	99.0	0.00	-10.0K	-10.0K	2.02	0.00	50.0K	80.0K	5.55	PA
+IIB(+CM) AT 5V,-35V	-58.2	61.9K	13.4K	11.7K	101	91.2	98.0	0.00	-10.0K	-10.0K	2.01	1.96	40.0K	80.0K	4.00	PA
+IIB(0CM) AT 20V,-20V	-54.8	72.7K	8.44K	10.7K	102	94.1	98.0	0.00	-10.0K	-10.0K	1.74	980.M	50.0K	80.0K	3.86	PA
+IIB(+CM) AT 5V,-25V	-51.7	71.9K	8.84K	10.5K	102	95.1	98.0	0.00	-10.0K	-10.0K	1.80	980.M	50.0K	80.0K	3.93	PA
-IIB(-CM) AT 35V,-5V	-805.	43.4K	5.21K	7.16K	102	95.1	99.0	0.00	-10.0K	-10.0K	2.12	0.00	50.0K	80.0K	6.26	PA
-IIB(+CM) AT 5V,-35V	29.2	56.9K	12.7K	11.4K	101	92.2	97.1	0.00	-10.0K	-10.0K	1.98	980.M	40.0K	80.0K	4.14	PA
-IIB(0CM) AT 20V,-20V	-217.	69.0K	8.15K	10.4K	102	95.1	99.0	0.00	-10.0K	-10.0K	1.74	980.M	50.0K	80.0K	4.01	PA
-IIB(+CM) AT 5V,-25V	21.2	68.4K	8.31K	10.1K	102	95.1	99.0	0.00	-10.0K	-10.0K	1.82	980.M	50.0K	80.0K	4.14	PA
+PSRR AT 10V,-20V	76.9	147.	122.	9.94	101	95.1	98.0	980.M	85.0	50.0	3.74	0.00	2.00K	150.	189.	DB
-PSRR AT 20V,-10V	76.9	148.	119.	10.5	101	92.2	98.0	980.M	85.0	50.0	3.23	0.00	2.00K	150.	179.	DB
CMR AT 20V,-20V	76.5	126.	99.3	8.82	102	94.1	99.0	980.M	85.0	50.0	1.62	0.00	2.00K	150.	215.	DB
V-ADJ(+) AT 20V,-20V	10.7	13.1	13.0	317.M	101	96.1	96.1	980.M	8.00	0.00	15.7	0.00	200.	20.0	590.	MV
V-ADJ(-) AT 20V,-20V	-14.3	-9.65	-14.0	667.M	100	94.1	96.1	0.00	-200.	-20.0	279.	1.96	-8.00	0.00	9.05	MV
IOS(+) AT 15V,-15V	-20.8	0.00	-14.7	3.43	102	98.0	99.0	0.00	-50.0	-60.0	10.3	0.00	1.00K	0.00	296.	MA
IOS(-) AT 15V,-15V	2.35	18.0	13.6	2.56	102	98.0	99.0	0.00	-1.00K	0.00	395.	0.00	50.0	60.0	14.2	MA
ICC AT 15V,-15V	2.09	6.16	3.76	1.14	100	97.1	99.0	----	----	2.00	----	3A.2 4/	4.00	7.00	209.M	MA
+VOP AT RL=10K	18.1	18.8	18.6	122.M	101	94.1	95.1	980.M	16.0	16.0	21.3	0.00	200.	20.0	1.88K	V
-VOP AT RL=10K	-19.0	-18.6	-18.8	83.8M	101	96.1	99.0	0.00	-200.	-20.0	2.16K	980.M	-16.0	-16.0	33.3	V
+VOP AT RL=2K	15.7	18.8	17.8	584.M	101	98.0	98.0	980.M	15.0	15.0	4.82	0.00	200.	20.0	312.	V
-VOP AT RL=2K	-19.2	-15.4	-17.4	943.M	101	98.0	99.0	0.00	-200.	-20.0	194.	980.M	-15.0	-15.0	2.57	V
AVS(+) AT RL=10K	214.	7.50K	1.75K	1.67K	88	80.4	83.3	0.00	25.0	0.00	1.04	0.00	105.K	10.0K	61.9	V/MV
AVS(-) AT RL=10K	1.31	10.0K	1.93K	1.80K	93	86.3	87.3	980.M	25.0	0.00	1.06	0.00	105.K	10.0K	57.2	V/MV
AVS(+) AT RL=2K	17.2	7.50K	1.61K	1.57K	97	88.2	93.1	980.M	25.0	0.00	1.01	0.00	105.K	10.0K	65.7	V/MV
AVS(-) AT RL=2K	551.M	10.0K	1.60K	1.74K	97	90.2	93.1	980.M	25.0	0.00	907.M	0.00	105.K	10.0K	59.8	V/MV
AVS AT 5V,-5V,RL=10K	13.3	800.	111.	136.	101	94.1	97.1	0.00	10.0	0.00	740.M	0.00	105.K	1.00K	769.	V/MV
AVS AT 5V,-5V,RL=2K	12.2	889.	109.	144.	100	92.2	95.1	0.00	10.0	0.00	690.M	0.00	105.K	1.00K	730.	V/MV
SR(+) AT 20V,-20V	5.68	24.4	10.7	3.52	66	63.7	83.7	0.00	1.50	0.00	2.61	18.6 5/	50.0	25.0	11.2	V/US
SR(-) AT 20V,-20V	8.62	25.0	19.9	3.68	56	60.8	82.7	0.00	1.50	0.00	5.01	18.6	50.0	25.0	8.16	V/US

NOTES: 1/ * Excludes population outside of low rej and high rej

2/ % fail values $\geq$ 5% are circled (○).

3/ Figure of merit definitions:

$$\text{LO - FM} = \frac{\bar{X} - \text{low limit}}{\sigma}$$

$$\text{HI - FM} = \frac{\text{High limit} - \bar{X}}{\sigma}$$

4/ The % fail for I_{CC} and SR on this table are not valid since all device types are compared to type 01 limits.

5/ There is no maximum fail limit for gain and slew rate.

Table 3-13. 125°C Statistical Summary For LF155A Series Devices.

A_V = 1 V/V

Parameter Symbol	Conditions AV = 1 V/V	VENDOR CODE A Serial No. 12	13	14	15	16	VENDOR CODE B* Serial No. 90	91	92	93	94	VENDOR CODE B Serial No. 83	86	87	88	89	UNITS
TR(tr)	VO = .05V	44	50	55	53	47	49	45	41	49	43	48	50	46	45	46	ns
	VO = .5V	48	58	76	64	63	52	48	42	56	48						
TR(os)	VO = .05V	43	42	38	40	47	38	35	35	33	36	36	36	38	36	44	%
	VO = .5V	46	38	30	34	36	33	31	34	29	32						
SR (+)	VO = -5V																
	TO + 5V	7.5	5.0	11.5	12.0	11.0	9.0	8.5	11.5	7.0	8.0	8.0	7.5	9.0	10	8.0	V/us
SR (-)	VO = -5V																
	TO + 5V	18.0	12.0	9.0	12.0	9.5	17.0	17.5	18.0	13.5	15.5	17.5	13.5	19.0	20.5	19.0	V/us
	VO = -5V																
ts	TO + 5V	700	850	1000	900	1200	800	750	800	900	800	1300	1250	1000	1100	1200	ns

* LF155A

Table 3-14. LF 155 Dynamic Data @ 25°C.

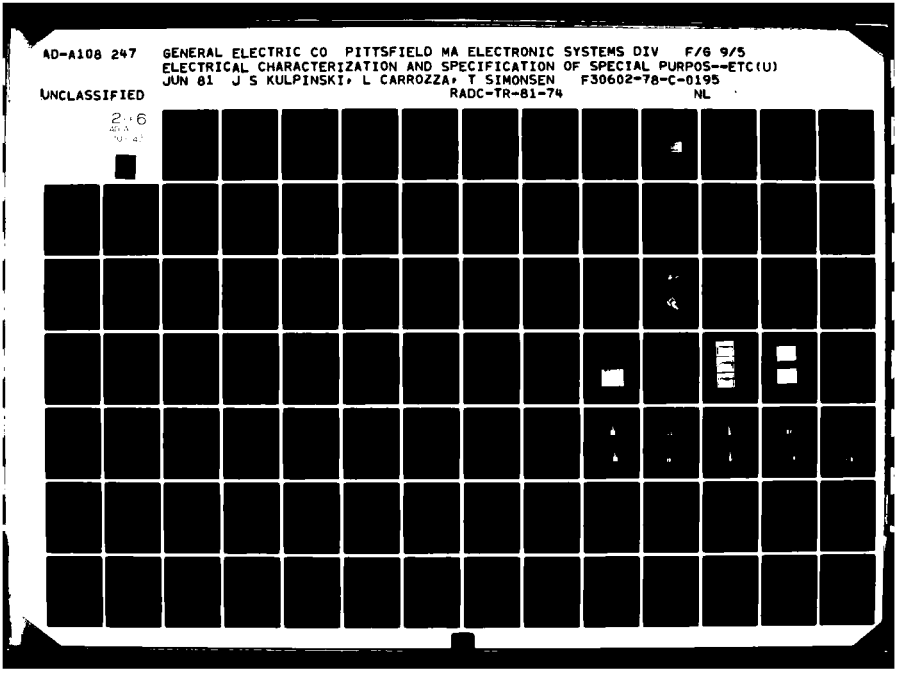
A_V = 1 V/V

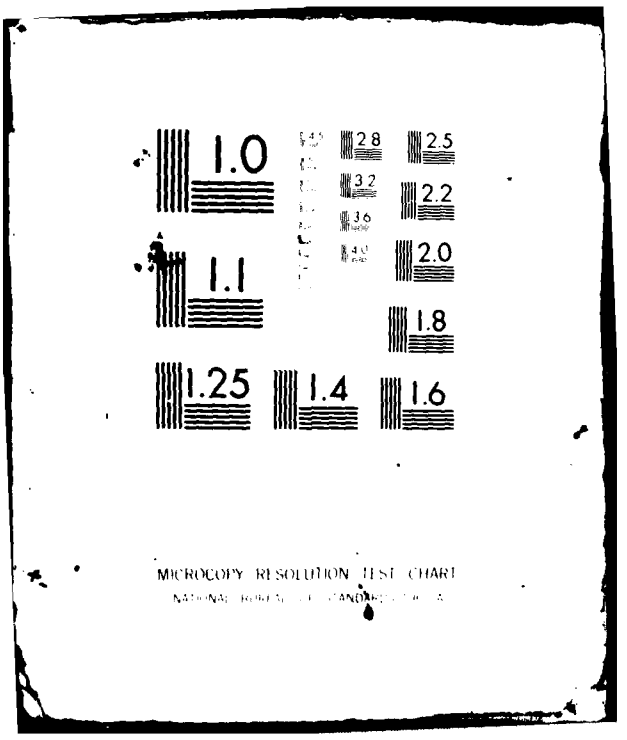
Parameter Symbol	Conditions A_V = 1 V/V	VENDOR CODE B* Serial No. 130	131	132	133	134	VENDOR CODE A Serial No. 34	35	36	37	38	VENDOR CODE E* Serial No. 149	150	151	152	153	UNITS
TR (tr)	VO = .05V	28	28	35	39	35	45	44	42	45	42	33	39	38	34	30	ns
	VO = .5V	33	38	37	41	35	50	47	44	46	44	40	32	31	41	34	
TR (os)	VO = .05V	47	42	45	42	44	46	48	44	46	48	42	46	46	44	44	%
	VO = .5V	39	37	38	36	38	36	380	390	36	390	36	40	390	36	37	
SR (+)	VO = -5V																
	TO + 5V	17.5	15.0	17.0	10.0	16.0	9.5	9.5	10.5	10.0	10.5	16.0	24.0	25.0	14.0	18.0	V/us
SR (-)	VO = -5V																
	TO + 5V	34.0	33.0	31.0	23.0	30.0	20.0	20.0	19.0	18.5	19.0	26.0	29.5	29.0	20.5	28.0	V/us
ts	VO = -5V																
	TO + 5V	900	950	900	1100	900	1100	1200	1250	1200	1300	1100	1000	1100	1300	1100	ns

* LF156A

Table 3-15. LF156 Dynamic Data @ 25°C.

AD-A108 247 GENERAL ELECTRIC CO PITTSFIELD MA ELECTRONIC SYSTEMS DIV F/G 9/5
ELECTRICAL CHARACTERIZATION AND SPECIFICATION OF SPECIAL PURPOS--ETC(U)
JUN 81 J S KULPINSKI, L CARROZZA, T SIMONSEN F30602-78-C-0195
UNCLASSIFIED RADC-TR-81-74 NL




1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART

A_V = 5 V/V

Parameter Symbol	Conditions A/V = 5 V/V	VENDOR CODE D Serial No.					VENDOR CODE C Serial No.					VENDOR CODE B Serial No.					UNIT
		60	61	62	67	68	69	70	71	72	73	78	79	80	81	82	
TR (tr)	VO = .05V VO = .5	270	260	290	290	260	290	300	280	310	290	240	260	250	260	280	ns
TR (os)	VO = .05V VO = .5V	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	%
SR (+)	VO = -5V TO + 5V	95.0	80.0	75.0	70.0	75.0	75.0	65.0	80.0	70.0	75.0	80.0	65:0	80.0	50.0	75.0	V/us
SR (-)	VO = -5V TO + 5V	90.0	85.0	95.0	80.0	75.0	85.0	85.0	110.0	90.0	95.0	95.0	80.0	85.0	85.0	90.0	V/us
ts	VO = -5V TO + 5V	450	450	450	550	500	400	300	300	400	300	550	600	600	650	600	ns

Table 3-16. LF157 Dynamic Data @ 25°C.

SECTION IV

MULTIPLE BI-FET OP AMPS

TABLE OF CONTENTS

SECTION IV

MULTIPLE BI-FET OP AMPS

MIL-M-38510/119

4.1 Introduction

The first op amps of this series which were introduced to RADC for characterization and possible slash sheet action were the TL061 and TL071 families from Texas Instruments. Each of these families included single, dual and quad device types. The TL061, TL062 and TL064 devices were offered as a low power category and the TL071, TL072 and TL074 devices were classified as low noise devices. Preliminary characterization studies at GEOS were encouraging and a recommendation for slash sheet action was made. Since these new BI-FET op amps had lower absolute maximum ratings than the LF155 series devices, it was necessary to generate a new slash sheet. National Semiconductor and Fairchild were also introducing multiple BI-FET op amp devices which could be included in the new slash sheet. Table 3-1 shows the relationship between the generic and military device types:

Table 4-1. Table of Device Types Specified.

Device Type	Generic Type	Manufacturer	BI-FET Op Amp Description
11901	TL061	Texas Instruments	Single-low power 1/
11902	TL062	" "	Dual-low power
11903	TL064	" "	Quad-low power
11904	TL071	" "	Single-general purpose 2/
" "	uAF771	Fairchild	" "
" "	LF151	National Semiconductor	" "
11905	TL072	Texas Instruments	Dual-general purpose
" "	uAF772	Fairchild	" "
" "	LF153	National Semiconductor	" "
11906	TL074	Texas Instruments	Quad-general purpose
" "	uAF774	Fairchild	" "
" "	LF147	National Semiconductor	" "

1/ The low power devices use less than 0.3 mA of supply current per op amp.
2/ The general purpose op amps are low cost J-FET front end devices, with performance that meet or exceed that of the popular 741 industry "workhorse".

4.2 Description of Device Types

The op amps specified in MIL-M-38510/119 have fewer J-FETs per op amp than the LF155 series devices. As a result the chip real estate per function is approximately 2/3 that of an LF155 device. Consequently, the options for lower cost and multiple op amp devices are also more viable than with the LF155 series design.

A simplified schematic which shows the main features of these new second generation BI-FET op amps is shown in Figure 4-1.

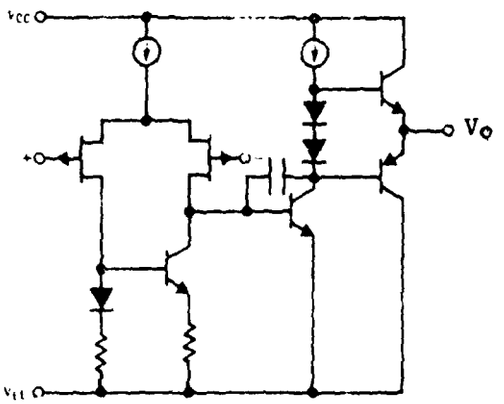


Figure 4-1. BI-FET Op Amp Simplified Schematic.

Detailed schematics of various generic devices are shown in Figures 4-2 through 4-3. All of these devices feature J-FETs for the differential input stage and complementary bipolar transistors for the totem pole output stage. Unlike the LF155 series design a J-FET is not used to replace the output PNP transistor for stability improvement.

Another common difference between these devices and the LF155 series is that the input J-FETs are not loaded by matched J-FET current sources. Instead a bipolar current mirror is used with trim resistors in the emitter legs. Offset voltage can be internally laser trimmed or externally potentiometer trimmed. Because of pinout restrictions some of the duals and all of the quads do not have external offset voltage adjustment capability. Caution should be exercised in swapping /119 single with /114 devices in applications using the offset control pins. Since the LF155 adjustment is connected to + Vcc and the /119 single device is connected to - Vcc proper operation after swapping will not work and could lead to device destruction if the trim wiper gets too close to one of the potentiometer ends.

The input for the single ended high gain second stage is taken off the collector of the current mirror transistor.

Another current mirror connected to a zener regulated current source provides separate constant current biasing for the first and second amplifier stages of the TL071 series devices.

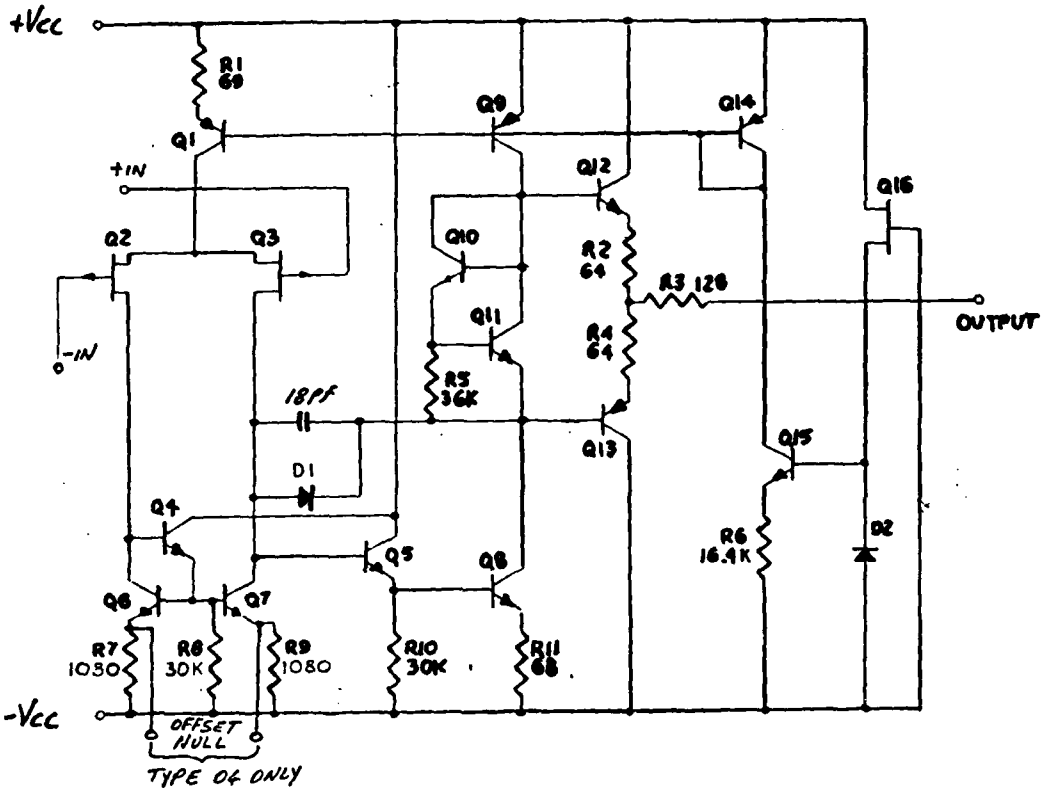


Figure 4-2. TL071 Series Op Amp Schematic.

The current source stage biasing for the other devices are all different in design. Modifications of current mirrors and lateral PNP transistors are used extensively as can be seen in the circuit schematics. The degree of circuitry used for stage biasing enables the op amps to be used over a wide range of power supply voltages while maintaining excellent power supply rejection to noise and other disturbances. Further details are covered in the manuals, books and papers referenced in the bibliography of this report.

All of the generic industry device types within the /119 specification have design differences which will tend to favor one parameter over another. As a consequence of this fact the margin of performance

between the different vendor devices and the specification limits will vary accordingly. The following device schematics are shown in the Appendix.

Figure	Device Electrical Schematic
4-3	TL061 Series Op Amp Schematic
4-4	LF151, 153, 147 Op Amp Schematic
4-5	uAF771 Series Op Amp Schematic

4.3 Test Development

The test development for the multiple BI-FET op amps was very similar to the procedure described in Section 3.3. A notable difference was that the test adapter had to be configured to accept dual and quad devices in addition to single devices. This was accomplished by building several DIP to TO5 pin-out converters with manual selection switches. Although this method was satisfactory in getting the data, a more elaborate relay controlled socket would have been more efficient for testing large quantities of devices, especially if this effort were required on a continuing basis. All of the standard op amp parameters as shown in the previous section Table 3-3 were required to characterize these devices.

The devices which were characterized are identified in Table 4-2.

Table 4-2. Device Types Characterized.

Generic Type	S/N	Manufacturer Code	Date Code	No. of Op Amps
TL061	101-120	A	-	20
TL062	201-210	A	-	20
TL064	301-303	A	7914	12
TL071	401-415	A	-	15
LF151	422-425	C	7925	3
AF771	431-440	B	7916	10
TL072	501-519	A	7831	20
LF153	521-526	C	7925	12
AF774	631-637	B	7906	20

Detailed test conditions and equations are identical to those in the Appendix, Table 3-4 except that the power supply voltages were reduced from ± 20 V to ± 15 V and the input common mode voltage range was reduced from ± 15 V to ± 11 V. The static test circuit is the same as that in Figure 3-2 except that the offset adjust resistor is 10 K ohms referenced to - Vcc.

Software changes were made to the program to reduce the power supply and command voltages to the specified values for these devices. Transient response, settling time and slew rate data were measured manually with a new test fixture having dedicated DIP sockets for single, dual and quad devices.

As with the LF155 series devices, a Tektronix 577 curve tracer was used to observe parameter to parameter characteristics of sample devices. Further details on op amp characterization test procedures are contained in Section 3.3.

4.4 Test Results and Data

A total of 51 low power op amps and 81 general purpose op amps in a combination of single, dual and quad packages were tested on the Tektronix S-3260. The test data was released to RADC and the manufacturer representatives of the JC-41 Committee in a report entitled "Characterization Data for MIL-M-38510/119 Multiple BI-FET Op Amps", Oct. 1979. A typical data sheet of several dual general purpose devices (Type 05) is shown in Table 4-3. Other data sheets are in the Appendix as follows:

Table	Subject
4-4	Typical Device Type 02 Data at 25°C
4-5	Typical Device Type 02 Data at -55°C
4-6	Typical Device Type 02 Data at 125°C
4-7	Typical Device Type 05 Data at -55°C
4-8	Typical Device Type 05 Data at 125°C

Each of these data sheets show how the data values of 10 devices compares to the JC-41 Committee limits at a given test temperature. Most parameters were tested with ± 16 volt power supplies over a ± 12 volt common mode range. Even though device types 01, 02, and 03 are not rated to drive a 2000 ohm load, data was taken with this condition for information only.

Histograms were generated on an op amp basis for both device type families for all parameter-temperature combinations. One such histogram at 25°C of common mode rejection for device types 04, 05 and 06 is shown in Figure 4-6.

MANUFACTURER CODE: TT; DEVICE TYPE: 153 DUAL ; TEMPERATURE: +25 DEG C ; 06 SEP 79 14:47:23

PARAMETER	LO-LIM	581-1	581-2	582-1	582-2	583-1	583-2	584-1	584-2	585-1	585-2	HI-LIM	UNIT
VIO(-CM) AT 25V,-4V	-5.00	2.80	-1.63	-3.36	3.19	-1.95	-2.39	-2.09	3.95	4.43	-1.99	5.00	MV
VIO(+CM) AT 4V,-25V	-5.00	3.00	-1.44	-3.83	4.53	-995.M	-2.08	-995.M	4.49	4.49	-1.65	5.00	MV
VIO(0CM) AT 15V,-15V	-5.00	2.10	-1.57	-3.15	3.93	-910.M	-2.13	-1.88	3.78	4.36	-1.81	5.00	MV
VIO(0CM) AT 5V,-5V	-5.00	2.48	-1.43	-3.21	3.53	-1.03	-2.06	-1.88	3.38	4.45	-1.80	5.00	MV
D-VIO/D-T FROM 25 OC	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	UV/C
IIO(-CM) AT 25V,-4V	-100.	11.0	29.5	96.0	-45.9	24.1	86.4	58.2	-18.9	79.9	30.4	100.	PA
IIO(+CM) AT 4V,-25V	-300.	-3.83	-45.9	-59.5	-144.	-61.3	817.	-23.4	-138.	-70.6	187.	300.	PA
IIO(0CM) AT 15V,-15V	-100.	-22.9	-23.7	1.10	-130. *	-31.5	316. *	-3.37	-84.8	38.3	62.0	100.	PA
IIO(+CM) AT 5V,-24V	-100.	-36.2	-31.1	-43.9	-208. *	-49.2	114. *	-13.6	-78.6	-27.5	69.2	100.	PA
+IIB(-CM) AT 25V,-4V	-200.	-19.9	-28.3	-103.	-85.8	-73.9	8.89	-117.	-23.2	-115.	8.66	200.	PA
+IIB(+CM) AT 4V,-25V	-200.	269.	223.	403.	122.	306.	436.	334.	71.8	333.	357.	1.20K	PA
+IIB(0CM) AT 15V,-15V	-200.	46.9	38.4	70.6	-78.0	44.8	274. *	32.2	33.6	83.1	128.	200.	PA
+IIB(+CM) AT 5V,-24V	-200.	126.	126.	212.	-61.7	154.	242.	162.	39.6	201.	209.	500.	PA
-IIB(-CM) AT 25V,-4V	-200.	-31.0	-57.7	-199.	-39.9	-98.0	-17.5	-169.	-4.31	-195.	-21.7	200.	PA
-IIB(+CM) AT 4V,-25V	-200.	272.	269.	463.	266.	367.	218.	357.	204.	403.	229.	1.20K	PA
-IIB(0CM) AT 15V,-15V	-200.	69.8	62.0	69.5	59.6	76.3	57.4	35.5	58.4	46.8	65.8	200.	PA
-IIB(+CM) AT 5V,-24V	-200.	162.	157.	256.	146.	203.	129.	175.	118.	228.	140.	500.	PA
+PSRR AT 5V,-15V	80.0	85.0	92.5	101.	100.	96.5	101.	98.5	118.	104.	200.	0.00	dB
-PSRR AT 15V,-5V	80.0	84.7	92.7	106.	88.2	96.1	104.	90.3	89.3	109.	101.	0.00	dB
CMR AT 15V,-15V	80.0	93.4	102.	93.1	85.1	102.	97.6	86.8	83.9	112.	94.9	0.00	dB
IOS(+) AT 15V,-15V	-80.0	-22.0	-22.2	-19.9	-20.7	-20.8	-20.6	-21.5	-21.4	-21.6	-21.6	0.00	MA
IOS(-) AT 15V,-15V	0.00	19.8	19.8	17.7	18.0	17.7	18.5	18.7	19.2	18.8	19.8	80.0	MA
ICC AT 15V,-15V	0.00	3.84 *	3.83 *	3.76 *	3.78 *	3.65 *	3.61 *	3.71 *	3.68 *	3.60 *	3.62 *	3.80	MA
+VOP AT RL=10K	12.0	15.1	15.1	15.1	15.2	15.2	15.1	15.2	15.2	15.2	15.2	0.00	V
-VOP AT RL=10K	0.00	-14.4	-14.4	-14.4	-14.4	-14.4	-14.4	-14.4	-14.4	-14.4	-14.4	-12.0	V
+VOP AT RL=2K	10.0	14.9	14.9	14.9	14.9	14.9	14.8	14.9	14.9	14.9	14.9	0.00	V
-VOP AT RL=2K	0.00	-14.2	-14.1	-14.2	-14.1	-14.2	-14.2	-14.2	-14.2	-14.2	-14.2	-10.0	V
AVS(+) AT RL=10K	50.0	300.	857.	800.	800.	545.	600.	600.	800.	600.	600.	0.00	V/MV
AVS(-) AT RL=10K	50.0	400.	400.	400.	400.	480.	800.	800.	800.	480.	343.	0.00	V/MV
AVS(+) AT RL=2K	50.0	218.	800.	300.	400.	400.	343.	400.	480.	480.	343.	0.00	V/MV
AVS(-) AT RL=2K	50.0	114.	100.	160.	185.	171.	160.	150.	800.	141.	141.	0.00	V/MV
AVS AT 5V,-5V,RL=10K	10.0	400.	160.	133.	88.9	857.	800.	133.	100.	160.	114.	0.00	V/MV
AVS AT 5V,-5V,RL=2K	10.0	88.9	80.0	114.	100.	114.	114.	88.9	114.	114.	88.9	0.00	V/MV
SR(+) AT 15V,-15V	7.00	16.7	16.4	16.4	17.2	16.1	16.1	16.7	16.9	16.4	16.1	0.00	V/US
SR(-) AT 15V,-15V	7.00	18.2	80.4	18.2	18.2	18.5	17.9	18.5	18.2	18.2	17.5	0.00	V/US

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 4-3. Typical Type 05 Data at 25°C.

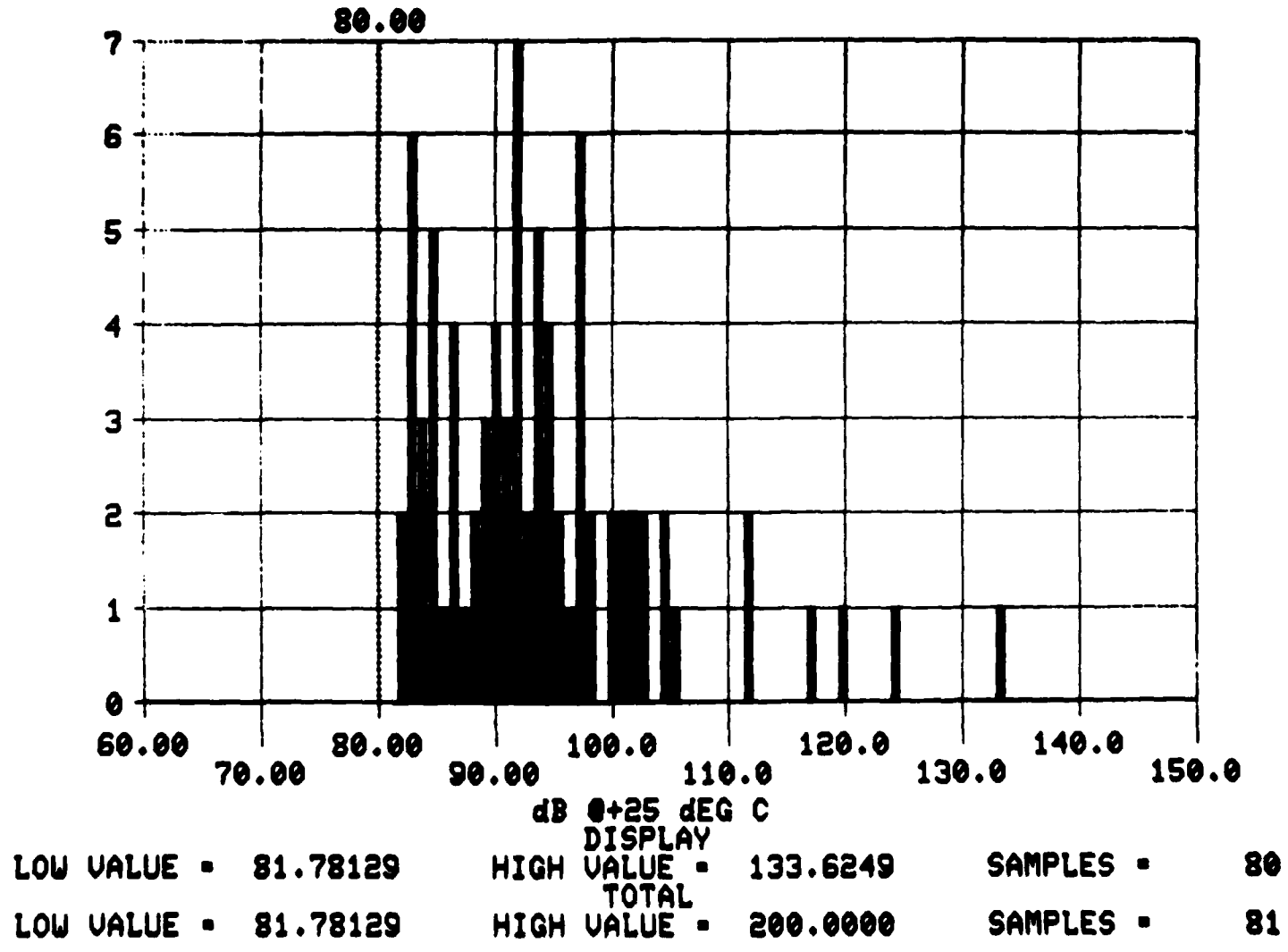


Figure 4-6. Common Mode Rejection at 25°C

Table 4-9. Device Type 01,02,03 Data Distribution & Limits
(Sheet 1 of 2)

PARAMETER (-55°C < TA < 125°C)	* [///DATA////] * LL<--------LIMIT-------->HL	UNIT
Offset Voltage (25°C) (Vio)	[//*//////////////////*//] . .-5 . . . . 0 5	mV
Offset Voltage (Vio)	[//////*//////////////////////////*] . . . .-7 . . . . . 0 7	mV
Offset Voltage Drift D-Vio/D-T	* [//////////////////*/] -30 . . . . . 0 . . . . . 30.	.uV/oC
Offset Current (25°C) (Iio)	[*/////////////////*] . . . .-100 . . . 0 . . . 100 . .	pA
Offset Current (Iio)	* [////] * . . . . -20 . . . 0 . . . 20. . .	nA
Input Bias Current (25°C) (0V Common Mode)	* [////////] * . . . .-200 . . . 0 . . . 200 . .	pA
Input Bias Current (25°C) (-12V Common Mode)	[/*//////////////////] * -400 . . . . . 0 . . . 200 . .	pA
Input Bias Current (25°C) (12V Common Mode)	* [///////////////] * -200 . 0 . . . . . 1200.	pA
Input Bias Current (125°C) (+ 0V and -12V Common Mode)	*[/////////] * -10 . . . . . 70. .	nA
Input Bias Current (125°C) (12V Common Mode)	*[//////////] * -10 100	nA
Power Supply Rejection (+PSRR,-PSRR)	[//*//////////////////] 80 . . . . . 120 . .	dB
Common Mode Rejection (CMR)	*[//////////////////] 80 . . . . . 120 . .	dB

Table 4-9. Device Type 01,02,03 Data Distribution & Limits
(Sheet 2 of 2)

PARAMETER (-55oC < TA < 125°C)	* [///DATA////] * LL<--------LIMIT-------->HL	UNIT
Output Short Circuit Current IOS(+)	* [//] -40 0	mA
Output Short Circuit Current IOS(-)	[/] * 0 40	mA
Supply Current (per Op Amp) (Icc) Ta= -55°C	[/] * 0 . . . . .0.3.	mA
Supply Current (per Op Amp) (Icc) 25°C< Ta <125°C	[/] * 0 . . . . .0.3.	mA
Output Voltage Swing (+Vop) 10 Kohm Load	* [/] 12 16	V
Output Voltage Swing (-Vop) 10 Kohm Load	[//] * -16 . . . . . .-12	V
Voltage Gain (25°C) (Avs(+)) 10 Kohm Load	* [/////////] 5 . . . . . 15.	V/mV
Voltage Gain (25°C) (Avs(-)) 10 Kohm Load	[*/////] 5 15	V/mV
Voltage Gain (Avs(+)) 10 Kohm Load	* [//////////////] 4 . . . . 9 15	V/mV
Voltage Gain (Avs(-)) 10 Kohm Load	[//*///////] . . 4 . . . . 9 15	V/mV
Slew Rate (25°C) (SR(+))	* [////] 0 . . . . . 4 8	V/uS
Slew Rate (25°C) (SR(-))	* [///////////////] 0 . . . . . 4 8	V/uS
Slew Rate (SR(+))	* [///] 0 . . . . . 4 8	V/uS
Slew Rate (SR(-))	* [//////////////////] 0 . . . . . 4 8	V/uS

Table 4-10. Device Type 04,05,06 Data Distribution & Limits
(Sheet 1 of 2)

PARAMETER ($-55^{o}C < TA < 125_{oC}$)	* [///DATA////] * LL<--------LIMIT-------->HL	UNIT
Offset Voltage ($25^{o}C$) (Vio)	[*/////////////////////*/] . .-5 . . . . 0 5	mV
Offset Voltage (Vio)	[//*/////////////////////////////*] . . . .-7 . . . . . 0 7	mV
Offset Voltage Drift D-Vio/D-T	* [/////////////////////*/] -30 . . . . . 0 . . . . . 30. .	uV/oC
Offset Current ($25^{o}C$) (Iio)	[*/////////////////*///] . . . .-100 . . . 0 . . . 100 . .	pA
Offset Current (Iio)	* [/////////] * . . . . -20 . . . 0 . . . 20. . .	nA
Input Bias Current ($25^{o}C$) (0V Common Mode)	* [/////////] * . . . .-200 . . . 0 . . . 200 . .	pA
Input Bias Current ($25^{o}C$) (-12V Common Mode)	[/*////////////////////] * -400 . . . . . 0 . . . 200 . .	pA
Input Bias Current ($25^{o}C$) (12V Common Mode)	* [///////////////] * -200 . 0 . . . . . 1200.	pA
Input Bias Current ($125^{o}C$) (+ 0V and -12V Common Mode)	*[////////] * -10 . . . . . 70. .	nA
Input Bias Current ($125^{o}C$) (12V Common Mode)	* [/////////] * -10 100	nA
Power Supply Rejection (+PSRR,-PSRR)	[*/////////////////////] 80 . . . . . 120 . .	dB
Common Mode Rejection (CMR)	[*/////////////////////] 80 . . . . . 120 . .	dB

Table 4-10. Device Type 04,05,06 Data Distribution & Limits
(Sheet 2 of 2)

PARAMETER (-55°C < TA < 125°C)	* [///DATA////] * LL<--------LIMIT--------->HL	UNIT
Output Short Circuit Current IOS(+)	* [/] -80 0	mA
Output Short Circuit Current IOS(-)	[//] * 0 80	mA
Supply Current (per Op Amp) (Icc) Ta= -55°C	[//] * 0 . . . . . 4 . .	mA
Supply Current (per Op Amp) (Icc) 25°C< Ta <125°C	[//] * 0 . . . . . .3.5. . .	mA
Output Voltage Swing (+Vop) 10 Kohm Load	* [/] 12 16	V
Output Voltage Swing (-Vop) 10 Kohm Load	[///] * -16 . . . . . .-12	V
Voltage Gain (25°C) (Avs(+)) 10 Kohm Load	*[////////////////// 50 300	V/mV
Voltage Gain (25°C) (Avs(-)) 10 Kohm Load	*[////////////////// 50 300	V/mV
Voltage Gain (Avs(+)) 10 Kohm Load	* [////////////////// 25 300	V/mV
Voltage Gain (Avs(-)) 10 Kohm Load	* [////////////////// 25 300	V/mV
Slew Rate (25°C) (SR(+))	[/*/////////////] 0 . . 7 25	V/uS
Slew Rate (25°C) (SR(-))	[*/////////////] 0 . . 7 25	V/uS
Slew Rate (SR(+))	[*/////////////] 0 . 5 25	V/uS
Slew Rate (SR(-))	[*/////////// 0 . 5 25	V/uS

4.5 Discussion of Results

The characterization data was carefully reviewed to determine how well it complies to the proposed JC-41 limits and the June 1979 Rev. 1 issue of MIL-M-38510/119. Where there is good agreement between the data and the limits, no further discussion is given here. The proposed JC-41 parameter limits were then carried over into Table 4-11. Where there is a discrepancy between the data and the JC-41 limits a discussion is included with GEOS proposed limits. Because of the limited sample size (51 low power op amps and 81 low cost op amps), the GEOS data may not accurately reflect the data of all manufacturer lot samples.

Tables 4-9 and 4-10 shows the distribution of most parameters in a cryptic histogram form. This comparison of data and initial limits is a good guage for defermining if any changes should be considered.

Input Offset Voltage (Vio)

With the exception of Vendor B Type 04 devices at 125°C, the offset voltage data agrees with the proposed limits of ± 5 mV and ± 7 mV at 25°C and over the military temperature range, respectively. No limit change was recommended.

Input Offset Current (Iio)

Early in the characterization program there were many device failures to the ± 50 pA JC-41 limits. Because of this the histogram and statistical analysis limits were loosened to ± 100 pA. A comparison of the 25°C, zero common mode offset current data against the data limits is as follows:

Device Type	Yield at $I_{io} = \pm 100$ pA (max)	Yield at $I_{i0} \pm 50$ pA (max)
01,02,03	(51-8)/51 = 84%	(51-15)/51 = 70%
04,09,06	(81-18)/81 = 78%	(81-27)/81 = 67%

Even with 100 pA limits, the yield is relatively low. Looser limits were not requested by the manufacturers.

Input Bias Current (± IiB)

At the negative common mode condition at 25°C, both device families had yields of less than 70% against the -200 pA limit. The yields improve to better than 80% with a recommended low limit of -400 pA. The high temperature high limits were too loose and it is suggested that they be changed from 100 nA to 70 nA at the positive common mode voltage and from 70 nA to 50 nA for the other common mode voltage conditions.

Short Circuit Current (Ios(+), Ios(-)

Based on these devices alone, limits of 30 mA would be recommended; however, other vendor type devices, not yet characterized, require the 40 mA limit for the low power category. The general purpose device limits of ± 80 mA are very conservative for the data distribution, which had a peak value of Ios(+) = - 50.6 mA at - 55°C.

Supply Current (Icc)

Although the supply current is specified on an op amp basis, observations of the data show that duals and quads use less current per op amp than does a single device. An average "discount" for the multiple op amps based on histogram mean values is 20% for the duals and 30% for the quads. No change is recommended for /119.

Output Voltage Swing (+ Vop, - Vop)

Based on the data, the voltage swing limits are specified very conservatively. For device types 01, 02 and 03 with a 10K ohm load, - Vop is the weakest drive. 50 out of 51 devices had less than 1.2 V of negative saturation. (-Vsat = | -Vcc - (-Vop) |).
The single 01 maverick with 1.7 V of negative saturation also failed the Vio, -PSRR and the gain tests. For the 04, 05, and 06 device data the maximum saturation drops were 2.1 V at 10 K ohm and 3.5 V with 2 K ohm loading.

It is recommended that the swing limits be increased to 12.5 V at 10 ohm and 11 V at 2 K ohm. The characterization data was measured with ± Vcc = ± 16 V, whereas the proposed slash sheet is specified with ± Vcc = ± 15 V. Because of this difference the data was examined on an "output to rail" basis.

Open Loop Voltage Gain (A_{VS}(+), (A_{VS}(-))

One of the tradeoffs for device types 01, 02 and 03 is that the low power option results in lower open loop gain. One change that can be recommended is that A_{VS} at ± Vcc = ± 5 V be increased from 2 to 3 V/mV (min.). The lowest corresponding data value was approximately 4.8 V/mV at - 55 °C.
As a general observation, device types 04, 05 and 06 have lower gains than the LF155 series devices by a factor of from 1/4 to 1/3.

Slew Rate (SR(+), SR(-))

With the exception of several failures from vendor code B devices, all of the devices had slew rates greater than the specified minimum levels. No specification change is recommended, unless vendor code B determines that a relaxation in limits is necessary.

Transient Response (TR(tr), TR(os))

The previous parameters were measured automatically, but transient response was measured manually with a signal generator and an oscilloscope. Histograms were generated on the S-3260 from the manual data.

For low power devices the data indicates that the rise time and overshoot should be changed from 600 nanoseconds and 40% to 400 nanoseconds and 20% respectively. These limits would still leave a 2:1 margin from the observed worst cases. Device types 04, 05 and 06 have data in good agreement with the limits.

Settling Time (ts(+), ts(-))

The data indicates that the settling time limit for device types 01, 02 and 03 needs to be increased from 1500 ns to 6000 ns. The initial limits of 1500 ns was a tentative estimate without a JC-41 recommendation.

In view of the fact that device types 04, 05 and 06 have four to five times as fast a slew rate as the low power devices, it is not surprising that the data yields a similar conclusion with regard to settling time.

4.6 Slash Sheet Development

MIL-M-38510/119 was developed according to the pattern established for MIL-M- 38510/114 and earlier op amp specifications. The major differences are in reduced power supply conditions and somewhat looser limits. The burn-in circuits are identical with those in MIL-M-38510/114.

4.7 Conclusions and Recommendations

A characterization study was conducted on a mix of single, dual and quad BI-FET op amps. The data base consists of 51 low power op amps and 81 general purpose op amps. Minor changes in JC-41 specifications were made to reflect GEOS's data observations, yield considerations and user priorities. These multiple BI-FET op amps should find many useful applications in military systems.

A recommended slash sheet was submitted to RADC and the JC-41 Committee. The attached Table 4-11 represents the finalized MIL-M-38510/119 Table I specification.

4.8 Bibliography

1. R. Russell and T. Frederiksen, "How the BI-FET process benefits linear circuits," Electronics, June 8, 1978.
2. BI-FET op amp family from Texas Instruments, Bulletin CB-24B.
3. Linear Applications Handbook, National Semiconductor (1978).
4. Linear Databook, National Semiconductor (1978).
5. Signetics Analog Data Manual (1977).

TABLE I. Electrical performance characteristics.

Characteristics	Symbol	Conditions $\pm V_{CC}$ = ±15 V (see 3.4 and figure 7, unless otherwise specified)		Device types	Limits Min	Limits Max	Unit
Input offset voltage	V_{IO}	$\pm V_{CC}$ = ±5 V at V_{CM} = 0 V, and $\pm V_{CC}$ = ±15 V at V_{CM} = ±11 V, 0 V	T_A = 25°C	All	-5	5	mV
			-55°C ≤ T_A ≤ +125°C		-7	7	mV
Input offset voltage temperature sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	V_{CM} = 0 V			-30	30	µV/°C
Input offset current	I_{IO} 3/	V_{CM} = 0 V; t ≤ 25 ms	T_J = 25°C		-100	100	pA
			T_J = 125°C		-20	20	nA
Input bias current	$+I_{IB}$	V_{CM} = +11 V; t ≤ 25 ms	T_J = 25°C		-200	1,200	pA
			T_J = 125°C		-10	70	nA
	$-I_{IB}$ 1/	$\pm V_{CC}$ = ±15 V; V_{CM} = 0 V; t ≤ 25 ms	T_J = 25°C		-200	200	pA
			T_J = 125°C		-10	50	nA
	2/	V_{CM} = -11 V; t ≤ 25 ms	T_J = 25°C		-400	200	pA
			T_J = 125°C		-10	50	nA
Power supply rejection ratio	+PSRR	$+V_{CC}$ = 20 V, 10 V; $-V_{CC}$ = -15 V			80	---	dB
	-PSRR	$+V_{CC}$ = 15 V; $-V_{CC}$ = -20 V, -10 V			80	---	dB
Input voltage common mode rejection 4/	CMR	-11 V ≤ V_{CM} ≤ 11 V			80	---	dB
Adjustment for input offset voltage 7/	V_{IO} ADJ(+)	V_{CM} = 0 V		01,02,04,05	+8	---	mV
	V_{IO} ADJ(-)	V_{CM} = 0 V		01,02,04,05	---	-3	mV
Output short circuit current (for positive output) 5/	$I_{OS(+)}$	t ≤ 25 ms (short circuit to ground)		01,02,03	-40	---	mA
				04,05,06	-80	---	

Table 4-11. Final MIL-M-38510/119 Electrical Specification

TABLE I. Electrical performance characteristics - Continued.

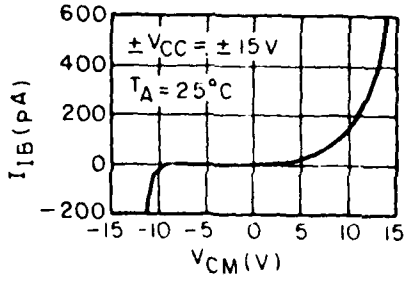
Characteristics	Symbol	Conditions $\pm V_{CC} = \pm 15$ V (see 3.4 and figure 7, unless otherwise specified)		Device types	Limits Min	Limits Max	Unit
Output short circuit current (for negative output) 5/	$I_{OS(-)}$	t ≤ 25 ms (short circuit to ground)		01,02,03	---	40	mA
				04,05,06	---	80	
Supply current (per amplifier)	I_{CC}		$T_A = -55°C$	01,02,03	---	0.3	mA
				04,05,06	---	4.0	
			$25°C \leq T_A \leq 125°C$	01,02,03	---	0.3	
				04,05,06	---	3.5	
Output voltage swing (maximum)	$+V_{OP}$, $-V_{OP}$	$R_L = 10$ kΩ		All	±12	---	V
		$R_L = 2$ kΩ		04,05,06	±10	---	
Open loop voltage gain (single ended) 6/	$A_{VS(+)}$,	V_{OUT} = 0 to 10 V 01-03, R_L=10 kΩ;	$T_A = 25°C$	01,02,03	5	---	V/mV
				04,05,06	50	---	
	$A_{VS(-)}$	V_{OUT} = -10 to 0 V 04-06, R_L = 2 kΩ	$-55°C \leq T_A \leq 125°C$	01,02,03	4	---	
				04,05,06	25	---	
Open loop voltage gain (single ended) 6/	A_{VS}	$\pm V_{CC} = \pm 5$ V; $R_L = 10$ kΩ; $V_{OUT} = \pm 2$ V		01,02,03	3	---	V/mV
				04,05,06	20	---	
Transient response rise time	$TR_{(tr)}$	$A_V = 1$; $V_{IN} = 50$ mV; $C_L = 100$ pF (see figure 8)	$R_L = 10$ kΩ	01,02,03	---	400	ns
			$R_L = 2$ kΩ	04,05,06	---	200	
Transient response overshoot	$TR_{(os)}$		$R_L = 10$ kΩ	01,02,03	---	20	Percent
			$R_L = 2$ kΩ	04,05,06	---	40	
Slew rate	$SR(+)$ and $SR(-)$	$V_{IN} = \pm 5$ V; $A_V = 1$ (see figure 8)	$T_A = 25°C$	01,02,03	.8	---	V/µs
				04,05,06	7	---	
			$T_A = -55°C$, $125°C$	01,02,03	.7	---	
				04,05,06	5	---	
Settling time	$ts(+)$ and $ts(-)$	(0.1 percent error) $T_A = 25°C$ $A_V = 1$ (see figure 9)		01,02,03	---	6,000	ns
				04,05,06	---	1,500	
Noise (referred to input) broadband	$N_I(BB)$	Bandwidth = 10 kHz (see figure 10)	$T_A = 25°C$	All	---	15	µVrms
Noise (referred to input) popcorn	$N_I(PC)$		$T_A = 25°C$	All	---	80	µVpk
Channel separation 8/	CS	See figure 11	$T_A = 25°C$	02,03,05,06	80	---	dB

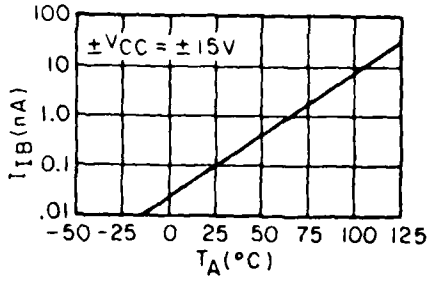
Table 4-11. Final MIL-M-38510/119 Electrical Specification

Footnotes:

1/ Bias currents are actually junction leakage currents which double (approximately) for each 10°C increase in junction temperature T_J. Measurement of bias current is specified at T_J rather than T_A, since normal warmup thermal transients will affect the bias currents. The measurements for bias currents must be made within 25 ms after power is first applied to the device for test. Measurement at $T_A = -55°C$ is not necessary since expected values are too small for typical test systems.

2/ Bias current is sensitive to power supply voltage, common mode voltage and temperature as shown by the following typical curves:





3/ I_{IO} is calculated as the difference between $+I_{IB}$ and $-I_{IB}$.

4/ CMR is calculated from V_{IO} measurements at $V_{CM} = +11$ and -11 V.

5/ Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that $T_J(max) \leq 175°C$.

6/ Because of thermal feedback effects from output to input, open loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

7/ Offset adjustment pins do not exist for 8-pin dual and 14-pin quad packages.

8/ Channel separation is applicable only for the dual and quad devices.

Table 4-11. Final MIL-M-38510/119 Electrical Specification

SECTION IV

APPENDIX

MULTIPLE BIFET OP AMPS

MIL-M-38510/119

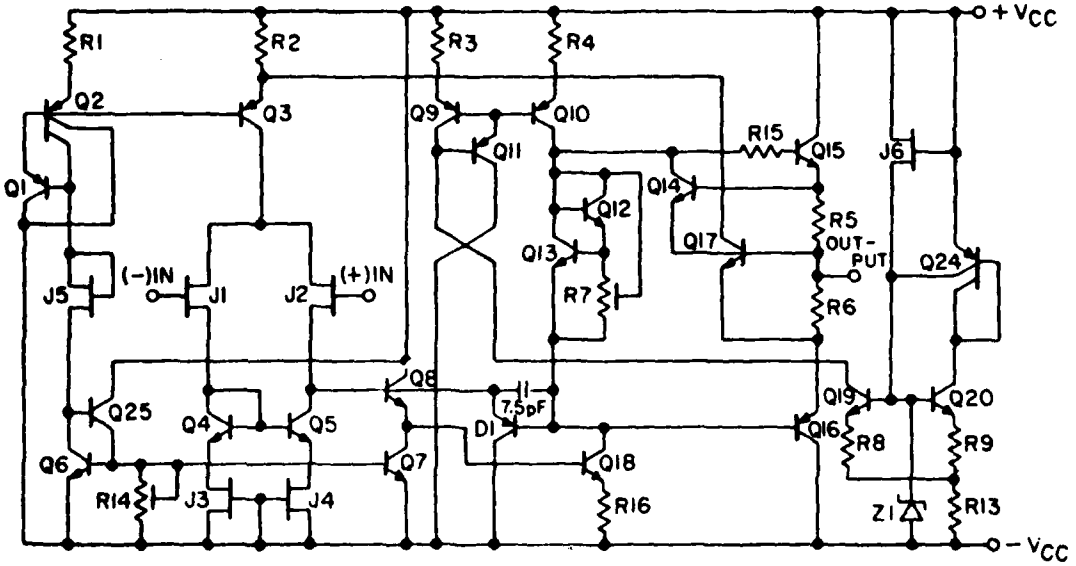


Figure 4-3. TL061 Series Op Amp Schematic

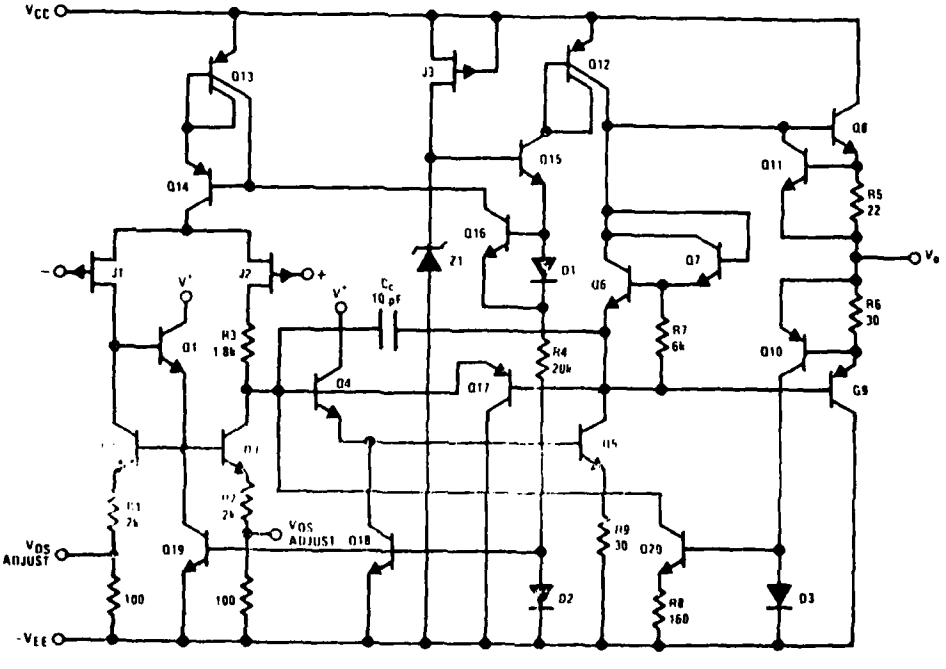


Figure 4-4. LF151, 153, 147 Op Amp Schematic

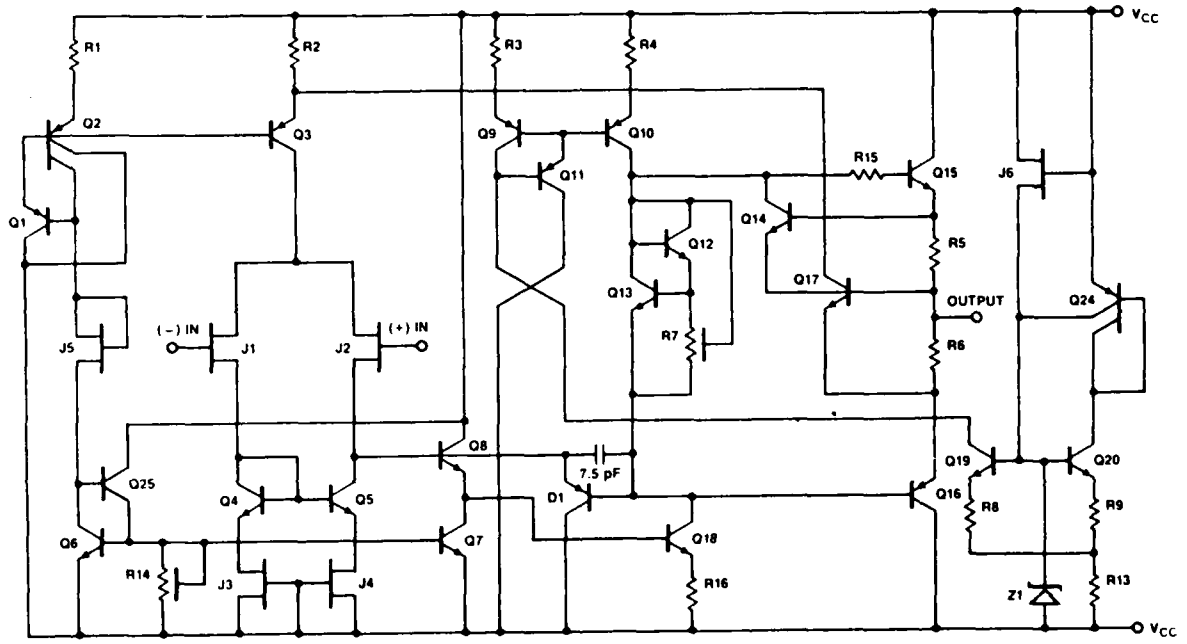


Figure 4-5 . uAF771 Series Op Amp Schematic.

MANUFACTURER CODE: ^ ; DEVICE TYPE: 02 DUAL- 8 ; TEMPERATURE: +25 DEG C ; 21 SEP 79 15:52:32

PARAMETER	LO-LIM	801	802	803	804	805	806	807	808	809	810	HI-LIM	UNITS
VIO(-CM) AT 20V,-4V	-5.00	1.30	-443.M	-1.48	-104.M	-96.0M	-362.M	-1.78	-598.M	-1.22	-884.M	5.00	MV
VIO(+CM) AT 4V,-20V	-5.00	2.30	-343.M	-488.M	-876.M	146.M	-548.M	-1.98	-1.41	-1.18	-330.M	5.00	MV
VIO(@CM) AT 16V,-16V	-5.00	1.90	-581.M	-800.M	-306.M	-63.0M	-886.M	-1.91	-1.04	-1.15	-78.0M	5.00	MV
VIO(@CM) AT 5V,-5V	-5.00	1.50	-90.0M	-1.08	76.0M	-30.0M	-448.M	-1.51	-388.M	-1.18	17.0M	5.00	MV
D-VIO/D-T FROM 25 OC	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	UV/C
IIO(-CM) AT 20V,-4V	-100.	-51.8	-31.4	88.4	348. X	-3.34	5.80	-18.3	-81.2	-7.83	-13.8	100.	PA
IIO(+CM) AT 4V,-20V	-300.	73.8	180.	70.3	-233.	73.9	79.2	184.	147.	137.	91.6	300.	PA
IIO(@CM) AT 16V,-16V	-100.	-36.0	-748.M	1.05	17.2	2.83	3.36	-0.58	-6.60	-0.16	8.72	100.	PA
IIO(+CM) AT 8V,-24V	-100.	18.1	50.8	30.7	-161. X	33.2	29.3	52.2	43.5	54.4	34.3	100.	PA
+IIB(-CM) AT 20V,-4V	-200.	-140.	-163.	-98.0	-314. X	-122.	-98.8	-149.	-194.	-138.	-142.	200.	PA
+IIB(+CM) AT 4V,-20V	-200.	437.	435.	341.	591.	342.	307.	433.	455.	436.	384.	1.00K	PA
+IIB(@CM) AT 16V,-16V	-200.	-9.18	2.16	-7.74	22.0	-12.6	-19.1	-12.1	-13.4	-14.4	3.65	200.	PA
+IIB(+CM) AT 8V,-24V	-200.	175.	186.	134.	278.	132.	107.	177.	163.	178.	145.	500.	PA
-IIB(-CM) AT 20V,-4V	-200.	-89.1	-131.	-120.	-656. X	-118.	-104.	-137.	-133.	-130.	-128.	200.	PA
-IIB(+CM) AT 4V,-20V	-200.	364.	306.	265.	824.	268.	228.	309.	308.	299.	273.	1.00K	PA
-IIB(@CM) AT 16V,-16V	-200.	25.8	2.90	-8.79	4.80	-15.5	-22.4	-2.49	-6.79	-5.25	-6.07	200.	PA
-IIB(+CM) AT 8V,-24V	-200.	156.	135.	104.	438.	99.3	78.2	125.	120.	122.	110.	500.	PA
+PSRR AT 5V,-15V	80.0	89.9	107.	104.	93.6	90.9	90.5	115.	92.5	88.4	93.9	0.00	dB
-PSRR AT 15V,-5V	80.0	89.4	88.6	200.	91.3	99.0	91.3	84.5	83.1	93.0	91.6	0.00	dB
CMR AT 15V,-15V	80.0	87.7	108.	87.2	103.	99.9	102.	102.	89.3	116.	106.	0.00	dB
IOS(+) AT 15V,-15V	-40.0	-8.70	-8.15	-8.55	-8.10	-9.20	-9.10	-8.60	-8.45	-8.55	-8.75	0.00	MA
IOS(-) AT 15V,-15V	0.00	5.85	5.55	5.85	5.60	6.40	6.40	6.65	6.60	6.20	6.20	40.0	MA
ICC AT 15V,-15V	0.00	335.MX	300.M	310.MX	235.M	306.MX	355.MX	300.M	320.MX	300.M	336.MX	300.M	MA
+VOP AT RL=10K	12.0	15.2	15.2	15.1	15.2	15.2	15.2	15.2	15.2	15.2	15.2	0.00	V
-VOP AT RL=10K	0.00	-14.9	-14.8	-14.9	-14.8	-14.9	-14.9	-14.9	-14.9	-14.9	-14.9	-12.0	V
+VOP AT RL=2K	10.0	14.7	14.6	14.6	14.6	14.7	14.6	14.6	14.6	14.6	14.6	0.00	V
-VOP AT RL=2K	0.00	-8.95 X	-8.80 X	-9.10 X	-8.80 X	-9.85 X	-9.85 X	-10.0	-9.90 X	-9.65 X	-9.60 X	-10.0	V
AVS(+) AT RL=10K	5.00	13.1	15.3	12.8	15.2	14.3	13.8	15.3	13.2	13.6	14.4	0.00	V/MV
AVS(-) AT RL=10K	5.00	6.08	5.23	5.31	5.22	6.40	6.12	6.25	6.06	5.76	6.07	0.00	V/MV
AVS(+) AT RL=2K	5.00	8.12	7.65	6.67	7.47	7.90	7.90	8.63	7.84	7.60	7.88	0.00	V/MV
AVS(-) AT RL=2K	5.00	977.MX	817.MX	700.MX	823.MX	838.MX	803.MX	750.MX	784.MX	776.MX	838.MX	0.00	V/MV
AVS AT 5V,-5V,RL=10K	2.00	2.80	2.21	1.95	2.00	2.77	2.65	2.99	2.38	2.23	2.36	0.00	V/MV
AVS AT 5V,-5V,RL=2K	2.00	2.25	1.88 X	1.91 X	1.86 X	2.34	2.26	2.30	2.23	2.10	2.24	0.00	V/MV
SR(+) AT 15V,-15V	2.00	2.40	1.96 X	2.24	1.98 X	2.41	2.27	2.38	2.34	2.20	2.28	0.00	V/US
SR(-) AT 15V,-15V	2.00	4.24	2.89	4.88	2.98	4.67	4.63	4.65	4.44	4.30	4.67	0.00	V/US

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 4-4 Typical type 02 data at 25°C.

MANUFACTURER CODE: TT; DEVICE TYPE: 02 DUAL- 2 ; TEMPERATURE: -55 DEG C ; 27 SEP 79 10:26:32

PARAMETER	LO-LIM	001	002	003	004	005	006	007	008	009	010	HI-LIM	UNIT
VIO(-CM) AT 20V,-4V	-7.00	1.11	348.M	361.M	-935.M	-885.M	-484.M	-1.72	80.0M	-1.68	218.M	7.00	MV
VIO(+CM) AT 4V,-20V	-7.00	0.13	584.M	1.40	-1.06	-340.M	-563.M	-1.90	-906.M	-1.80	-88.0M	7.00	MV
VIO(0CM) AT 10V,-10V	-7.00	1.76	368.M	385.M	-1.06	-600.M	-736.M	-1.96	-645.M	-1.70	190.M	7.00	MV
VIO(0CM) AT 5V,-5V	-7.00	1.28	486.M	850.M	-780.M	-678.M	-674.M	-1.63	189.M	-1.55	302.M	7.00	MV
D-VIO/D-T FROM 25 OC	-30.0	2.94	-11.1	-23.1	9.51	6.83	625.M	562.M	-4.94	7.94	-3.47	30.0	UV/C
IIO(-CM) AT 20V,-4V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
IIO(+CM) AT 4V,-20V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
IIO(0CM) AT 10V,-10V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
IIO(+CM) AT 5V,-20V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+IIB(-CM) AT 20V,-4V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+IIB(+CM) AT 4V,-20V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+IIB(0CM) AT 10V,-10V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+IIB(+CM) AT 5V,-20V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
-IIB(-CM) AT 20V,-4V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
-IIB(+CM) AT 4V,-20V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
-IIB(0CM) AT 10V,-10V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
-IIB(+CM) AT 5V,-20V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+PSRR AT 5V,-10V	80.0	92.5	101.	94.5	101.	95.1	93.2	100.	94.5	93.2	96.3	0.00	dB
-PSRR AT 10V,-5V	80.0	91.6	91.7	103.	91.2	96.5	90.5	86.1	81.1	87.3	87.4	0.00	dB
CMR AT 10V,-10V	80.0	87.4	100.	87.2	106.	97.9	110.	99.3	87.0	105.	97.9	0.00	dB
IOS(+) AT 15V,-15V	-40.0	-11.9	-9.90	-9.65	-9.60	-11.5	-11.6	-11.4	-11.6	-11.1	-11.2	0.00	MA
IOS(-) AT 15V,-15V	0.00	6.15	5.35	4.90	5.75	6.50	6.40	6.70	6.65	6.45	6.15	40.0	MA
ICC AT 15V,-15V	0.00	305.M	x 385.M	x 290.M	350.M	x 300.M	x 285.M	305.M	x 295.M	285.M	285.M	300.M	MA
+VOP AT RL=10K	12.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	0.00	V
-VOP AT RL=10K	0.00	-14.8	-14.8	-14.8	-14.8	-14.8	-14.8	-14.8	-14.8	-14.8	-14.8	-12.0	V
+VOP AT RL=2K	10.0	13.8	12.5	11.3	12.1	13.6	13.5	13.6	13.5	13.1	13.3	0.00	V
-VOP AT RL=2K	0.00	-9.00	x -8.25 x	-7.35 x	-8.80	x -9.00	x -8.60	x -9.90	x -9.70	x -9.00	x -9.35	x -10.0	V
AVS(+) AT RL=10K	4.00	11.2	12.2	7.66	10.1	11.9	11.7	12.9	11.3	11.5	10.2	0.00	V/MV
AVS(-) AT RL=10K	4.00	6.14	4.96	3.78	x 5.08	6.17	5.96	6.18	6.00	5.72	6.06	0.00	V/MV
AVS(+) AT RL=2K	4.00	5.26	4.09	868.M	x 3.86	x 4.99	4.90	5.21	4.99	4.82	4.73	0.00	V/MV
AVS(-) AT RL=2K	4.00	982.M	x 967.M x	900.M	x 786.M	x 811.M	x 884.M	x 744.M	x 900.M	x 751.M	x 958.M	x 0.00	V/MV
AVS AT 5V,-5V,RL=10K	2.00	8.48	7.28	4.88	7.33	8.08	8.08	8.32	8.15	7.98	7.96	0.00	V/MV
AVS AT 5V,-5V,RL=2K	2.00	8.07	1.83	x 1.18	x 1.88	x 8.07	8.01	8.00	8.04	1.91	x 8.00	0.00	V/MV
SR(+) AT 10V,-10V	1.00	1.90	1.68	1.82	1.87	1.90	1.87	1.86	1.84	1.88	1.86	0.00	V/US
SR(-) AT 10V,-10V	1.00	8.76	8.17	3.88	8.18	4.06	4.86	4.48	4.31	4.89	4.82	0.00	V/US

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 4- 5 Typical Type 02 Data at -55°C.

MANUFACTURER CODE: ^ ; DEVICE TYPE: 02 DUAL- 1 ; TEMPERATURE: +125 DEG C ; 21 SEP 79 15:33:17

PARAMETER	LO-LIM	201	202	203	204	206	206	207	208	209	210	HI-LIM	UNITS
VIO(-CM) AT 20V,-4V	-7.00	2.69	1.01	2.48	2.61	-1.11	745.M	880.M	2.88	1.59	-1.18	7.00	MV
VIO(+CM) AT 4V,-20V	-7.00	1.96	1.30	2.04	3.20	-930.M	855.M	1.25	2.04	2.53	-466.M	7.00	MV
VIO(0CM) AT 10V,-10V	-7.00	2.16	1.26	2.01	3.16	-1.17	770.M	1.61	2.79	2.14	-655.M	7.00	MV
VIO(0CM) AT 5V,-5V	-7.00	2.02	1.06	2.41	2.93	-1.09	910.M	1.04	2.50	1.89	-1.07	7.00	MV
D-VIO/D-T FROM 25 OC	-30.0	2.50	0.00	0.00	12.3	3.20	2.19	7.36	9.70	10.2	6.30	30.0	UV/C
IIO(-CM) AT 20V,-4V	-20.0K	2.00K	-4.83K	-1.20K	-2.40K	499.	401.	-694.	-1.46K	-462.	-318.	20.0K	PA
IIO(+CM) AT 4V,-20V	-30.0K	-4.70K	3.36K	-1.43K	-3.34K	-1.70K	-2.36K	-1.69K	-3.13K	-1.73K	-1.57K	30.0K	PA
IIO(0CM) AT 10V,-10V	-20.0K	-3.07K	-1.75K	-2.11K	-3.45K	-630.	-793.	-936.	-2.64K	-1.13K	-988.	20.0K	PA
IIO(+CM) AT 0V,-24V	-20.0K	-3.04K	2.58K	-1.10K	-3.12K	-1.43K	-1.70K	-1.09K	-3.10K	-1.70K	-1.31K	20.0K	PA
+IIB(-CM) AT 20V,-4V	-10.0K	-24.4K	x -36.9K	x -34.5K	x -21.0K	x 140.	1.57K	1.54K	847.	2.40K	1.45K	70.0K	PA
+IIB(+CM) AT 4V,-20V	-10.0K	20.5K	35.7K	34.2K	27.2K	6.49K	9.89K	6.68K	7.54K	9.12K	8.49K	100.K	PA
+IIB(0CM) AT 10V,-10V	-10.0K	-7.65K	-4.07K	-3.62K	874.	2.69K	5.18K	3.83K	3.61K	5.43K	4.37K	70.0K	PA
+IIB(+CM) AT 0V,-24V	-10.0K	13.3K	25.0K	23.6K	20.5K	5.38K	8.63K	6.15K	6.42K	8.18K	7.45K	70.0K	PA
-IIB(-CM) AT 20V,-4V	-10.0K	-27.2K	x -32.1K	x -33.2K	x -18.5K	x -359.	1.17K	2.23K	2.31K	2.87K	1.77K	70.0K	PA
-IIB(+CM) AT 4V,-20V	-10.0K	25.2K	32.3K	35.6K	31.1K	8.21K	12.2K	8.27K	10.7K	10.9K	10.1K	100.K	PA
-IIB(0CM) AT 10V,-10V	-10.0K	-4.58K	-2.32K	-1.41K	4.33K	3.22K	5.98K	4.76K	6.15K	6.56K	5.36K	70.0K	PA
-IIB(+CM) AT 0V,-24V	-10.0K	16.4K	22.4K	24.7K	23.6K	6.81K	10.4K	7.23K	9.52K	9.89K	8.76K	70.0K	PA
+PSRR AT 5V,-16V	80.0	88.8	91.2	89.4	95.1	88.8	90.7	88.4	89.0	92.3	89.3	0.00	dB
-PSRR AT 16V,-5V	80.0	83.7	103.	84.5	103.	96.8	89.6	90.3	115.	118.	96.1	0.00	dB
CMR AT 16V,-16V	80.0	90.3	96.1	94.8	91.0	102.	109.	87.8	96.6	88.1	90.5	0.00	dB
IOS(+) AT 15V,-15V	-40.0	-5.25	-5.00	-5.05	-4.90	-6.05	-5.50	-5.70	-5.55	-5.50	-5.50	0.00	MA
IOS(-) AT 15V,-15V	0.00	4.45	4.10	4.15	3.75	5.30	4.75	4.80	4.50	4.45	4.95	40.0	MA
ICC AT 15V,-15V	0.00	315.M	x 235.M	280.M	300.M	380.M	x 300.M	300.M	300.M	300.M	300.M	300.M	MA
+VOP AT RL=10K	12.0	15.3	15.3	15.3	15.3	15.3	15.3	15.3	15.3	15.3	15.3	0.00	V
-VOP AT RL=10K	0.00	-14.8	-14.7	-14.8	-14.7	-14.8	-14.8	-14.8	-14.8	-14.8	-14.8	-12.0	V
+VOP AT RL=2K	10.0	10.4	9.86	x 9.90	x 9.65	x 11.9	10.8	11.2	10.9	10.8	10.8	0.00	V
-VOP AT RL=2K	0.00	-7.36	x -6.95	x -7.06	x -6.31	x -8.65	x -7.85	x -8.00	x -7.40	x -7.35	x -8.25	x -10.0	V
AVS(+) AT RL=10K	4.00	11.8	14.1	12.6	13.8	13.2	12.7	14.0	12.2	12.6	12.8	0.00	V/MV
AVS(-) AT RL=10K	4.00	4.49	4.02	4.29	3.90	x 4.94	4.67	5.02	4.66	4.57	4.67	0.00	V/MV
AVS(+) AT RL=2K	4.00	780.M	x 842.M	x 800.M	x 741.M	x 2.38	x 874.M	x 886.M	x 764.M	x 794.M	x 976.M	x 0.00	V/MV
AVS(-) AT RL=2K	4.00	986.M	x 986.M	x 984.M	x 1.09	x 776.M	x 891.M	x 946.M	x 1.05	x 992.M	x 806.M	x 0.00	V/MV
AVS AT 5V,-5V,RL=10K	8.00	6.84	6.90	6.56	6.40	7.34	7.08	7.55	6.90	6.96	6.96	0.00	V/MV
AVS AT 5V,-5V,RL=2K	8.00	1.78	x 1.40	x 1.60	x 1.43	x 1.86	x 1.77	x 1.91	x 1.77	x 1.78	x 1.76	x 0.00	V/MV
SR(+) AT 10V,-10V	1.00	8.46	1.97	2.85	1.96	8.46	8.41	8.30	8.36	8.35	8.40	0.00	V/US
SR(-) AT 10V,-10V	1.00	3.97	8.97	3.75	8.96	4.86	4.08	4.00	4.00	3.94	4.12	0.00	V/US

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 4- 6 Typical Type 02 Data at 125°C.

MANUFACTURER CODE: TT; DEVICE TYPE: 153 DUAL ; TEMPERATURE: -55 DEG C ; 06 SEP 79 14:46:17

PARAMETER	LO-LIM	S01-1	S01-2	S02-1	S02-2	S03-1	S03-2	S04-1	S04-2	S05-1	S05-2	HI-LIM	UNIT
VIO(-CM) AT 20V,-4V	-7.00	-910.M	-3.33	-8.40	0.06	* -1.29	-1.07	-497.M	8.96	* 4.05	805.M	7.00	MV
VIO(+CM) AT 4V,-20V	-7.00	-1.15	-8.04	-1.09	10.4	* -800.M	-890.M	443.M	10.2	* 4.99	1.01	7.00	MV
VIO(0CM) AT 10V,-10V	-7.00	-1.03	-3.10	-8.10	0.05	* -1.08	-875.M	318.M	9.01	* 4.04	805.M	7.00	MV
VIO(0CM) AT 5V,-5V	-7.00	-1.05	-3.14	-8.05	0.08	* -1.02	-970.M	-374.M	9.06	* 4.08	1.00	7.00	MV
D-VIO/D-T FROM 25 OC	-30.0	41.6	* 20.1	-10.1	-74.1	* 8.10	-16.6	-10.7	-70.9	* -6.10	-35.1	* 30.0	UV/C
IIO(-CM) AT 20V,-4V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
IIO(+CM) AT 4V,-20V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
IIO(0CM) AT 10V,-10V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
IIO(+CM) AT 5V,-20V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+IIB(-CM) AT 20V,-4V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+IIB(+CM) AT 4V,-20V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+IIB(0CM) AT 10V,-10V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+IIB(+CM) AT 5V,-20V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
-IIB(-CM) AT 20V,-4V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
-IIB(+CM) AT 4V,-20V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
-IIB(0CM) AT 10V,-10V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
-IIB(+CM) AT 5V,-20V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+PSRR AT 5V,-10V	80.0	94.3	93.2	95.8	107.	95.5	97.6	96.1	103.	93.7	97.6	0.00	dB
-PSRR AT 10V,-5V	80.0	94.8	94.8	107.	94.8	96.5	96.5	105.	94.0	96.5	107.	0.00	dB
CMR AT 10V,-10V	80.0	100.	95.9	93.4	86.4	97.6	102.	88.1	85.9	104.	97.2	0.00	dB
IOS(+) AT 15V,-15V	-80.0	-26.0	-21.4	-25.7	-26.5	-26.9	-25.7	-27.9	-27.1	-27.7	-26.8	0.00	MA
IOS(-) AT 15V,-15V	0.00	27.4	27.0	25.0	25.0	25.3	25.6	26.5	26.4	26.7	27.0	80.0	MA
ICC AT 15V,-15V	0.00	3.96	* 3.93	* 3.88	* 3.85	* 3.76	* 3.65	* 3.81	* 3.79	* 3.68	* 3.67	* 3.50	MA
+VOP AT RL=10K	12.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	0.00	V
-VOP AT RL=10K	0.00	-14.2	-14.2	-14.2	-14.2	-14.2	-14.2	-14.2	-14.2	-14.2	-14.2	-12.0	V
+VOP AT RL=2K	10.0	14.8	14.8	14.8	14.8	14.8	14.8	14.8	14.8	14.8	14.8	0.00	V
-VOP AT RL=2K	0.00	-13.9	-13.9	-13.9	-13.9	-13.9	-13.9	-13.9	-13.9	-13.9	-13.9	-10.0	V
AVS(+) AT RL=10K	25.0	240.	210.	400.	600.	600.	511.	600.	800.	600.	750.	0.00	V/MV
AVS(-) AT RL=10K	25.0	267.	240.	800.	480.	600.	348.	615.	400.	400.	480.	0.00	V/MV
AVS(+) AT RL=2K	25.0	133.	104.	210	343.	300.	831.	303.	480.	300.	320.	0.00	V/MV
AVS(-) AT RL=2K	25.0	96.0	82.8	800.	210.	210.	800.	198.	240.	150.	170.	0.00	V/MV
AVS AT 5V,-5V,RL=10K	10.0	400.	88.9	100.	80.0	800.	133.	190.	100.	100.	121.	0.00	V/MV
AVS AT 5V,-5V,RL=2K	10.0	80.0	67.1	80.0	88.9	800.	114.	163.	100.	133.	93.0	0.00	V/MV
SR(+) AT 10V,-10V	5.00	15.8	13.3	15.8	17.8	15.8	14.9	16.4	16.7	16.1	15.4	0.00	V/US
SR(-) AT 10V,-10V	5.00	17.9	10.6	17.8	17.5	17.5	16.9	17.5	17.9	17.8	16.9	0.00	V/US

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 4-7 Typical Type 05 Data at -55°C.

MANUFACTURER CODE: TT; DEVICE TYPE: 153 DUAL , ; TEMPERATURE: +125 DEG C ; 06 SEP 79 14:46:16

PARAMETER	LO-LIM	581-1	581-2	582-1	582-2	583-1	583-2	584-1	584-2	585-1	585-2	HI-LIM	UNITS
VIO(-CM) AT 28V,-4V	-7.00	5.85	-1.08	-3.63	-976.M	-1.84	-3.75	-3.54	-8.18	3.38	-4.86	7.00	MV
VIO(+CM) AT 4V,-28V	-7.00	4.85	-1.03	-3.17	409.M	-1.14	-3.36	-8.44	-407.M	3.38	-4.38	7.00	MV
VIO(0CM) AT 16V,-16V	-7.00	4.83	-1.08	-3.48	-841.M	-1.16	-3.58	-8.88	-1.87	3.84	-4.88	7.00	MV
VIO(0CM) AT 8V,-8V	-7.00	5.48	-876.M	-3.51	-876.M	-1.86	-3.83	-3.37	-1.78	3.38	-4.66	7.00	MV
D-VIO/D-T FROM 25 OC	-30.0	28.3	4.00	-3.30	-41.7 *	1.55	-13.7	-15.4	-50.6 *	-11.1	-28.7	30.0	UV/C
IIO(-CM) AT 28V,-4V	-20.0K	-958.	-900.	-1.86K	-304.	-1.56K	-1.40K	-1.81K	-821.	-1.36K	-1.47K	20.0K	PA
IIO(+CM) AT 4V,-28V	-30.0K	-1.42K	-1.20K	-138.	-488.	-457.	-1.17K	-939.	-986.	-865.	-1.54K	30.0K	PA
IIO(0CM) AT 16V,-16V	-20.0K	-860.	-1.02K	-784.	-831.	-1.15K	-1.00K	-1.10K	-874.	-938.	-1.44K	20.0K	PA
IIO(+CM) AT 8V,-24V	-20.0K	-1.06K	-1.05K	-203.	-767.	-899.	-1.13K	-942.	-989.	-812.	-1.25K	20.0K	PA
+IIB(-CM) AT 28V,-4V	-10.0K	8.30K	4.35K	3.03K	4.20K	3.08K	6.88K	9.00K	3.30K	10.6K	9.92K	70.0K	PA
+IIB(+CM) AT 4V,-28V	-10.0K	19.6K	16.6K	14.6K	14.0K	12.3K	16.4K	20.6K	10.8K	25.8K	21.5K	100.K	PA
+IIB(0CM) AT 16V,-16V	-10.0K	14.6K	10.8K	8.95K	9.02K	7.63K	12.0K	15.0K	7.23K	18.6K	16.3K	70.0K	PA
+IIB(+CM) AT 8V,-24V	-10.0K	18.5K	15.0K	13.2K	12.3K	10.7K	15.0K	18.8K	9.81K	23.2K	20.1K	70.0K	PA
-IIB(-CM) AT 28V,-4V	-10.0K	9.25K	5.25K	4.29K	4.50K	4.64K	8.38K	10.2K	4.12K	11.9K	11.4K	70.0K	PA
-IIB(+CM) AT 4V,-28V	-10.0K	21.0K	17.8K	14.8K	14.5K	12.7K	17.5K	21.4K	11.8K	26.1K	23.0K	100.K	PA
-IIB(0CM) AT 16V,-16V	-10.0K	15.4K	11.8K	9.71K	9.65K	8.78K	13.1K	16.1K	8.21K	19.5K	17.8K	70.0K	PA
-IIB(+CM) AT 8V,-24V	-10.0K	19.6K	16.0K	13.4K	13.1K	11.6K	16.1K	19.7K	10.8K	24.0K	21.3K	70.0K	PA
+PSRR AT 8V,-16V	80.0	103.	105.	124.	95.4	110.	124.	103.	93.5	118.	106.	0.00	dB
-PSRR AT 16V,-8V	80.0	112.	110.	98.5	96.5	110.	102.	95.1	95.8	118.	105.	0.00	dB
CMR AT 16V,-16V	80.0	89.5	124.	94.3	84.8	109.	95.7	86.7	82.9	124.	93.9	0.00	dB
IOS(+) AT 15V,-15V	-80.0	-15.0	-15.4	-13.9	-14.1	-14.3	-13.5	-13.9	-14.6	-14.0	-14.1	0.00	MA
IOS(-) AT 15V,-15V	0.00	10.7	11.3	10.4	10.3	10.2	9.85	9.75	10.9	9.55	10.3	80.0	MA
ICC AT 15V,-15V	0.00	3.12 *	2.74	3.31 *	2.67	3.00 *	2.88	3.28 *	3.03 *	2.85	2.73	3.00	MA
+VOP AT RL=10K	12.0	15.3	15.3	15.3	15.3	15.3	15.3	15.3	15.3	15.3	15.3	0.00	V
-VOP AT RL=10K	0.00	-14.7	-14.7	-14.7	-14.7	-14.7	-14.7	-14.7	-14.7	-14.7	-14.7	-12.0	V
+VOP AT RL=2K	10.0	14.9	14.9	14.9	14.9	14.9	14.9	14.9	14.9	14.9	14.9	0.00	V
-VOP AT RL=2K	0.00	-14.3	-14.2	-14.2	-14.2	-14.2	-14.2	-14.3	-14.3	-14.3	-14.3	-10.0	V
AVS(+) AT RL=10K	25.0	300.	222.	343.	400.	343.	267.	343.	400.	267.	300.	0.00	V/MV
AVS(-) AT RL=10K	25.0	267.	267.	267.	353.	400.	267.	300.	300.	267.	267.	0.00	V/MV
AVS(+) AT RL=2K	25.0	218.	200.	267.	316.	300.	218.	240.	267.	240.	218.	0.00	V/MV
AVS(-) AT RL=2K	25.0	77.4	75.0	104.	117.	100.	88.9	88.9	100.	72.7	75.0	0.00	V/MV
AVS AT 5V,-5V,RL=10K	10.0	114.	100.	133.	113.	133.	114.	100.	114.	100.	88.9	0.00	V/MV
AVS AT 5V,-5V,RL=2K	10.0	86.7	88.7	88.9	87.9	78.7	78.7	80.0	86.7	81.6	81.6	0.00	V/MV
BR(+) AT 16V,-16V	5.00	16.1	15.8	15.4	16.1	15.8	15.4	15.8	15.6	14.9	14.9	0.00	V/UB
BR(-) AT 16V,-16V	5.00	18.2	19.6	17.5	17.8	17.8	16.7	17.5	17.8	16.9	16.7	0.00	V/UB

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 4-8 Typical Type 05 Data at 125°C.

SECTION V

SAMPLE/HOLD CIRCUITS
MIL-M-38510/125

TABLE OF CONTENTS

SECTION V

SAMPLE/HOLD CIRCUITS

MIL-M-38510/125

5.1 Introduction

Sample and hold circuits are becoming more and more important, especially with the growth in the fields of data acquisition and data distribution. National Semiconductor's LF198 was the first I.C. sample and hold circuit to be proposed by the JC-41 Committee for military slash sheet action. Table 5.1 shows the sample and hold circuits which were specified for MIL-M-38510/125.

Table 5-1. Table of Device Types Specified.

Device Type	Generic Type	Manufacturer	Description
12501	LF198	National	Sample & hold circuit, 10K ohm load
12501	LF198	AMD	Sample & hold circuit, 10K ohm load
12501	LF198	Signetics	Sample & hold circuit, 10K ohm load
12502	SE5537	Signetics	Sample & hold circuit, 2K ohm load

Some of the outstanding features of the LF198, which helped promote its characterization as a military device type are as follows:

1. Power supply range from +/- 5V to +/- 18 V
2. Monolithic I.C. construction
3. +/- .005% gain error
4. Low "hold" mode noise and droop
5. Wide bandwidth
6. Fast acquisition time
7. High feedthrough rejection ratio

5.2 Description of Device Types

The LF198 is a monolithic, unity gain, closed loop type sample and hold circuit. A functional schematic is shown in Figure 5-1. When this device is in the sample mode with the switch closed, the external hold capacitor charges to whatever level it takes to make the output equal to the input.

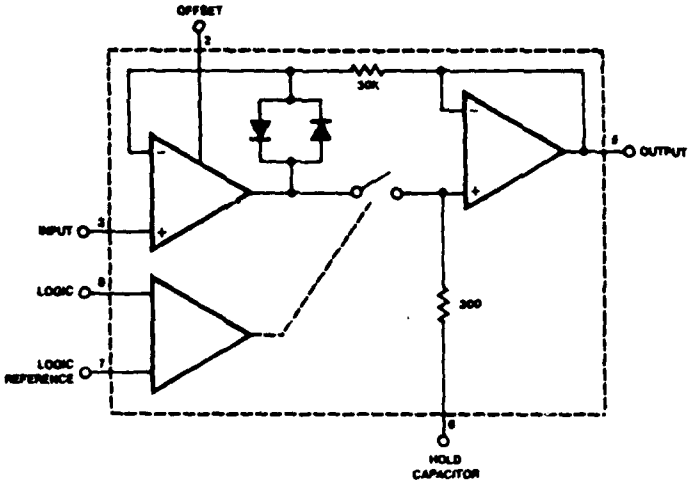


Figure 5-1. LF198 Sample Hold Circuit Functional Schematic.

The static gain error from unity is guaranteed to be within +/- .005% at 25°C and within +/- .02% over the military temperature range. Acquisition time to 0.01% accuracy is guaranteed within 25 microseconds using an external .01 uF capacitor. With a .001 uF capacitor the acquisition time is typically reduced to six microseconds.

The device is manufactured with BI-FET technology so that the best features of bipolar and J-FET transistors can be incorporated where they will do the most good. For low offset, drift and gain error the input buffer is all bipolar. The output buffer uses front end J-FETs so as to minimize "hold" mode "droop" due to input gate to capacitor leakage current. One consequent penalty of the J-FETs is that at elevated temperatures the leakage current, which doubles for each 11°C rise in chip temperature, becomes a dominant error source. A differential logic comparator driving a diode bridge performs the switch function of connecting the input buffer to the external hold capacitor upon the receipt of a sample (logic - high) command. In order to keep the input buffer active with the input signal in the "hold" mode, the back to back diodes and 30 K ohm feedback resistor are connected into the compound follower configuration. Without this feature the input buffer would go into saturation in the "hold" mode and additional time would be needed to come out of saturation when the "sample" mode was initiated.

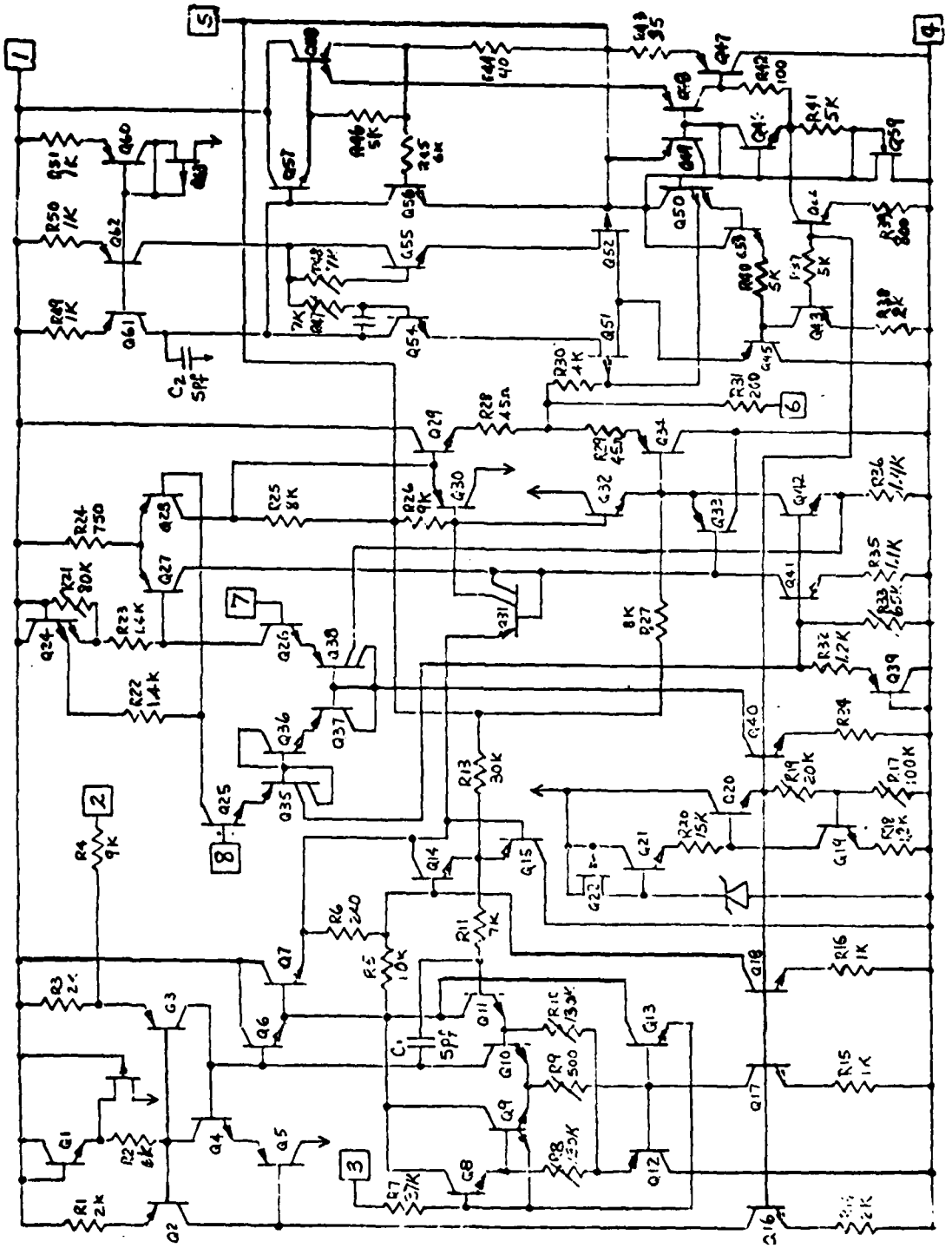


Figure 5-2. LF198 Schematic Diagram

The 300 ohm isolation resistor in series with the "hold" capacitor terminal is included for stability reasons. The penalty for this increase in stability is an increase in acquisition time and dynamic sampling error. An offset adjustment pin is provided for D.C. zeroing the input offset voltage. "Hold" mode performance of the LF198 is very dependent on the quality of the "hold" capacitor. These capacitors should have low dielectric absorption so that "creep" or hysteresis of the stored voltage is well within the allowable application accuracy.

A detailed schematic of an LF198 is shown in Figure 5-2.

The SE5537 is generically the same as the LF198, except that the output has been designed to drive up to a 2000 ohm load instead of a 10,000 ohm load. Both device types are packaged in a TO-99 metal can.

5.3 Test Development

Test Parameters

Monolithic sample and hold circuits are relatively new devices, which are not presently covered by a military slash sheet. In order to develop a test procedure for these devices GEOS first contacted the various manufacturers for recommendations. Also a preliminary MIL-M-38510 Table I was provided by the JC-41 Committee. All of the manufacturers submitted test procedures for their commercial parts. In addition, National Semiconductor presented additional ideas for a more comprehensive military device test procedure. Sample devices were procured during the same time frame, as shown in Table 5-2.

Table 5-2. Device Types Characterized.

Generic Type	S/N	Manufacturer Code	Date Code
LF198	6-48	A	7909
LF198	51-68	B	7833
LF198	74-79	C	7934
SE5537	81-90	C	7946

Analysis of the manufacturer test documentation, bench observations and GEOS-generated ideas were blended to yield a preliminary test procedure. Table 5-3 gives a list of the parameters which evolved during the characterization of the LF198 Sample and Hold circuits.

Table 5-3. Test Parameters for Characterization.

Item No	Symbol	Test Parameter
1	VIO	Input offset voltage
2	D-VIO/D-T	Input offset voltage temperature sensitivity
3	IiB	Input bias current
4	Zi	Input impedance
5	Ae	Gain error
6	VIO (ADJ +)	Input offset voltage adjustment (Pos.)
7	VIO (ADJ -)	Input offset voltage adjustment (neg.)
8	+PSRR	Power supply rejection ratio
9	-PSRR	Power supply rejection ratio
10	FRR, FRRac	Feedthrough rejection ratio
11	Zo	Output impedance
12	Vhs	"Hold" step
13	Icc	Supply current
14	Rsc	Series change resistance
15	IIH	Logic input current (high)
16	IIL	Logic input current (low)
17	IOS(+)	Output short circuit current (Pos. output)
18	IOS(-)	Output short circuit current (Neg. output)
19	IHL(+)	Hold mode leakage current (Pos. output)
20	IHL(-)	Hold mode leakage current (Neg. output)
21	ICH(+)	Hold cap. charge current (Pos. output)
22	ICH(-)	Hold cap. charge current (Neg. output)
23	VTH	Differential logic threshold voltage
24	taq	Acquisition time (.01% error)
25	tap	Aperture time
26	TR(ts)	Transient response settling time
27	TR(OS)	Transient response overshoot
28	en(H)	Noise (hold mode)
29	en(S)	Noise (sample mode)

Test Adapter

A schematic of the LF198 test adapter is shown in Figure 5-3. Relay coils and their means of excitation are not shown. Relay contacts are shown in the normally de-energized position. Most of the D.U.T. parameters are measured in the "Sample" mode. This requires that a TTL compatible "logic one" signal be applied across the mode control logic inputs. Also most parameters are measured with the input grounded and no load on the output. The output of the D.U.T. is amplified by a gain of 100 V/V before being presented to the measurement system. Most of the measured parameters are static and therefore are easily exercised and measured by an automatic tester.

An adapter sample and hold circuit is provided for the measurement of dynamic and volatile data, which would change too much during the several milliseconds of cycle time of the automatic measurement system. More details on how the different parameter tests are mechanized will be covered in subsequent paragraphs.
Several photographs of the adapter are shown in Figure 5-4.

"Sample" Mode Test Mechanizations

Table 5-4 shows the voltage conditions, relay programming, and equations for all of the automatic tests.

This table is an abbreviated version of the MIL-M-38510/125 Table III and together with the test adapter schematic gives the required detail information for each specific test.

Input common mode voltage conditions are exercised by swinging the power supplies by a voltage increment while grounding the input signal. Thus to set up the + 11.5 V input common mode condition, + Vcc is programmed for + 3.5 V and - Vcc is programmed for -26.5 V. With these supply voltages the grounded input is + 11.5 V positive with respect to the mid point voltage of the DUT (device under test).

Next in order to put the DUT in the "sample" mode, the "logic reference" pin is programmed to the DUT mid point voltage and the "logic" pin voltage is made 2.5 V higher.

The most basic parameter to be tested is input offset voltage. Since the DUT is a compound voltage follower in the "sample" mode, the output of the DUT equals the input offset voltage. Five separate conditions of power supply voltage and input common mode voltage are exercised. The next eight parameters in Table 5-3 are tested in a similar manner with slight modifications. For instance input bias current is extracted from the offset voltage measurement when 100K ohms is programmed at the DUT input. Input impedance is determined by dividing the change in bias current into the exercised 23 V input common mode voltage change. The change in offset voltage divided by the input common mode voltage change determines the gain error from unity. Similarly, the changes in offset voltage due to changes of the + Vcc and - Vcc voltage levels determine the power supply rejection ratios + PSRR and - PSRR respectively.

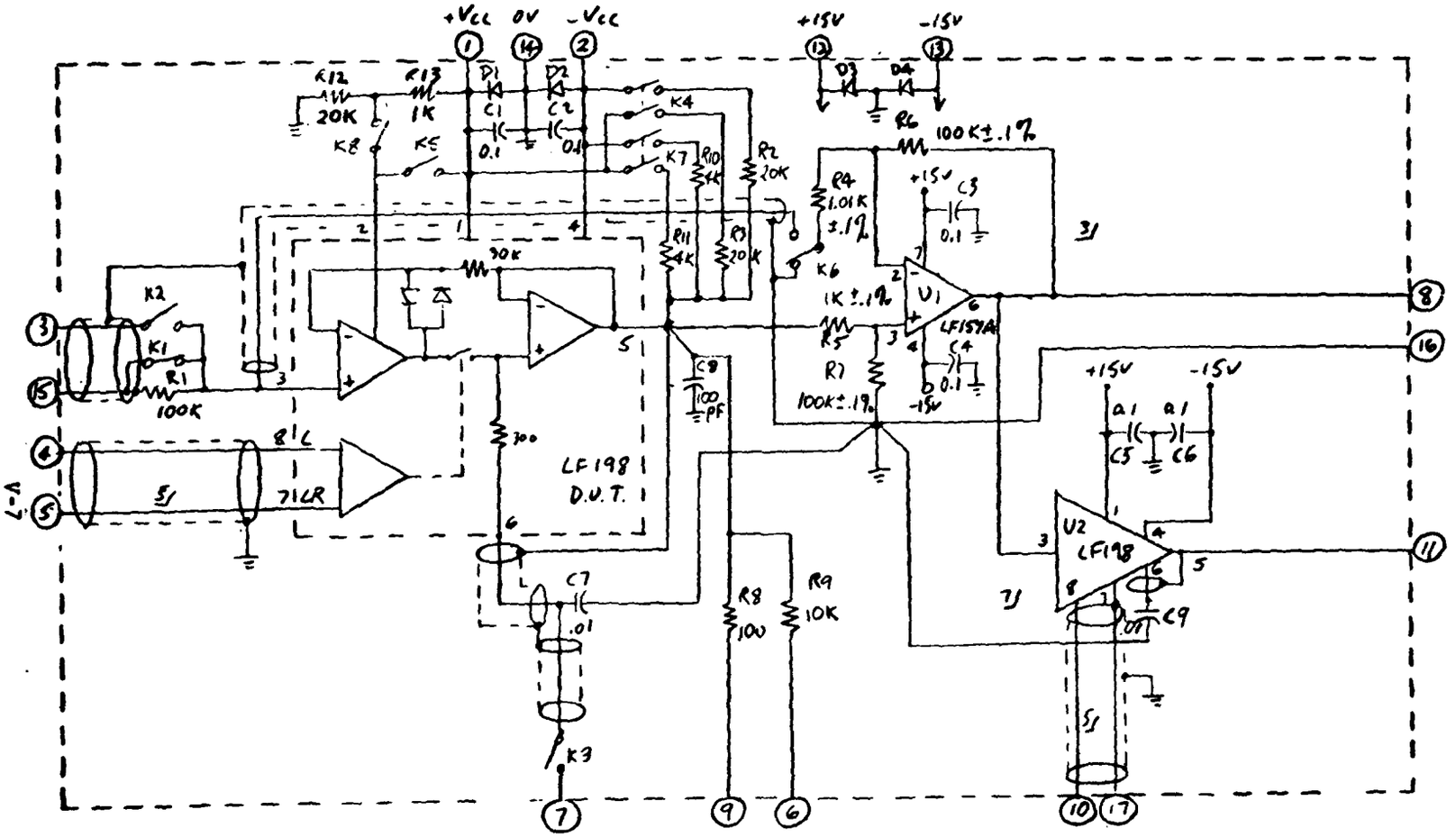


Figure 5-3. Test Adapter Schematic

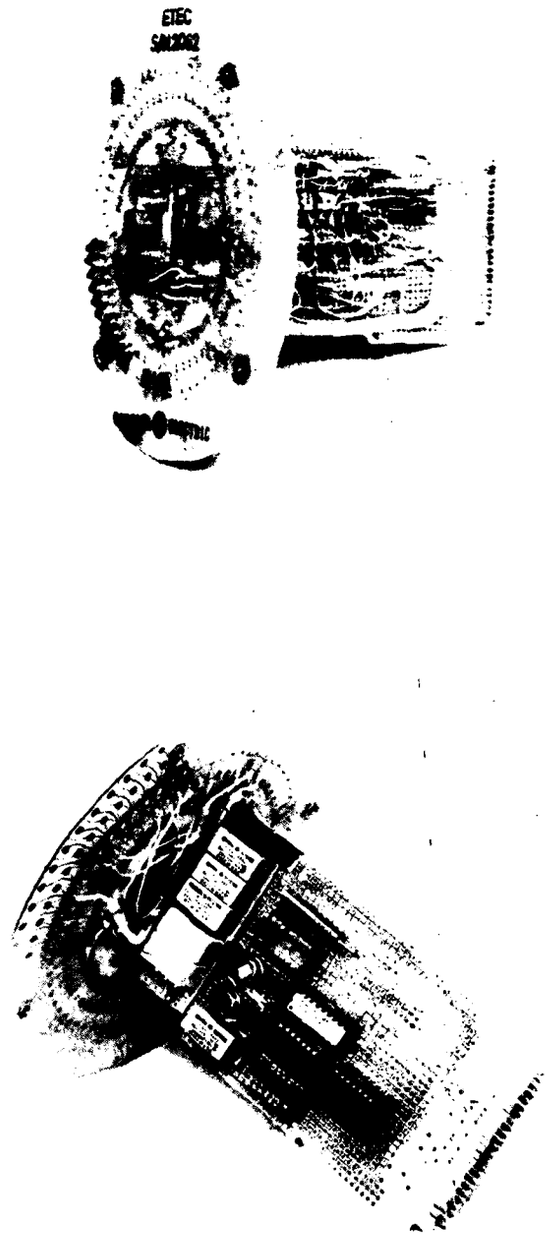


Figure 5-4. LF198 S/H Circuit Automatic Test Adapter.

Table 5-4. Device Test Mechanization

Symbol	Test No	Adapter Pin Numbers 1	2	3	4	5	6	7	Energized Relays	Measured Pin No	Value	Units	Equation 2 /	25°C Limits Min	Max	Units
	1	Apply 0V to pin 9 with D.U.T removed							None	8	E1	V	V cal = 10 E1	-2	2	mV
VIO	2	3.5V	-26.5V	open	- 9V	-11.5V	open	open			E2		VIO = 10 (E2-E1)	-3	3	
	3	26.5V	- 3.5V		14V	11.5V					E3		VIO = 10 (E3-E1)			
	4	15V	-15V		2.5V	0V					E4		VIO = 10 (E4-E1)			
	5	7V	- 3V		4.5V	2V					E5		VIO = 10 (E5-E1)			
	6	3V	- 7V		0.5V	- 2V					E6		VIO = 10 (E6-E1)			
IIB	7	3.5V	-26.5V		- 9V	-11.5V			K1		E7		IIB = 100 (E2-E7)	-1	25	nA
	8	26.5V	- 3.5V		14V	11.5V					E8		II3 = 100 (E3-E8)			
	9	15V	-15V		2.5V	0V					E9		IIB = 100 (E4-E9)			
	10	7V	- 3V		4.5V	2V					E10		IIB = 100 (E5-E10)			
	11	3V	- 7V		0.5V	- 2V					E11		IIB = 100 (E6-E11)			
ZI	12	Calculate value using data from tests 2,3,7 and 8											ZI = 0.23/IE2+E8-E3-E7I	2	-	GΩ
Ae	13	3.5V	-26.5V	open	- 9V	-11.5V	open	open	K4		E12	V	Ae = (E12-E13)/23	-.005	.005	%
		26.5	- 3.5V		4V	11.5V					E13					
	14	5V	-25V		- 7.5	-10V			K7		E14		Ae = (E14-E15)/20			
		25V	- 5V		12.5V	10V					E15					
	15	3V	- 7V		0.5V	- 2V			K4		E16		Ae = (E16-E17)/4	-.02	.02	
		7V	- 3V		4.5V	2V					E17					
VIO (ADJ+)	16	15V	-15V		2.5V	0V			K5		E18		VIO(ADJ+) = 10(E4-E18)	6	-	mV
VIO (ADJ-)	17								K8		E19		VIO(ADJ-) = 10(E4-E19)	-	-6	
+PSRR	18	18V	-18V		2.5V	0V			None		E20		+PSRR = 20log|600/(E20-E21)|	80	-	dB
		12V	-18V		- 0.5V	- 3V					E21					
-PSRR	19	18V	-12V		5.5V	0V				8	E22		-PSRR = 20log|600/(E20-E22)|			
FRR	20	15V	-15V	See Fig 8		0V			K1,K2		E23		FRR = 20 log|1150/(E24-E23)|	86	-	dB
	21	15V	-15V	timing		0V					E24		FRR = 20 log|1150/(E25-E24)|			
	22										E25		FRR = 20 log|1150/(E26-E25)|			
	23										E26		FRR = 20 log|1150/(E27-E26)|			

Table 5-4. Device Test Mechanization (Continued)

Symbol	Test No	Adapter Pin Numbers 1	2	3	4	5	6	7	Energized Relays	Measured Pin No	Value	Units	Equation 2/	25°C Limits Min	Max	Units
Zo	24	15V	-15V	See Fig 10 timing		0V 10V	-10V 0V	0V	K3	8	E28		Zo = 5 (E29-E28)	-	2	Ω
Vhs	25	3.5V	-26.5V	See Fig 11 timing		-11.5V	open	open	K6		E30 E31		Vhs = 10(E31-E30)	-2	2	mV
	26	26.5V	- 3.5V			11.5V					E32 E33		Vhs = 10(E33-E32)			
Icc	27	15V	-15V	open	2.5V	0V			None	2	I1	mA	ICC = I1	1	5.5	mA
Rsc	28			0V				0V	K1,K2,K3	7	I2 I3		RSC = 400/(I3-I2)	100	400	Ω
IIH	29 30	8.5V	-21.5V	open	5.5V 0V	0V 5.5V	open	open	None	4 5	I4 I5	uA	IIH = I4 IIH = I5	0	10	
IIL	31 32	21.5V	- 8.5V			0V				4 5	I6 I7		IIL = I6 IIL = I7	-1.0	1.0	
Ios(+) Ios(-)	33 34	15V	-15V	10V -10V	2.5V	0V			K1,K2	9	I8 I9	mA	Ios(+) = I8 Ios(-) = I9	-30 -	- 30	mA
IHL(+)	35	3.5V	-26.5V	See Fig 12 timing		-11.5V			None	8	E34 E35	mV	IHL(+) = (E35-E34)	-100	100	pA
IHL(-)	36	26.5V	- 3.5V	(dt = 100ms)		11.5V					E36 E37		IHL(-) = (E37-E36)			
ICH(+)	37	15V	-15V	11.5V	2.5V	0V		9.5V	K1,K2,K3	7	I10	mA	ICH(+) = I10	-	-3	mA
ICH(-)	38			-11.5V				-9.5V			I11		ICH(-) = I11	3	-	
VTH(H)	39			- 2V	2.0V			0V			I12		VTH(H) ≤2V if I12 ≥ 1mA	1	-	
VTH(L)	40			- 2V	0.8V						I13	uA	VTH(L) ≥0.8V if -10<I13<10mA	-10	10	uA

Supply current is measured in the "sample" mode because its value is higher here than in the "hold" mode.

Series charge resistance is measured as a static parameter by determining the change in charge current for a 400 mV change across it. The hold cap terminal is grounded. Dynamic sampling error (DSE) is proportional to series charge resistance according to the equation:

$$DSE = K * Rsc * Ch * SR$$

where

K = proportionality constant

Ch = "hold" capacitance in μF

SR = Input Signal Slew Rate in volts/μsec

Rsc = series change resistance in ohms

By keeping the applied voltage change small, the current is not at the full slew rate limit.

The tests for ICH(+) and ICH(-) charge current are similar to the Rsc test except that the common mode voltage technique with a grounded input is used. These two tests determine the ability of the DUT to supply source and sink current out of the "hold cap" terminal to ground. The slew rate interval of acquisition time for a given "hold" capacitor size is dependent on these charge currents. Output short circuit current is measured and checked against a maximum limit to verify that internal device protection exists.

"Hold" Mode Test Mechanizations

All of the "hold" mode tests are performed using an external .01 uF Teflon capacitor. This capacitor is chosen for low dielectric absorption. Also its size is a definite test condition which will contribute to the DUT data values for feedthrough rejection ratio, "hold" step and acquisition time. This capacitor has a shield connected to the output in order to minimize leakage and undesired feedthrough coupling.

For the feedthrough rejection test, the DUT is first made to sample 0V. Next the DUT is commanded to the "hold" mode and the input is stepped from 0V to + 11.5 V to 0 V to - 11.5 V and back to 0V.

For each input condition, the output is measured and the data value is stored. The difference between adjacent data values for each of the four transitions is used to calculate static feedthrough rejection. As with the other tests the amplifier gain of 100 and the measurement range

is factored into the parameter equation. It should be emphasized that test adapter and test socket capacitance between pins must be rigorously minimized in order that the feedthrough rejection value reflects that of the DUT and not the tester.

Output impedance is determined by driving the output with 10 volts through a 10 K ohm resistor, while shorting the "hold" capacitor terminal to ground. The measured output voltage divided by the applied current is calculated to determine Zo. Both polarities of the 10 volt signal are applied.

In switching from the "sample" mode to the "hold" mode there is a shift in the output voltage called "hold" step. This parameter is determined for both input common mode end point conditions.

Hold mode leakage currents IHL(+) and IHL(-) correspond to the BI-FET input bias current of the output buffer for both end point common mode voltage conditions. Since these picoampere currents are too small for direct machine measurement, the test is performed by measuring the output "hold" mode voltage droop over a 100 millisecond interval. The leakage current is then calculated by I = C (D-V/D-T).

At 125°C where the leakage current can increase 1000 times its 25°C value, the droop interval time is reduced to 10 milliseconds. In order to improve the time resolution of the measurement, the adapter sample and hold circuit is used to capture the data values for the measurement system. For most parameter measurements the characterization and recommended "slash" sheet methods are identical. One exception to this, however, is with regard to differential input logic threshold voltage. For characterization it is necessary to know the exact threshold level at which the DUT changes its operating mode. This was done by applying a differential logic voltage and then measuring the "hold" capacitor terminal current. After the measurement the test voltage was incremented and repeated. The differential logic voltage at which the current changed from less than 10 microamperes to more than one milliampere is the desired threshold voltage. In the "slash" sheet procedure it is only necessary to test that at VTH = 0.8 V, the device is in the "hold" mode and that with VTH = 2.0 V the device is in the "sample" mode.

5.3 Test Development (continued.)

A complete characterization of the LF198 Sample/Hold circuit requires an automated measurement of aperture and acquisition times over the full military temperature range (-55oC to +125oC). Since both measurements are made to within 0.01% (i.e. 1 mV out of a 10 volt step) the mechanization of these tests involves some unique problems that may effect the accurate measurement of the parameter in an automated test system environment. Therefore, it is important that proper grounding and shielding techniques be used to insure a relatively noise-free operation.

Acquisition Time

Figure 5-5 shows the circuit configuration used in the mechanization of the acquisition time test for the LF198 Sample/Hold circuit. Acquisition time is defined as the time required to acquire a new analog output voltage to a specified accuracy with an input step of 10V. This includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode. The X100 error amplifier (LF157) is configured differentially so as to reflect the difference between the input to the device under test and its output. Applying a variable width logic pulse to the Sample/Hold input some fixed delay after a 10V step has been applied to the analog input will cause the output to assume some particular value. When this value is 99.99% of the applied input level (i.e. 1 mV difference between input and output after removing offsets) the width of the logic pulse is the acquisition time of the device. Since the droop of the device is relatively high at +125oC it can be a significant error factor in attempting to make the measurement. To compensate for this a Sample/Hold device has been added to the adapter to facilitate acquisition of the error amplifier output as quickly after the sample to hold transition as possible. Figure 5-6 depicts the relative timing of the required stimulus signals. The automatic implementation of the acquisition time measurement is described in the flow-chart shown in Figure 5-7. The measurement made the first time through the loop (i.e. M = 0) is the steady state measurement labeled Vss. This measurement is made after applying a generous Sample/Hold logic pulse (PW = 50.0 usec) and includes all offsets such as the device DC offset and hold step voltages, the DC offset of the X100 error amplifier, and the DC offset and hold step voltages of the adapter Sample/Hold. This offset term will then be subtracted from each subsequent measurement. The pulse width (PW) applied to the mode control input of the device is decreased by 0.1 usec and the procedure repeated until the error output Ve first exceeds 100mV at which point the pulse width is saved as the acquisition time of the device.

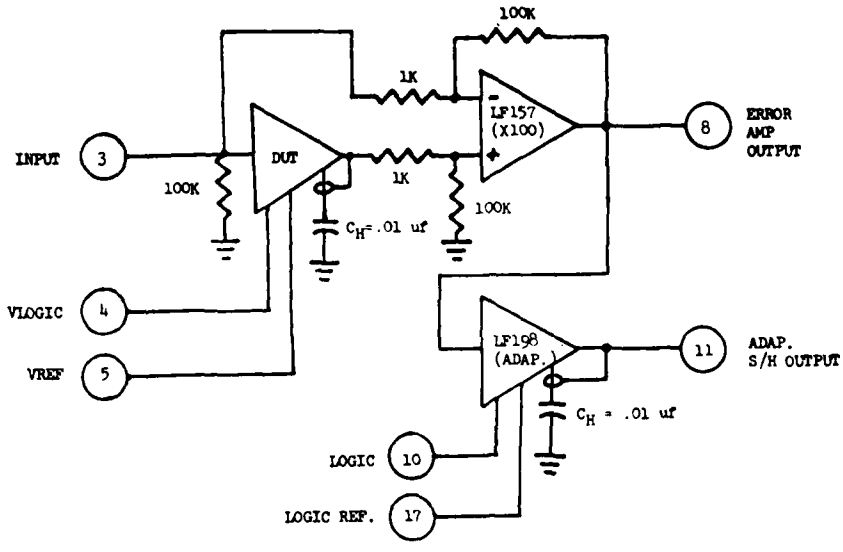


Figure 5-5. Acquisition Time and Aperture Time Test Circuit

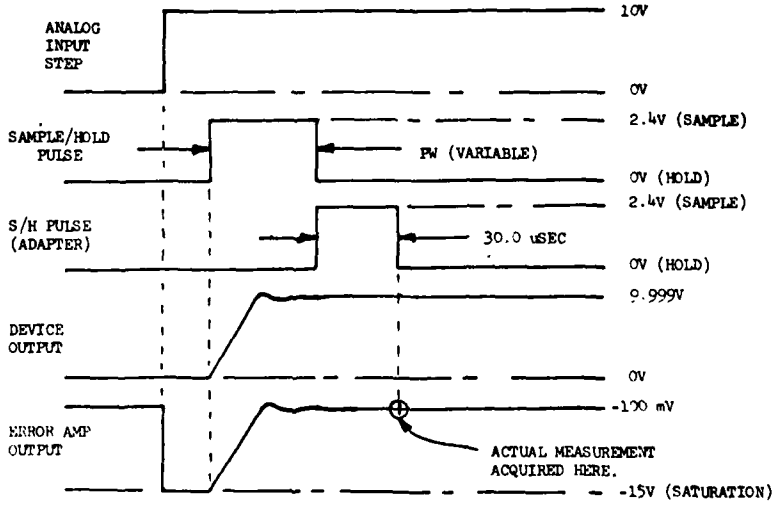


Figure 5-6. Acquisition Time Test Timing Diagram

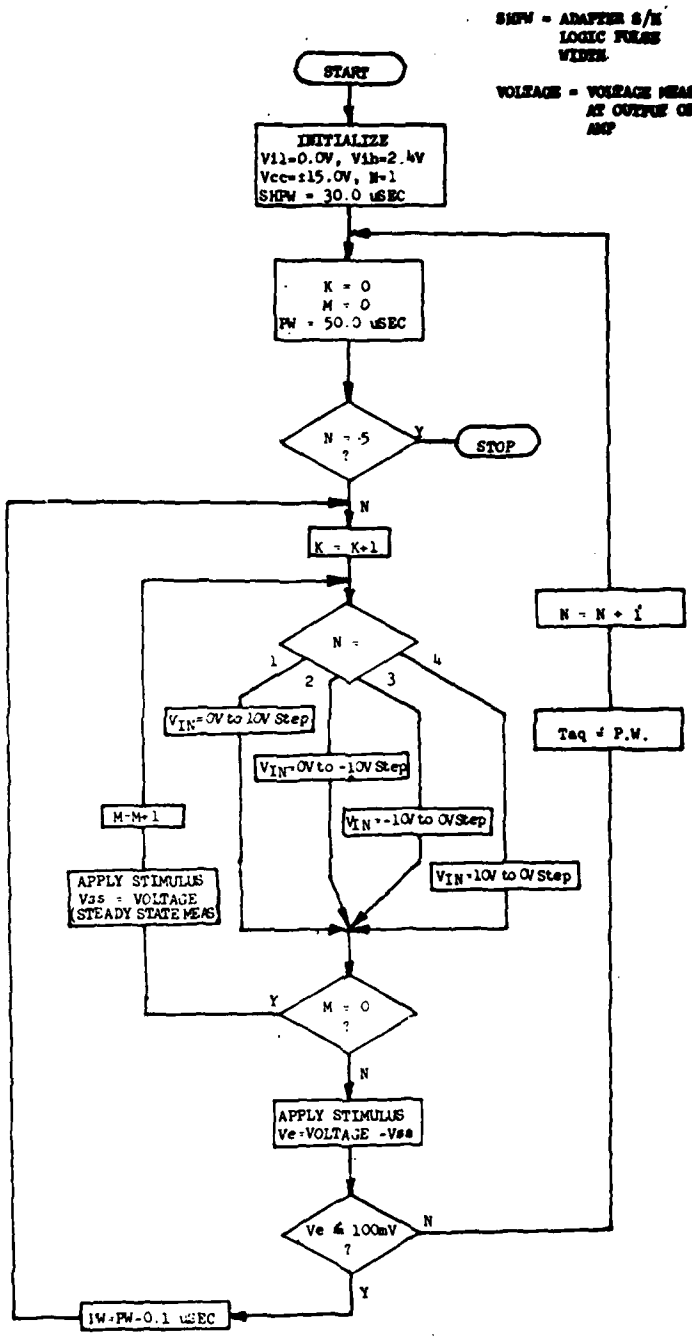


Figure 5-7. Acquisition Time Flow Chart

Aperture Time

The aperture time measurement is accomplished in the same manner as acquisition time. By definition, aperture time is the delay required between the "hold" command and an analog input transition, so that the transition does not affect the held output. The circuit configuration used to obtain an aperture time measurement is the same as that used for acquisition time but the stimulus is different. By applying a "sample" to "hold" transition at the mode input of the device and then applying a 10 volt step to the analog input after some particular delay, the effect on the device output can be monitored at the output of the X100 error amplifier. Figure 5-8 represents the required relative timing of the stimulus to achieve these results. The delay, Del, is initially set at 1 usec to obtain the steady state offset value, Vss. Given a sufficiently wide delay, the output is relatively unaffected by the analog step because the device has already achieved a "hold" status prior to its application. This delay is then decreased by 5 nsec each time and a measurement made until the level on the output exceeds 1 mV (0.01% of 10V). This delay is then stored as the aperture time of the device. A more detailed description of the iteration is presented in the aperture time flow-chart, Figure 5-9.

Bench Test Development

Although the main objective of the characterization testing was to develop automatic parameter tests, a certain amount of bench testing was necessary. Bench tests were used to verify parameter measurements made on the S-3260 and to obtain dynamic type data, which could not be readily automated.

A bench test circuit is shown in Figure 5-10. With S1 in the "Normal" position, most of the static tests could be set up to verify S-3260 data measurements. With S1 in the "TAQ/TAP" position special input signals could be generated to implement the acquisition time and aperture time tests.
The acquisition time bench test also used the clamped current to voltage converter which is shown separately in Figure 5-11 along with typical test waveforms. When a 10 volt pulse is applied to the DUT analog input in the "sample" mode, the "hold" capacitor is changed to the same voltage after a certain time delay.

By monitoring the "hold" capacitor current with the I/V converter and an oscilloscope, one is able to make a direct measuremement of acquisition time. In order for the measurement to be valid a number of test conditions must be established because they all have a direct bearing on the resulting data. These conditions are as follows:

1. Input step = 10V
2. Capacitor value = .01 uF +/- 10%
3. Settling error = 0.01% of 10V = 1 mV

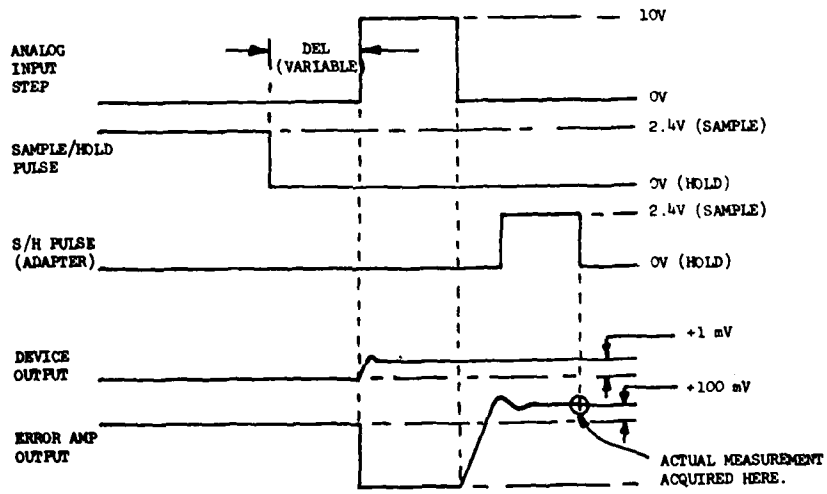


Figure 5-8. Aperture Time Test Timing Diagram

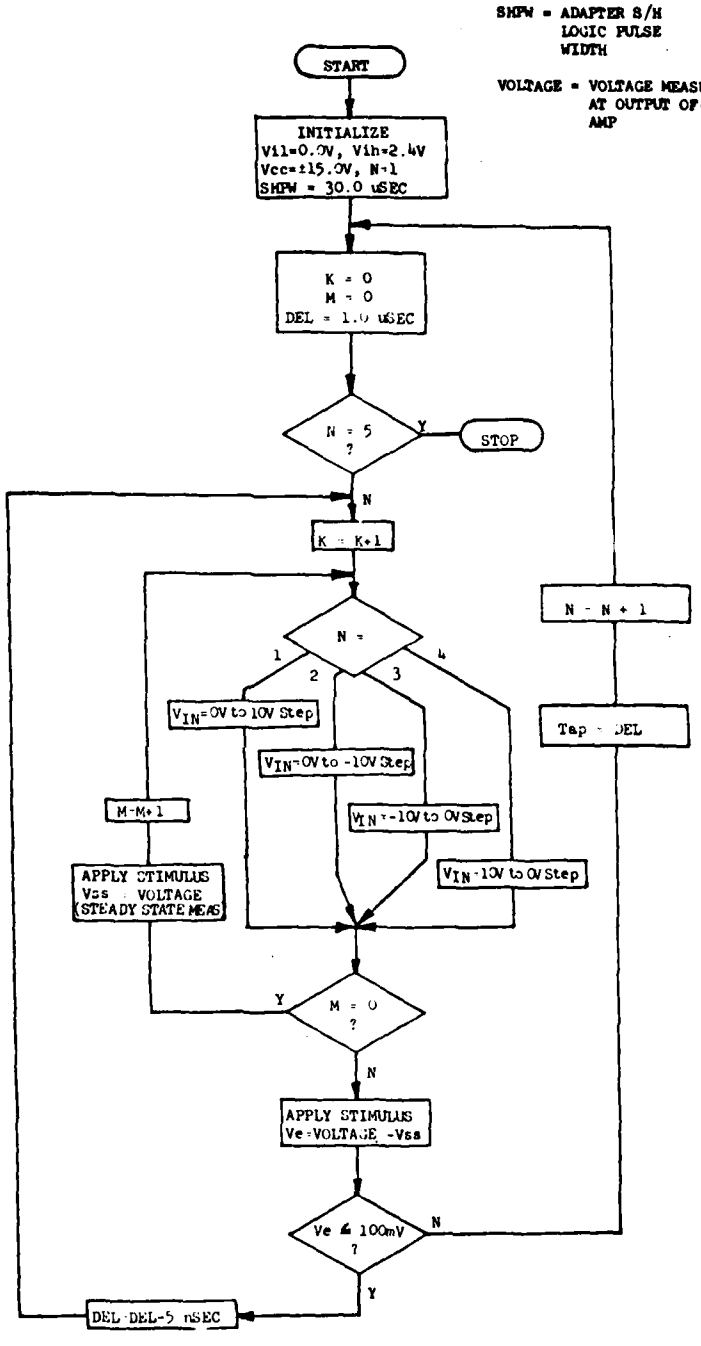


Figure 5-9. Aperture Time Flow Chart

Bench Test Development (continued)

When the hold capacitor voltage is 1 mV from final value, the charge current is Ich = dV/RSC = 1 mV/300. The corresponding I/V converter output is eo = Rf•Ich = (3000)(1 mV/300) = 10 mV. Thus acquisition time to .01% is the I/V output pulse width from the leading edge to the trailing edge at 10 mV from the final "no current" value. It is significant to observe from the waveforms in Figure 5-11 that the sample/hold output settles long before the "hold" capacitor current stops flowing.

The aperture time bench test was set up by applying the signals shown in Figure 5-12 to the DUT. It should be noticed that the DUT is commanded to the "sample" mode when the input Vin is at 0V. Also, before Vin is switched to 10V or -10V the logic input is switched to the 0V "hold" state. As long as there is an adequate delay between the sample to hold transition and the 10V input step, no effect is seen at the DUT output. However, as the delay is reduced a slight bit of input to output coupling or "sampling" is eventually observed. The delay corresponding to one millivolt of sampling is the required aperture time. Application of this definition means that if a large input transition occurs after the aperture time delay there will be no disturbance to the "hold" output voltage. This is so because the internal mode switching will have put the DUT in the "hold" mode before the input transient is applied. Feedthrough effects will still occur long after the aperture time delay. Hold mode settling time can be measured along with the aperture time test since the settling time interval follows the aperture time. It is sufficient, however, to observe the output response with an oscilloscope while grounding the analog input and switching the logic input from "sample" to "hold". The transient interval for the output to settle is the hold mode settling time. The importance of this specification is that in an application both the aperture time and settling time intervals should have expired before commanding an A/D converter to begin a conversion.

Bench tests were also used to determine the transient response, noise, and a.c. feedthrough characteristics of the devices.

The transient response test is performed to verify the stability of the devices. Originally, this test was done at zero input common mode voltage (i.e. with +/- Vcc = +/-15 V and the input signal referenced to ground). Since some devices tended to be more unstable at the common mode voltage extremes it was decided to specify the test under these more comprehensive conditions. Characteristically, there are three poles in the transfer function of the sample and hold circuit. Two of these poles are associated with the I.C. compound follower and the third dominant one is caused by the "hold" capacitor and the I.C. series charge resistance. The shape of the transient response is affected by these poles. Figure 5-13 shows several transient response waveshapes.

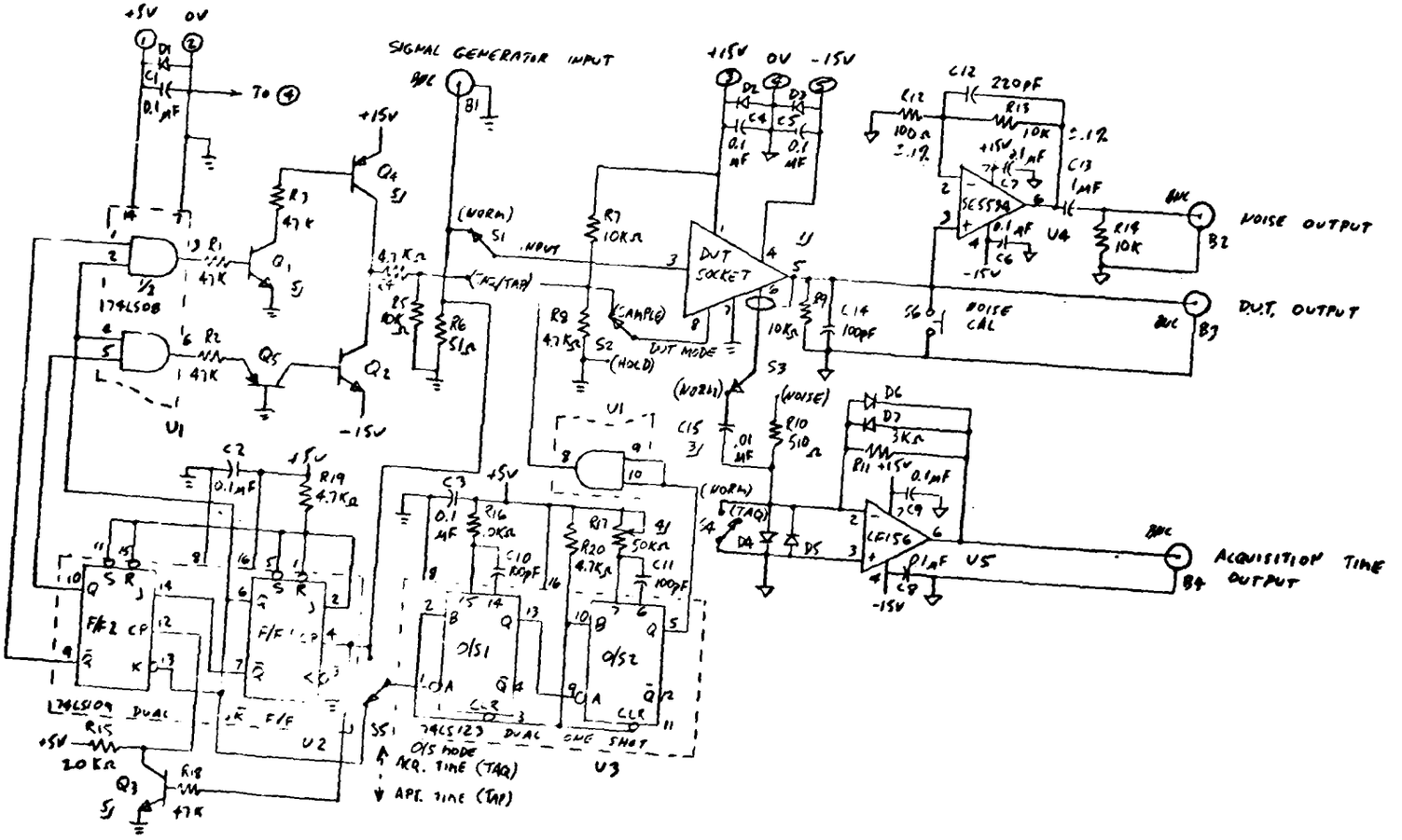
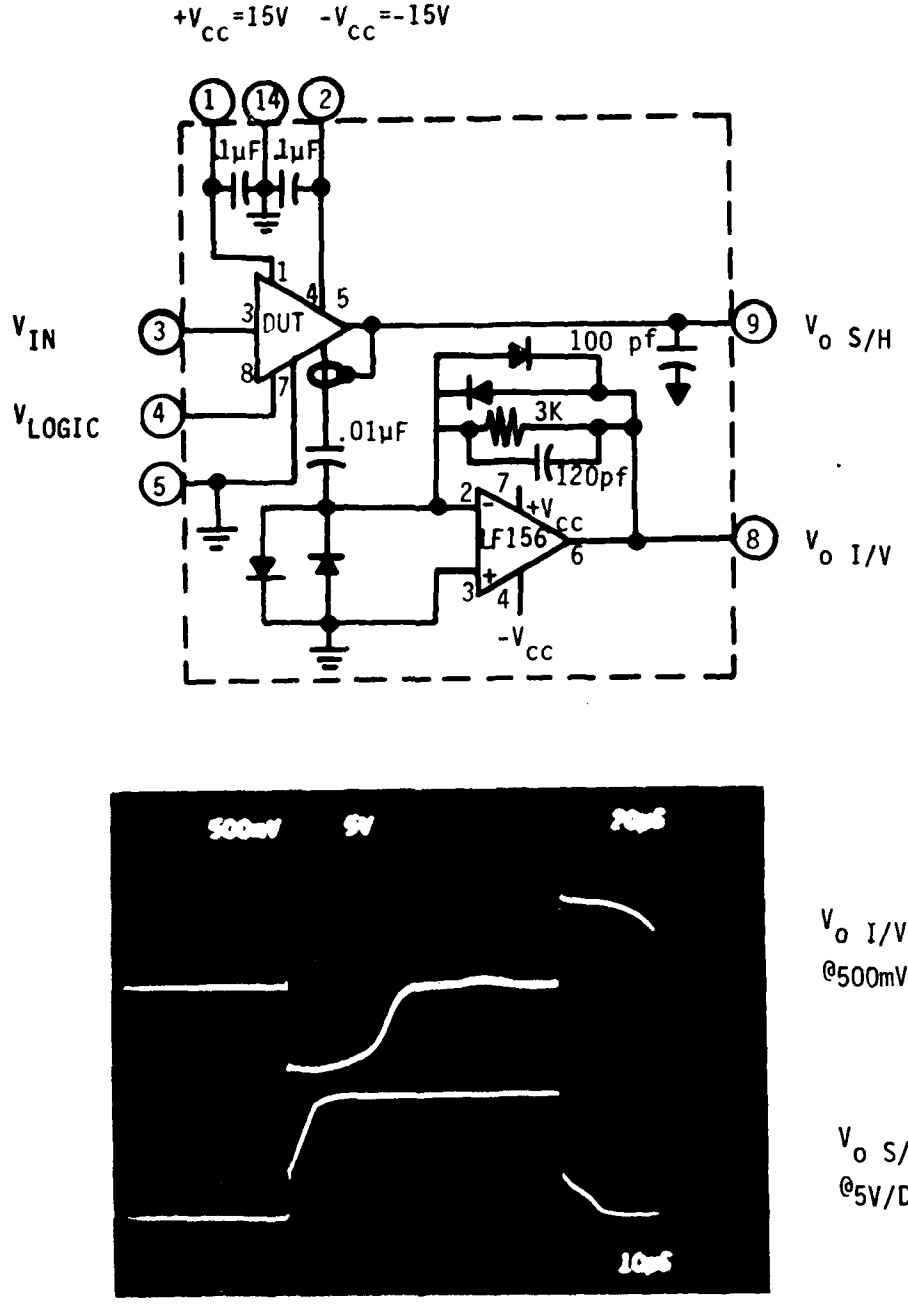


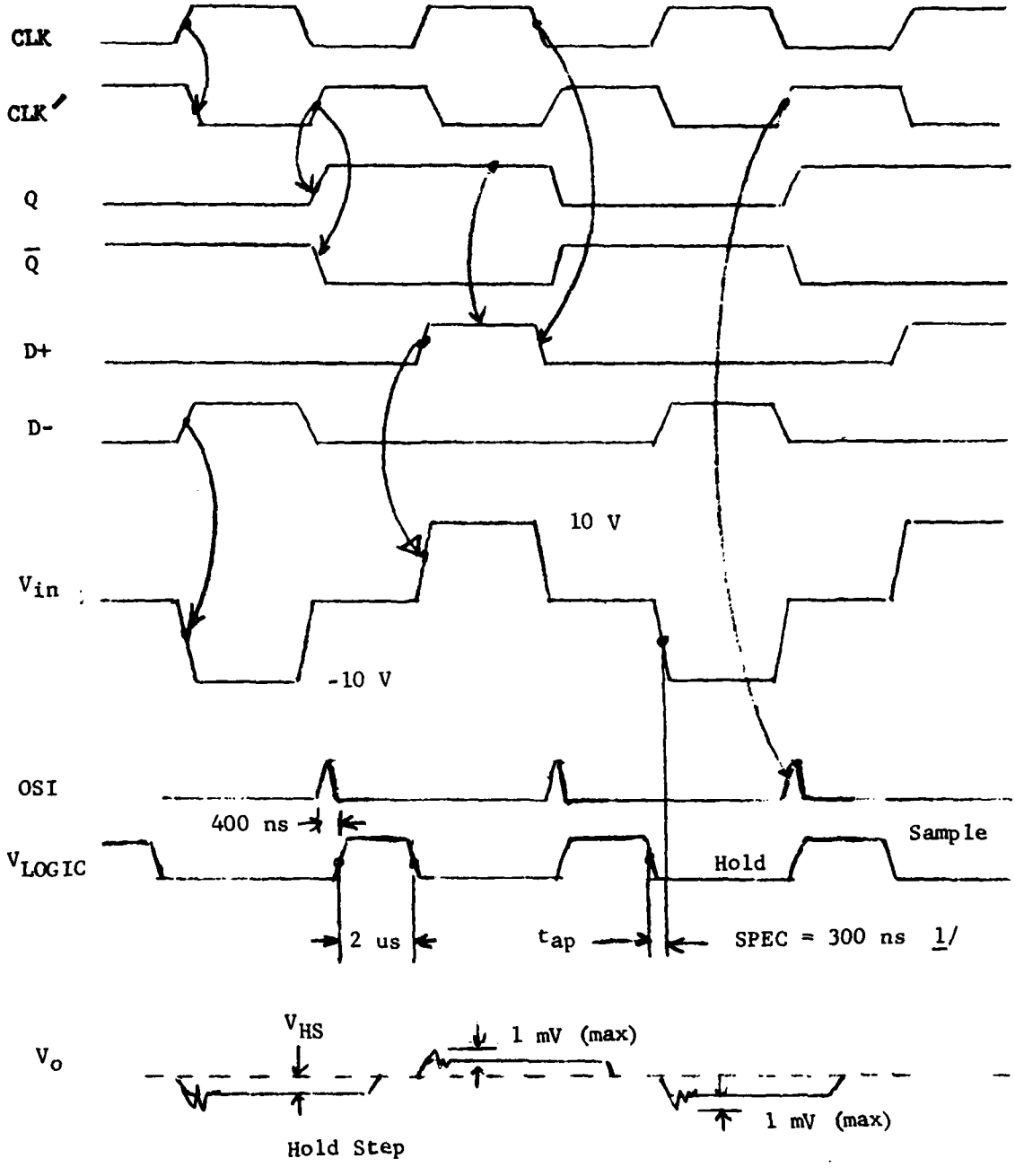
Figure 5-10. LF198 S/H Bench Test Circuit



Vo I/V
@500mV/DIV

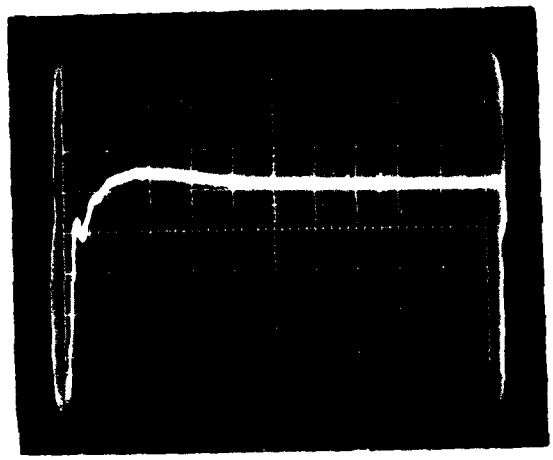
Vo S/H
@5V/DIV

Figure 5-11. Acquisition Time Test Circuit and Output Waveforms

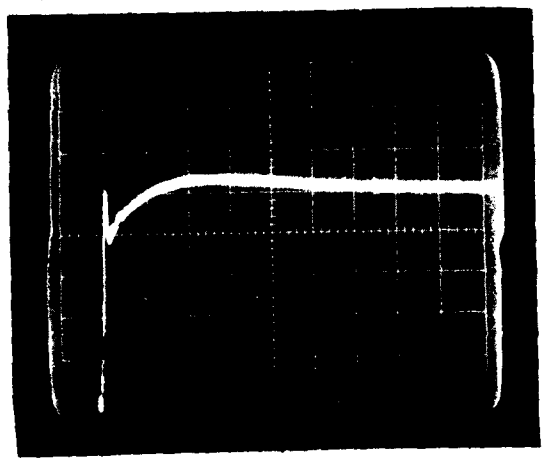


1/ The clock frequency and logic pulse width are adjusted so that there is a 300 nanosecond delay from the logic Hold transition to a ± 10 V input transition. For these conditions the effect on the output shall be less than 1 mV. Laboratory instruments may be used to apply similar input conditions.

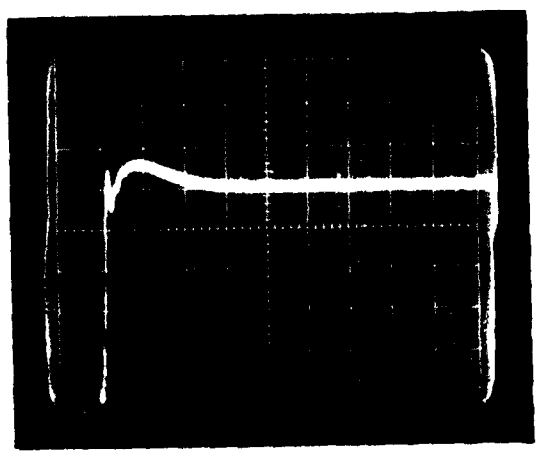
Figure 5-12. Aperture Time Test Waveforms



Manufacturer B
C_H = .01 uF
Vert: 10 mV/div
Horiz: 1 us/div
TR (OS) = 6%
TR (tr) = 550 ns

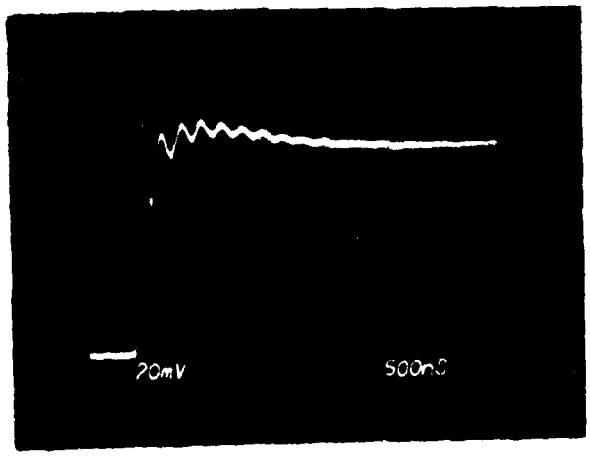


Manufacturer C
C_H = .01 uF
Vert: 10 mV/div
Horiz: 1 us/div
TR (OS) = 6%
TR (tr) = 80 ns

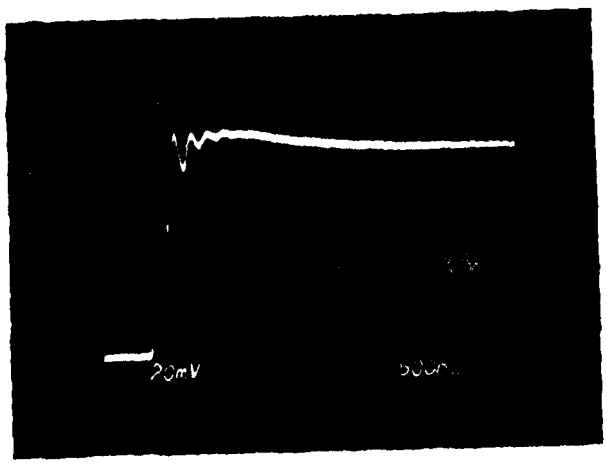


Manufacturer C
C_H = .001 uF
Vert: 10 mV/div
Horiz: 1 us/div
TR (OS) ≈ 12%
TR (tr) ≈ 80 ns

Figure 5-13. LF198 Transient Response vs Manufacturer and Hold Capacitor Size.



Manufacturer A
VCM = + 11.5 V
C_H = .001 uF
Vert: 20 mV/div
Horiz: 500 ns/div
TR (OS) = 18%
TR (ts) = 1.12 us



Manufacturer A
VCM = - 11.5 V
C_H = .001 uF
Vert: 20 mV/div
Horiz: 500 ns/div
TR (OS) = 23%
TR (ts) = 0.52 us

Figure 5-14. LF198 Transient Response vs Common Mode Voltage.

Bench Test Development (continued)

It can be observed that each response waveshape has an initial fast response peak followed by a slower dominant response peak. Depending on the sample and hold circuit's manufactured design characteristics, the initial peak may be below or above the steady state value. Also in some designs this peak is below 0.9 Vss. For this situation a conventional transient response rise time measurement becomes ambiguous. This problem was resolved by specifying settling time to 10% of final value, TR(ts) instead of rise time, TR(tr). Also, the "hold" capacitor size was reduced from 0.01 uF to 0.001 uF. Figure 5-19 shows how input common mode voltage affects the response of a typical device. An interesting observation from this figure is that although the negative common mode situation has the largest overshoot, its characteristic is more stable than the positive common mode situation. According to the proposed transient response specification, any high frequency ringing should be over within one microsecond. On this basis the device is unstable at the positive common mode condition but stable at the negative common mode. It should be mentioned that the transient response characteristic is very much dependent on capacitive loading and the specification sets this at 100 pF.

The test circuit for noise started out with the SE5534 op amp circuit shown in Figure 5-10. The SE5534 is designed for low noise applications. In using this circuit to measure DUT (10 Hz to 10 kHz) broadband noise, it was determined that typical LF198 noise is so low, that an additional gain stage of 100 V/V should be cascaded with the existing 100 V/V stage. With this modification the amplified broadband noise is of sufficient magnitude to be measured by a true rms voltmeter on a 100 mV full scale range. The noise amplifier has an effective "brickwall" bandwidth of 10 Hz to 10 KHz.

A.C. feedthrough rejection is measured with a 20 Vpp sine wave at 1 kHz. "Hold" mode observations of typical devices, even at 125°C, showed very good rejection of the applied A.C. signal. Typical output signals were under 0.5 mVpp. An interesting observation, however, is that when the input signal exceeded the common mode range, the feedthrough would increase dramatically.

Tester Correlation

Considerable effort was expended to correlate all of the measurements. Past experience has shown that "the data looks good!" is a bad criteria for certifying a measurement technique and the associated measuring instruments. For a particular parameter such as feedthrough rejection "good looking data" can be good for the wrong reasons. If the 10 volt analog input signal is not applied to the DUT because a test relay is not picked up, the small "feedthrough" output will look very good indeed! This problem actually happened and caused a first data run to be scrapped.

Also if a particular measurement is made on the wrong range because of an auto ranging error it is possible to have good looking data. In this latter situation, however, the real data is literally buried in the data value that is recorded and any resemblence of one to the other is coincidental.

Signetics Corporation provided GEOS with two devices and associated parameter data. These were used as correlation standards to check GEOS automatic and bench data. In most cases a three point check was made and any differences were resolved with another check. Much testing was done before the measurement system was considered qualified to perform the characterization testing.

5.4 Test Results and Data

Thirty-seven (37) devices from three manufacturers were tested on GEOS' Tektronix S-3270. Each device was sequentially tested at 25°C, -55°C and 125°C. The data was recorded in several different forms as follows:

1. Individual device measurements at all temperatures.

2. Ten device groups of data at each temperature.

3. Parameter histograms at each temperature.

This 144 page collection of data was published in September 1980 for RADC and the JC-41 Committee in a handbook entitled:

Characterization Data for MIL-M-38510/125
Sample and Hold Circuits (LF198 & SE5537)

Selected data sheets are shown in this report as follows:

Table 5-5. Typical Mfr. Code A Device Data Sheet.

Table 5-7. Typical Mfr. Code A Device Data Sheet.*

Table 5-8. Typical Mfr. Code A Device Data Sheet.*

Table 5-9. Typical Mfr. Code B Device Data Sheet.*

Table 5-10. Typical Mfr. Code B Device Data Sheet.*

Table 5-11. Typical Mfr. Code B Device Data Sheet.*

Table 5-12. Typical Mfr. Code C Device Data Sheet.*

Table 5-13. Typical Mfr. Code C Device Data Sheet.*

Table 5-14. Typical Mfr. Code C Device Data Sheet.*

Table 5-15. Mfr. Code A Devices at 25°C.*

Table 5-16. Mfr. Code B Devices at 25°C.

Table 5-17. Mfr. Code C Devices at 25°C.*

Table 5-18. Mfr. Code A Devices at 125°C.*

Table 5-19. Mfr. Code B Devices at 125°C.*

Table 5-20. Mfr. Code C Devices at 125°C.*

Table 5-21. Mfr. Code A Devices at -55°C.*

Table 5-22. Mfr. Code B Devices at -55°C.*

Table 5-23. Mfr. Code C Devices at -55°C.*

* This data sheet is contained in the Appendix.

Selected parameter histograms are shown as follows:

Figure 5-15. Offset Voltage at 25°C.

Figure 5-16. Gain Error at 25°C.

Figure 5-17. Feedthrough Rejection at 25°C.

Figure 5-18. Hold Capacitor Leakage Current at 25°C.

Figure 5-19. Acquisition Time at 25°C.

Figure 5-20. Aperture Time at 25°C.

Bench data is tabulated as follows:

Table 5-24. Transient Response Data.*

Table 5-25. Broadband Noise Data.*

Table 5-26. Hold Mode Settling Time Data.*

All of the automatic and bench data is summarized in the bar graphs of Table 5-6. This last table is very convenient for comparing the data distributions to the initial limits recommended by the JC-41 Committee. Potential problem areas can then be examined in more detail on the individual parameter histograms.

5.5 Discussion of Data

The characterization data was carefully reviewed to determine how well it complies to the proposed JC-41 limits. The following discussion seeks to explain on a parameter by parameter basis the characteristics of the LF198 and SE5537 Sample and Hold circuits. Table 5-26 shows the relationship between the data and the initial limits.

Limit changes were recommended even though this statistical sample of 37 parts from three manufacturers is very small. These proposed limits are shown in MIL-M-38510/125 Table I at the end of this report.

Input Offset Voltage (VIO)

VIO data for all vendors is well behaved. Distributions are normal for all common mode values over the full military temperature range. All data is well within the proposed limits of $\pm$ 3 mV and $\pm$ 5 mV at 25°C and -55°C/125°C respectively. No limit change is recommended.

Input Bias Current (IIB)

The input bias currents for all vendors are relatively unaffected by changes in common mode conditions and are distributed reasonably well over the common mode range. Magnitudes of IIB over the military temperature range are well within the specified limits, therefore, no limit changes are recommended. IIB current decreases with increasing temperature because the input transistor current gain goes up at approximately 0.3%/°C while the quiescent collector current is held constant by the input stage constant current source.

Input Impedance (Zi)

Input impedance is not a directly measured parameter but is derived as dVcm/dIIB. Zi is therefore distributed over temperature in the same manner as IIB. Large leakage currents swamping out the input bias currents at + 125°C account for the distribution crowding the specified minimum limit at that temperature but no limit change is recommended.

Output Impedance (Zo)

The distribution of output impedance data is relatively normal throughout the military temperature range and all data are well within specified limits. Temperature extremes (i.e. -55°C and + 125°C) affect the distribution of this parameter very slightly.

Series Charge Resistance (Rsc)

Data distributions for series charge resistance are divided into two distinct groups. Vendor groups A and C are distributed around the nominal 300 ohm value whereas Vendor group B is distributed around 150 ohms. Data distributions are relatively unaffected by temperature with the exception of an approximate 0.5 ohm/^{o}C shift with temperature. (i.e. Rsc is directly proportional to temperature.) All values fall well within the specified limits.

Gain Error (Ae)

Since the gain error distribution shows only negative values, it appears that loop gain is more dominant than common mode rejection in the quality of this parameter. The gain error from unity is excellent for these devices.

Offset Voltage Adjustment (VIO-ADJ(+), VIO-ADJ(-))

VIO-ADJ(+) presents a fairly normal distribution over the full temperature range and at + 25^{o}C the mean falls at approximately the middle of the 6 mV to 30 mV limit range. VIO-ADJ(-) on the other hand displays a wide, almost random distribution that distinguishes between at least two vendor types. Vendor Code C devices fall around the - 6 mV upper limit. Since this condition can be remedied by minor adjustments to the VIO-ADJ Network, limit changes as a means of correcting this marginal condition are not recommended.

Power Supply Rejection Ratio (+PSRR, -PSRR)

Power supply rejection ratio for all vendors exceed the minimum specified limit over the full military temperature range. -PSRR tended to be higher, in general, than +PSRR.

Feedthrough Rejection Ratio (FRR)

Feedthrough rejection data for all transitions are represented by relatively normal distributions. The mean value for all devices is approximately 92 dB as an average. As was confirmed during the correlation procedure temperature has essentially no effect on the data since feedthrough is a function of the capacitive coupling between the input and the hold capacitor. The data is stable and meets the minimum specified limits. The step input used has been reduced from a 15 V step to an 11.5 V step in order to be within the *common mode* voltage range of the device.

Hold Step Voltage (Vhs)

This parameter was measured at both common mode voltage extremes. Although most of the data is within the specified limits, the distribution tends to be negative. Hold step is also sensitive to parasitic capacitive coupling.

Supply Current (Icc)

Supply current data is split into two distinct groups with vendor codes A and B together and vendor code C about 1 mA higher over the full military temperature range. The reason for this is that vendor code C contained samples of SE5537s which are designed to drive a 2 K ohm load. A limit change has been proposed to account for this difference in device characteristics.

Logic Input Leakage CurrenIIH, IIL)

Even though all of the data is much less than the specified limits, the only recommended change is to use the initial 25°C limits over the full temperature range.

Output Short Circuit Current (Ios(+), Ios(-))

As with supply current, the output short circuit current of the SE5537s was greater than that for the LF198's. In order to have the limits reflect the device characteristics, higher limit values have been proposed. Also the SE5537's limits are specified separately.

Hold Capacitor Leakage Current (IHL(+), IHL(-))

Hold capacitor leakage currents were measured at both common mode extremes (± 11.5V) as IHL(+) and IHL(-). These leakage currents are due to the FET input on the final stage of the device. Data distributions were relatively normal and are well within specified limits.

One of the weakest features of the LF198 is that in going from 25°C to 125°C, the leakage current can theoretically increase a thousand fold.

(i.e. $I(125^{\circ}C) = I(25^{\circ}C) * 2 \exp((125-25)/10) = I(25^{\circ}C) * 1000$)

This means that at elevated temperatures "hold" data is much more volatile. Consequently, A/D conversion of this data voltage must be proportionally quicker.

Hold Capacitor Charge Current (ICH(+), ICH(-))

Since hold capacitor charge current is largely a function of the series charge resistance of the device, the data distributions for ICH(+) and ICH(-) were divided into two distinct vendor groups as was the Rsc data. Vendor Code B which had nominal Rsc values of approximately 150 ohms displayed the largest charge currents. These were typically around 8 to 10 mA whereas vendor codes A and C were around 4 to 7 mA.

In testing the devices a ten milliampere full-scale range was considered reasonable for the 3 milliampere maximum limit. Nevertheless, several devices had sufficient charge current to saturate the meter with readings of 10.2 mA. No limit change was recommended because the weaker devices need the established limits.

Logic Threshold Voltage (VTH)

The operating mode (sample or hold) for a device is determined by the logic input voltage and its relationship to the logic threshold voltage. In characterizing the LF198, the exact threshold was determined on an iterative basis by finding the logic input level at which hold capacitor leakage current changed to charge current. The resulting logic threshold voltage varies with temperature such that at -55°C it is typically at 1.6 V and at 125°C it is 0.85V. Although no failures were observed, the 125°C test is the closest to the TTL compatible logic level limit of VIL(max) = 0.8V.

Acquisition time (taq)

Data distributions of acquisition time measurements reveal a distinct division between Vendor Code B and Vendor Codes A and C. Acquisition times for devices of Vendor Code B are typically 12 to 16 usec at 25°C, whereas those of Vendor Codes A and C have a mean of approximately 21 usec.

Although acquisition time is a dynamic parameter which is rather difficult to measure on an automatic test basis, it closely correlates with two simple static parameters. Both hold capacitor charge current and series charge resistance have a direct effect on acquisition time. The slew rate interval of acquisition is reduced with increased charge current. In the same way lower series charge resistance speeds up the final settling interval of acquisition time. Data for all transitions are within the specified limits at 25°C. Although no limits are specified over the military temperature range, the trend is for acquisition times to increase with increasing temperature. This is due in part to the increase in series charge resistance with temperature.

Aperture time (tap)

Aperture time data for positive transitions (i.e. 0V to 10V and -10V to 0V) were normally distributed and fell within specified limits at 25°C. The negative transitions, however, exhibited a high percentage of failures against the 200 nanosecond maximum limit. It was necessary to increase the limit to 300 nanoseconds in order to have reasonable test yields. Although aperture time is not specified over the military temperature range, observations show that at 125°C typical data values are 100 to 150 nanoseconds longer than the corresponding 25°C values. At -55°C, aperture time values were typically shorter than at 25°C by 75 to 125 nanoseconds.

Transient Response Overshoot (TR(OS))

There were no observed failures of this parameter. However, manufacturer code A devices were considerably more sensitive to capacitive loading than devices from the other two manufacturers.

Transient Response Settling Time (TR(ts))

No specification change was recommended eventhough the data suggests that a tightening of the maximum limit from 2.5 microseconds to 2.0 microseconds could be tolerated.

Noise (en)

All of the devices had very low broadband noise in both the "sample" and "hold" modes.

Settling Time (ts)

"Hold" mode settling time of all the devices was well within the 1.5 microsecond (max) limits.

5.6 Slash Sheet Development

MIL-M-38510/125 was the first slash sheet to be written for Sample and Hold circuits. New parameters and test conditions had to be defined for this slash sheet. Most of the original ideas on parameters and how to test them came from Carl Nelson, the designer of the LF198 at National Semiconductor Corp.

Development of the slash sheet closely followed the characterization effort, such that changes to either could be factored into the other. Many subtle problems arose and had to be solved. MIL-M-38510/125 was developed using the most comprehensive and efficient test methods, which could be mustered. An on-going dialogue was maintained with all of the manufacturers during this development.

Some parameters and the format of the specification are similar to those in the Bi-FET op amp slash sheets.

.7 Conclusions and Recommendations

A characterization study was conducted on a sample of LF198 and SE5537 devices from three manufacturers. Although the original data base contained over 60 devices during the test development phase, 37 devices were used for the final statistical data base. The reason for the reduced data base was to have equal manufacturer representation in the sample.

The results of the characterization study were incorporated into MIL-M-38510/125. Both the data handbook and the revised version of the slash sheet were presented to RADC and the manufacturer representatives at a JC-41 meeting in Burlington, Mass on Oct. 7, 1980. It is recommended that MIL-M-38510/125 be accepted by RADC and the manufacturers. Table I of MIL-M-38510/125 concludes this report section.

The LF198 Sample and Hold circuits have many excellent features, which should make them useful and cost effective in a variety of applications.

.8 Bibliography

Linear Databook, National Semiconductor (1978)

C. Nelson, "I.C. Sample and Hold is 0.01% Accurate," E.E. Times I.C. Applications Conference Proceedings, 1977.

C. Nelson, National Semiconductor, LF198 Test Information. (not published)

M. Mullen, Advanced Micro Devices, LF198 Test Information. (not published)

RADC-TR-80-49, Electrical Characterization of Special Purpose Linear Microcircuits, May 1980.

MANUFACTURER CODE: A DEVICE TYPE: 198 ; S/N: 23 ; DATE CODE: 7909 26 SEP 80 08:52:52

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	+125 DEG C LO-LIM	+125 DEG C DATA	+125 DEG C HI-LIM	
VIO(+CM) AT 3.5V,-26.5V	-5.00	-858.M	5.00	-3.00	-19.5M	3.00	-5.00	374.M	5.00	MV
VIO(-CM) AT 26.5V,-3.5V	-5.00	478.M	5.00	-3.00	418.M	3.00	-5.00	836.M	5.00	MV
VIO(DCM) AT 15.0V,-15.0V	-5.00	274.M	5.00	-3.00	371.M	3.00	-5.00	756.M	5.00	MV
VIO(-CM) AT 7.0V,-3.0V	-5.00	82.3M	5.00	-3.00	75.5M	3.00	-5.00	403.M	5.00	MV
VIO(+CM) AT 3.0V,-7.0V	-5.00	-632.M	5.00	-3.00	-452.M	3.00	-5.00	-10.1M	5.00	MV
DELTA VIO/DELTA T (DCM)	-20.0	1.21	20.0	0.00	0.00	0.00	-20.0	-3.86	20.0	UV/DEG C
IIB(+CM) AT 3.5V,-26.5V	-75.0	14.8	75.0	1.00	7.10	25.0	-75.0	-1.96	75.0	NA
IIB(-CM) AT 26.5V,-3.5V	-75.0	14.2	75.0	1.00	6.23	25.0	-75.0	-10.1	75.0	NA
IIB(DCM) AT 15.0V,-15.0V	-75.0	14.2	75.0	1.00	6.42	25.0	-75.0	-9.54	75.0	NA
IIB(-CM) AT 7.0V,-3.0V	-75.0	14.3	75.0	1.00	6.46	25.0	-75.0	-3.97	75.0	NA
IIB(+CM) AT 3.0V,-7.0V	-75.0	14.4	75.0	1.00	6.63	25.0	-75.0	-1.32	75.0	NA
INPUT IMPEDANCE (ZI)	1.00	35.6	500.	2.00	26.4	500.	1.00	1.42	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	300.M	4.00	0.00	400.M	2.00	0.00	580.M	4.00	OHMS
RSC-SERIES CHG RESISTANCE	100.	345.	600.	100.	385.	400.	100.	479.	600.	OHMS
GAIN ERROR (+/-11.5V CM)	-20.0M	-3.35M	20.0M	-5.00M	-2.17M	5.00M	-20.0M	-8.69M	20.0M	%
GAIN ERROR (+/-2.0V CM)	-40.0M	-19.6M	40.0M	-20.0M	-14.5M	20.0M	-40.0M	-16.3M	40.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	14.4	30.0	6.00	18.2	30.0	6.00	22.2	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-4.46 %	-6.00	-30.0	-5.53 %	-6.00	-30.0	-5.97 %	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	97.3	200.	80.0	95.5	200.	80.0	93.8	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	132.	200.	80.0	100.	200.	80.0	96.1	200.	dB
FEEDTHRU REJ 0V TO 15V IN	80.0	91.3	200.	86.0	90.4	200.	80.0	89.3	200.	dB
FEEDTHRU REJ 15V TO 0V IN	80.0	95.7	200.	86.0	94.8	200.	80.0	93.2	200.	dB
FEEDTHRU REJ 0V TO-15V IN	80.0	94.4	200.	86.0	87.9	200.	80.0	88.0	200.	dB
FEEDTHRU REJ -15V TO 0V	80.0	91.7	200.	86.0	89.1	200.	80.0	97.4	200.	dB
HOLD STEP VOLTAGE (VHS+)	-5.00	215.M	5.00	-2.00	-370.M	2.00	-5.00	-666.M	5.00	MV
HOLD STEP VOLTAGE (VHS-)	-5.00	-173.M	5.00	-2.00	-1.01	2.00	-5.00	-2.14	5.00	MV
ICC-SUPPLY CURRENT (15V)	0.00	4.30	6.50	0.00	3.93	5.50	0.00	3.82	5.00	MA
IIH-LOGIC INPUT	0.00	3.31	20.0	0.00	1.15	10.0	0.00	710.M	20.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	1.32	20.0	0.00	635.M	10.0	0.00	410.M	20.0	UA
IIL-LOGIC INPUT	-3.00K	-900.M	3.00K	-1.00K	-700.M	1.00K	-3.00K	-1.45	3.00K	MA
IIL-LOGIC REFERENCE INPUT	-3.00K	-350.M	3.00K	-1.00K	-1.20	1.00K	-3.00K	-2.95	3.00K	MA
OUTPUT SHORT CIRCUIT (+)	-20.0	-12.4	0.00	-20.0	-8.70	0.00	-20.0	-5.45	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	14.2	20.0	0.00	11.2	20.0	0.00	8.45	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	0.00	5.00	0.00	-100.	-44.0	100.	-100.K	-13.7K	100.K	PA
HOLD CAPACITOR LEAKAGE(-)	0.00	1.00	0.00	-100.	8.00	100.	-100.K	1.85K	100.K	PA
HOLD CAP CHRG CURRENT(+)	-100.	-5.60	-2.00	-100.	-4.44	-3.00	-100.	-3.33	-2.00	MA
HOLD CAP CHRG CURRENT(-)	2.00	4.42	100.	3.00	4.12	100.	2.00	3.15	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	1.48	2.00	800.M	1.25	2.00	800.M	840.M	2.00	V
TAQ (VIN=0V TO 10V STEP)	0.00	28.2	50.0	0.00	29.7 %	85.0	0.00	34.3	50.0	USEC
TAQ (VIN=0V TO -10V STEP)	0.00	28.2	50.0	0.00	30.4 %	85.0	0.00	50.0	50.0	USEC
TAQ (VIN=-10V TO 0V STEP)	0.00	27.5	50.0	0.00	29.8 %	85.0	0.00	35.7	50.0	USEC
TAQ (VIN=10V TO 0V STEP)	0.00	28.1	50.0	0.00	29.8 %	85.0	0.00	34.4	50.0	USEC
TAP (VIN=0V TO 10V STEP)	0.00	45.0	400.	0.00	105.	200.	0.00	220.	400.	NSEC
TAP (VIN=0V TO -10V STEP)	0.00	25.0	400.	0.00	85.0	200.	0.00	180.	400.	NSEC
TAP (VIN=-10V TO 0V STEP)	0.00	45.0	400.	0.00	95.0	200.	0.00	210.	400.	NSEC
TAP (VIN=10V TO 0V STEP)	0.00	30.0	400.	0.00	90.0	200.	0.00	185.	400.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-5. Typical Mfr. Code A Device Data Sheet.

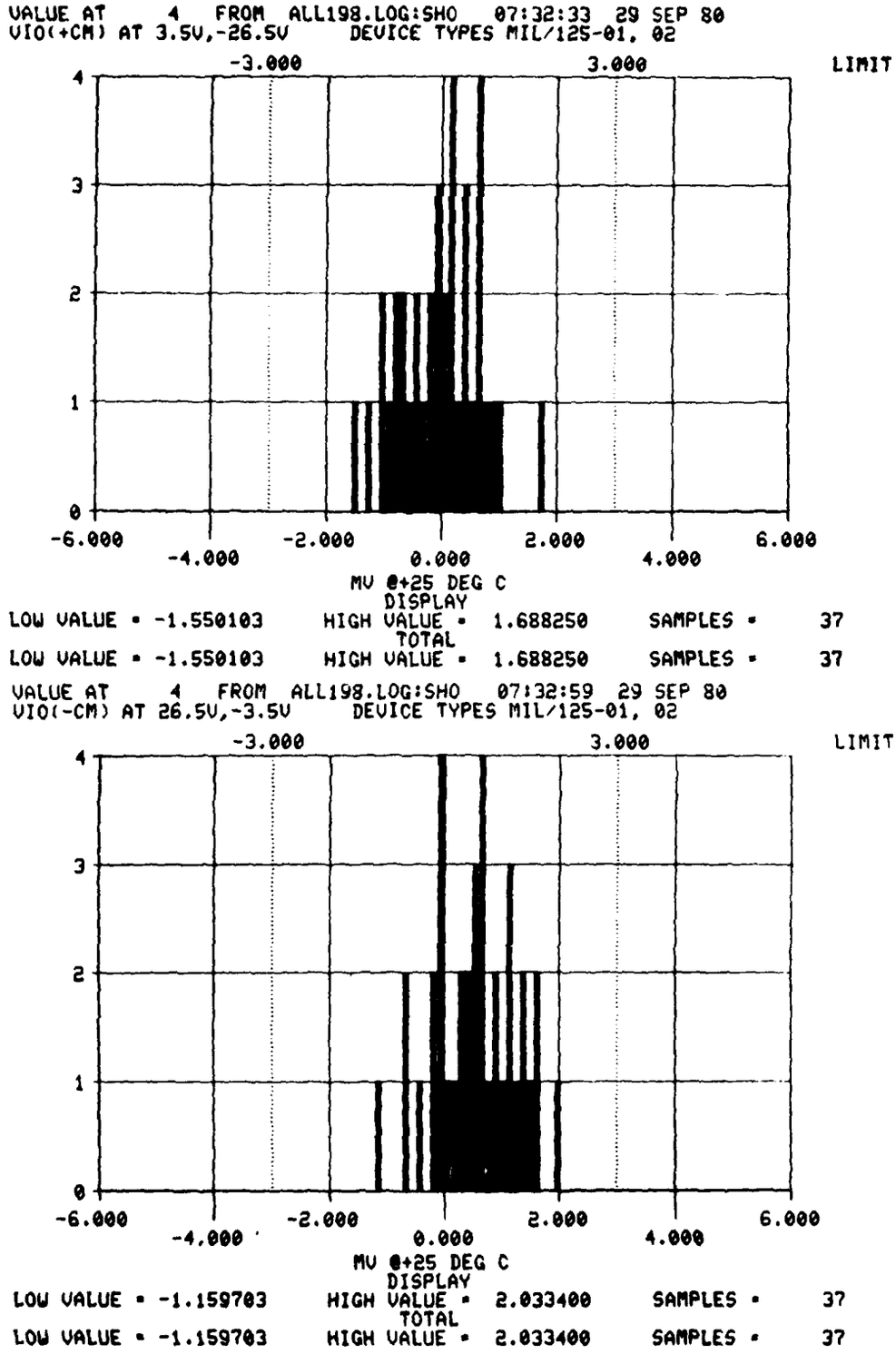


Figure 5-15. Offset Voltage at 25°C

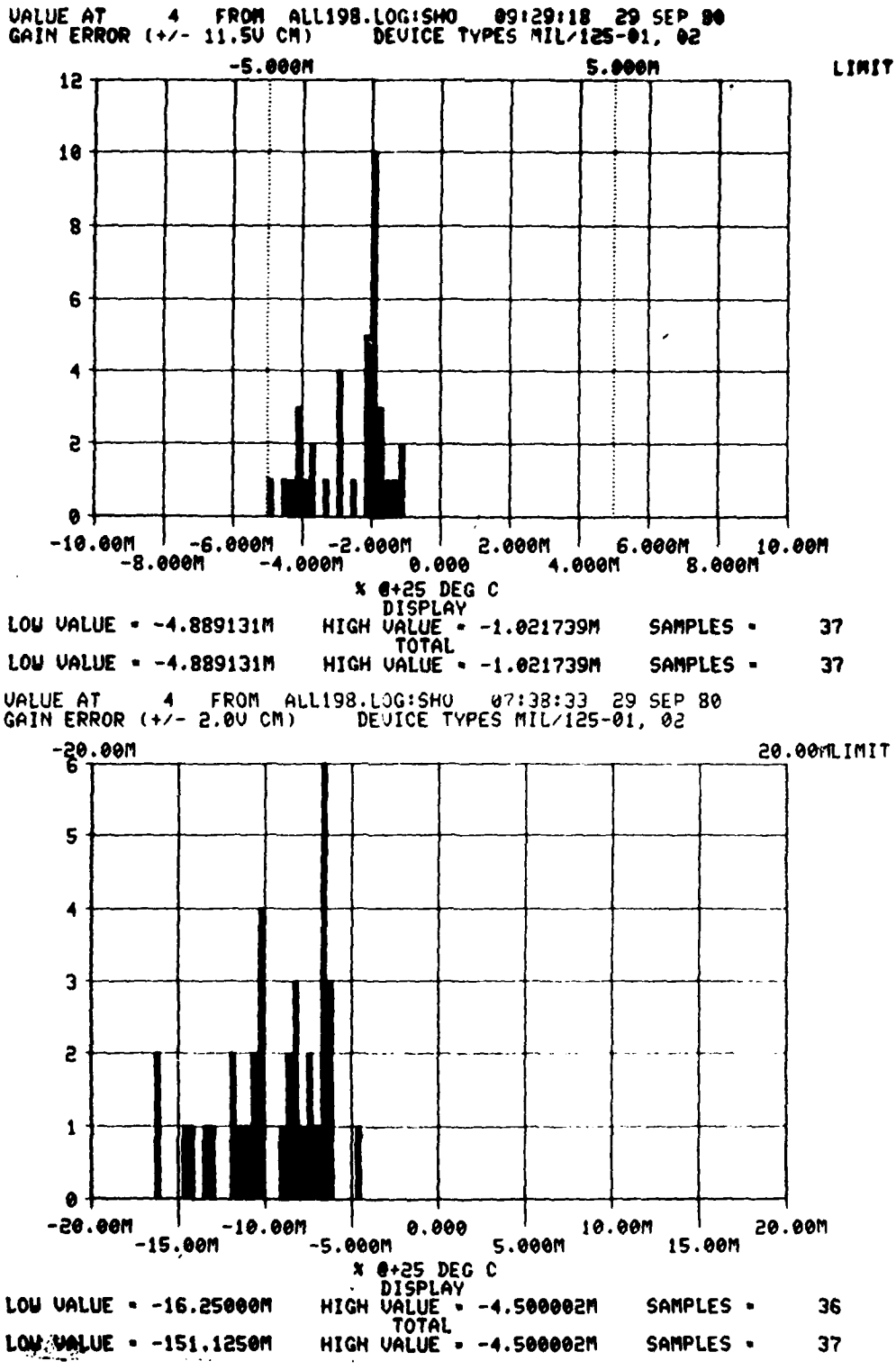


Figure 5-16. Gain Error at 25°C

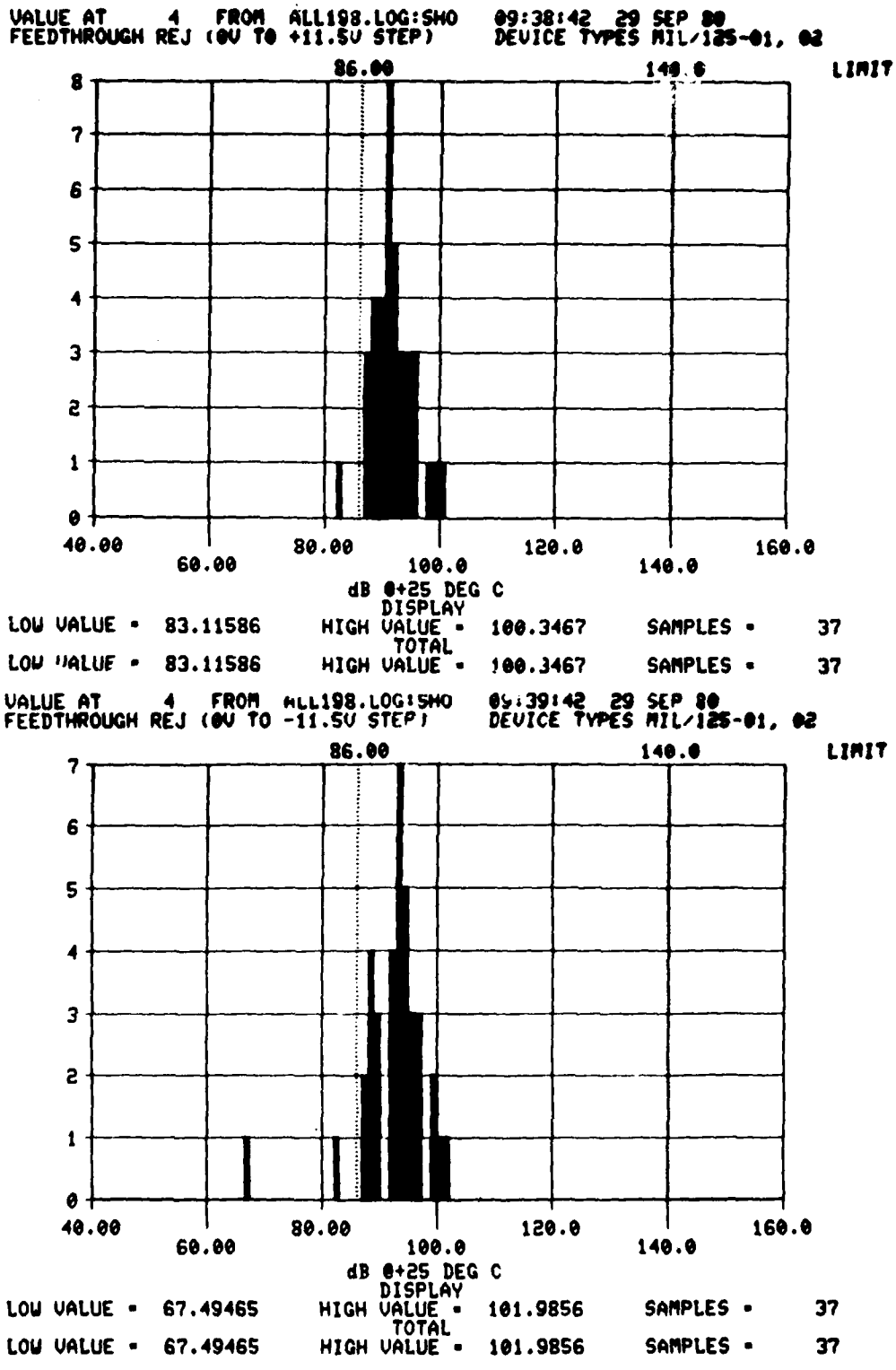


Figure 5-17. Feedthrough Rejection at 25°C

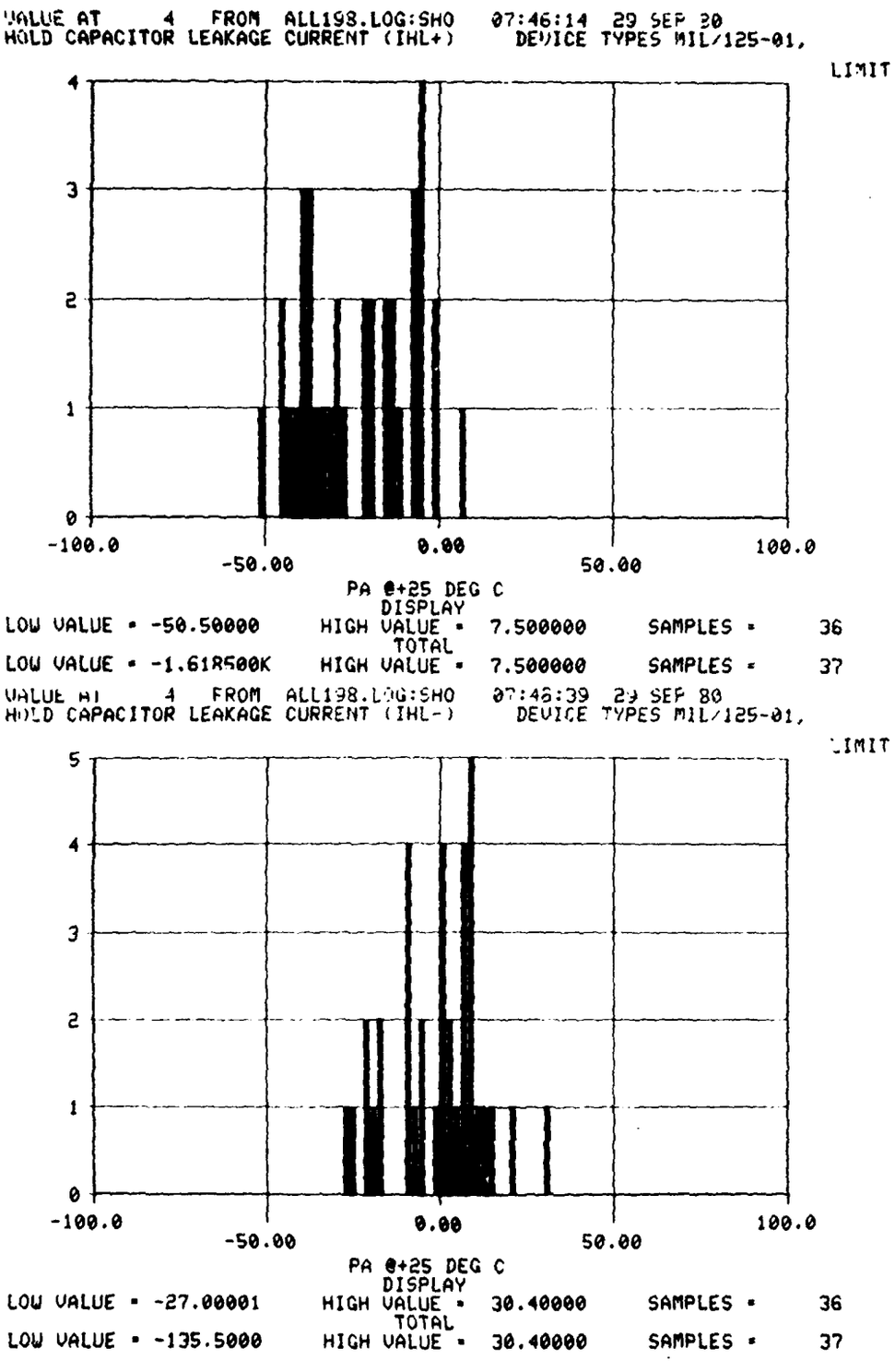


Figure 5-18. Hold Capacitor Leakage Current at 25°C

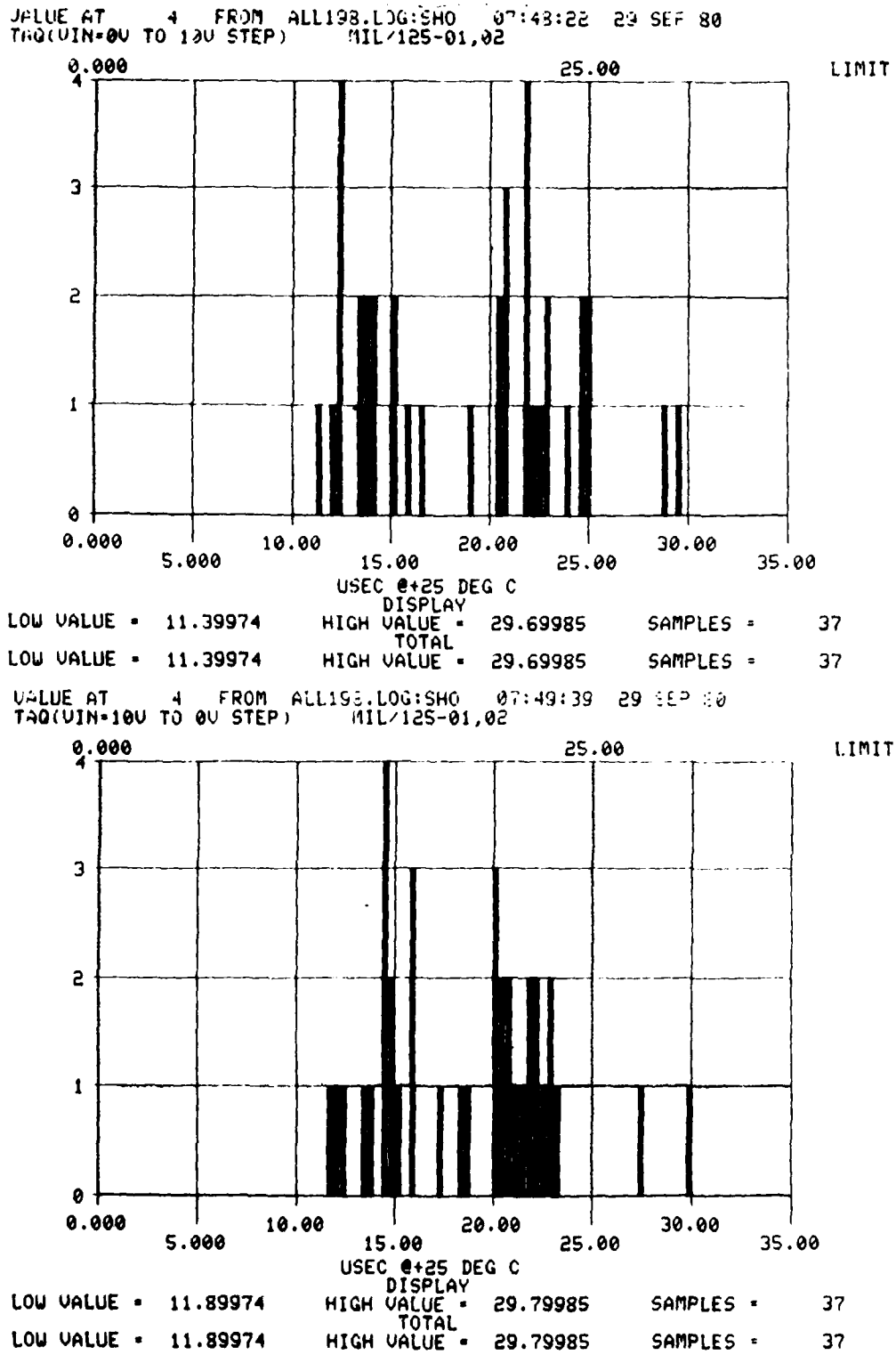


Figure 5-19. Acquisition Time at 25°C

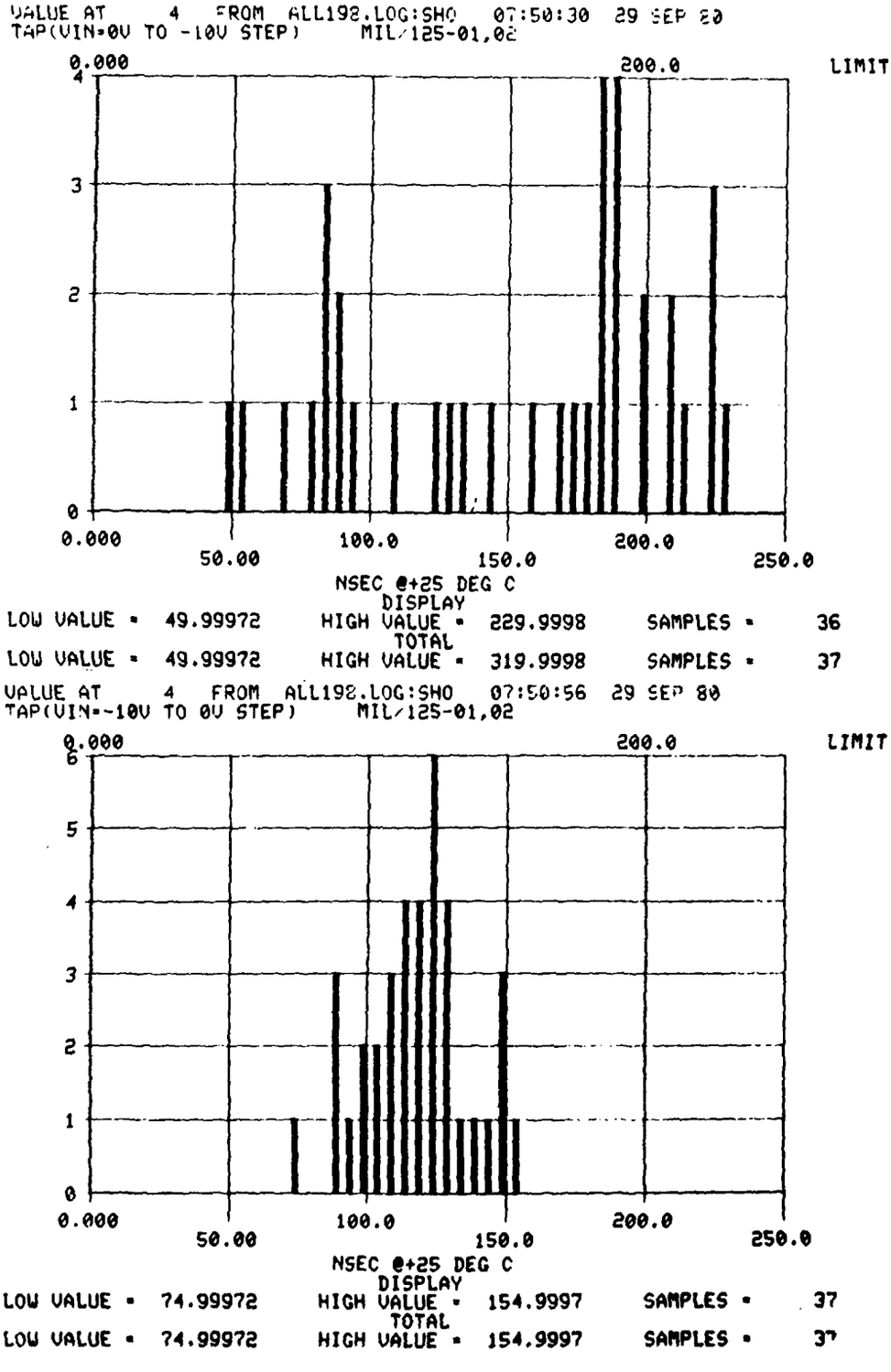


Figure 5-20. Aperture Time at 25°C

Table 5-6 . LF198 Sample and Hold Data Distribution vs. Limits.

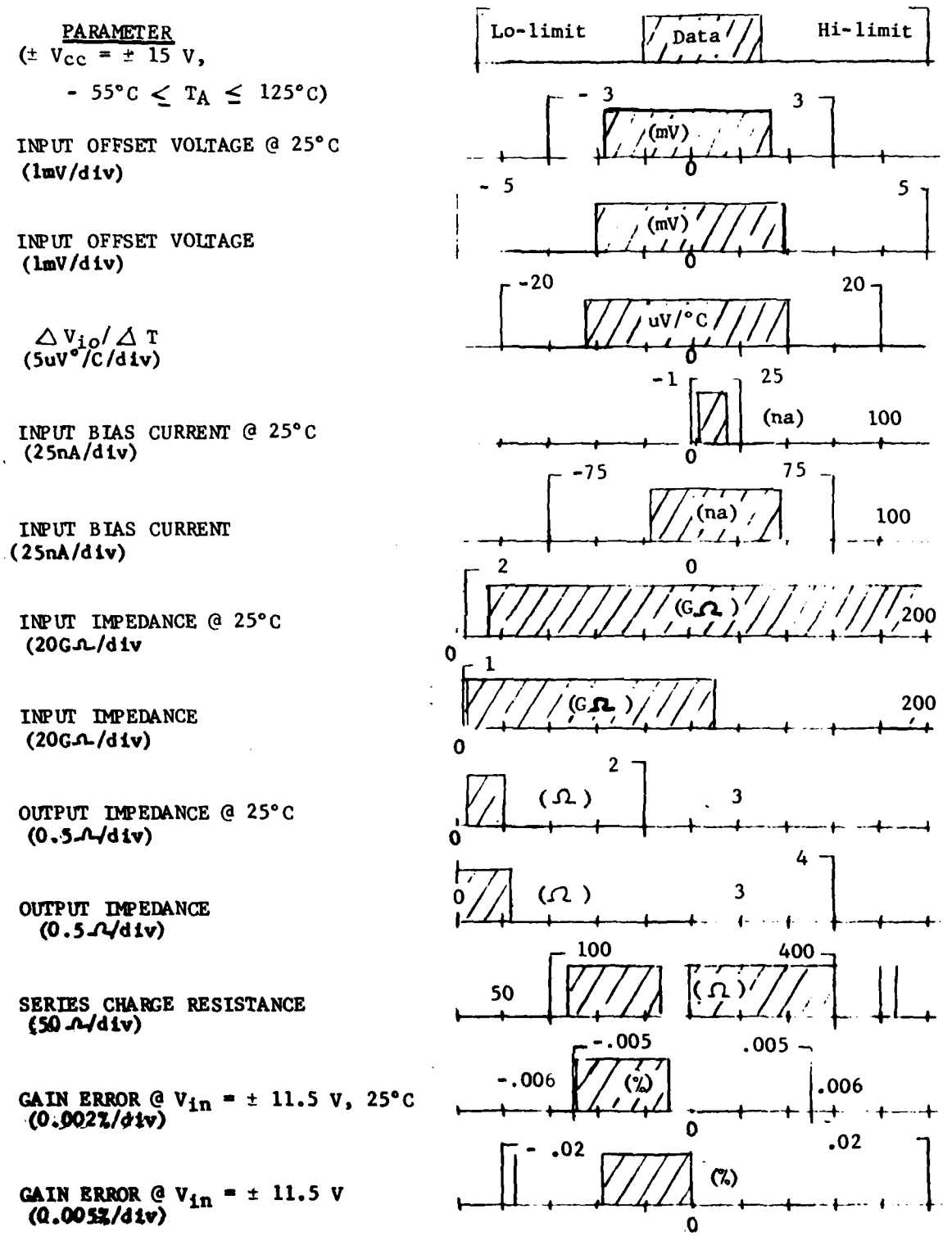


Table 5-6. LF198 Sample and Hold Data Distribution vs. Limits.

PARAMETER ($\pm V_{CC} = \pm 15$ V, $-55°C \leq T_A \leq 125°C$)	
GAIN ERROR @ $V_{CC} = \pm 5$V, 25°C (0.01%/div)	LO-LIMIT, DATA, HI-LIMIT; -.02, .02, (%), .01, 0
GAIN ERROR @ $V_{CC} = \pm 5$V (0.01%/div)	-.04, .04, (%), 0
OFFSET VOLTAGE ADJ. (+) (3mV/div)	0, 6, (mV), 30
OFFSET VOLTAGE ADJ. (-) (5mV/div)	-40, -30, -6, (mV), 0
POWER SUPPLY REJ. RATIO (+ PSRR) (10dB/div)	60, 80, (dB), 130
POWER SUPPLY REJ. RATIO (- PSRR) (10dB/div)	60, 80, (dB)
FEEDTHROUGH REJ. RATIO @ 25°C (10dB/div)	60, 86, (dB), 120
FEEDTHROUGH REJ. RATIO (10dB/div)	60, 80, (dB)
HOLD STEP (V_{HS+}, V_{HS-}) @ 25°C (1mV/div)	-2, 2, (mV), 0
HOLD STEP (V_{HS+}, V_{HS-}) (1mV/div)	-5, 5, (mV), 0
SUPPLY CURRENT @ 25°C TO 125°C (0.5mA/div)	3, 5.5, (mA), 6
SUPPLY CURRENT @ - 55°C 0.5mA/div)	3, 6.5, (mA), 7

Table 5-6. LF198 Sample and Hold Data Distribution vs. Limits.

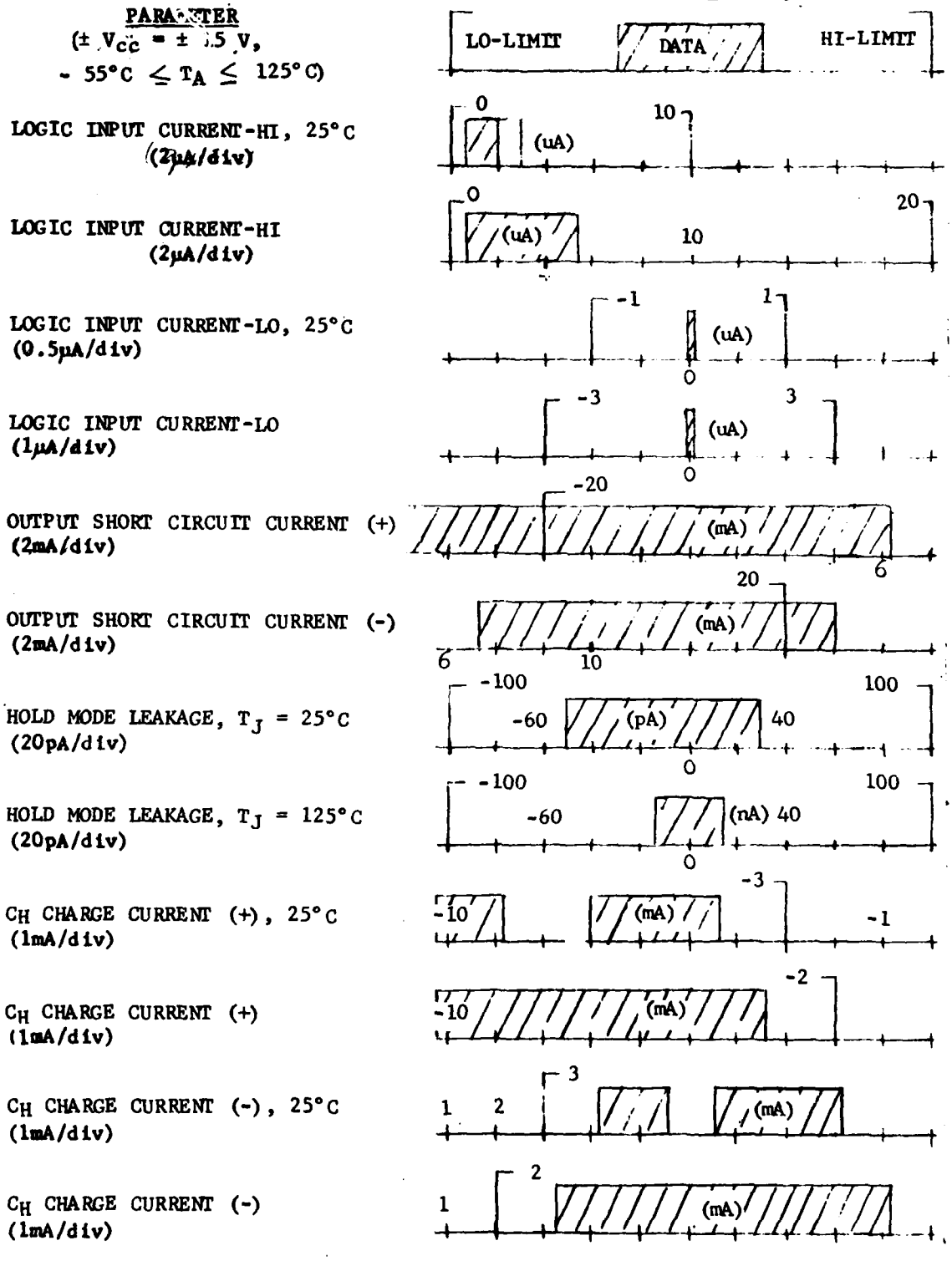
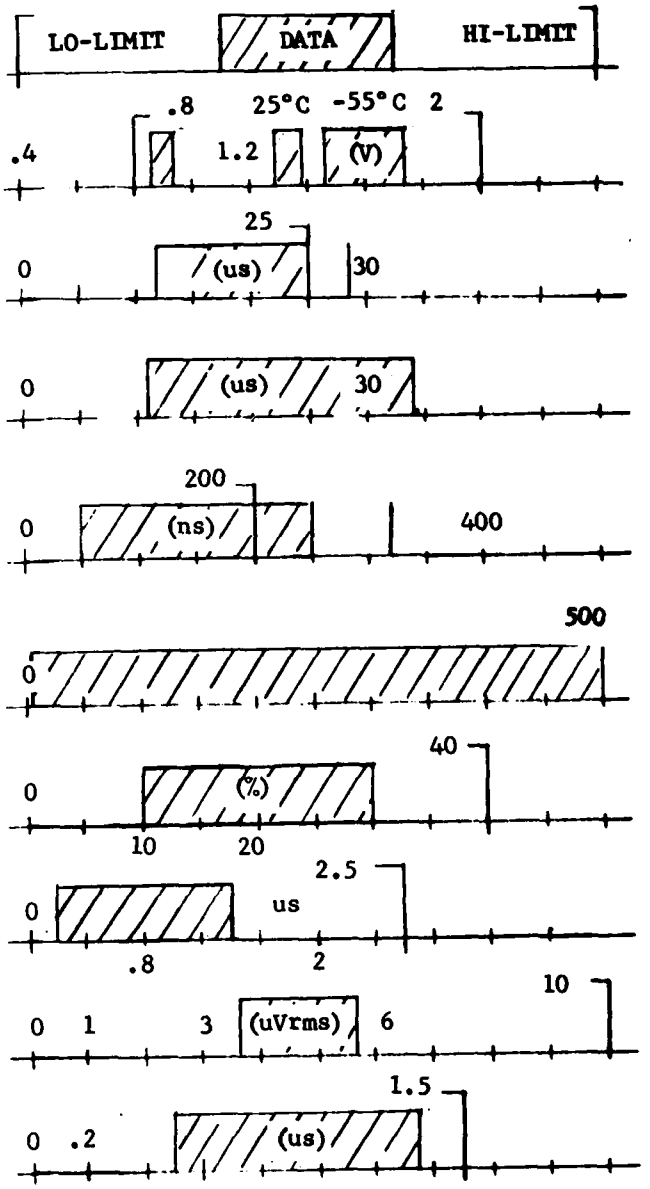


Table 5-6. LF198 Sample and Hold Data Distribution vs. Limits.



Electrical performance characteristics 1/

(Changes = *)

Characteristic	Symbol	Conditions for all device types ($\pm V_{CC} = \pm 15$ V and paragraph 3.4 with Figure 7 unless otherwise specified)		Limits Min	Limits Max	Units
Input offset voltage 2/	V_{IO}	$\pm V_{cc} = \pm 5V$ to $\pm 15V$	$T_A = 25^oC$	-3	+3	mV
			$-55^oC \leq T_A \leq +125^oC$	-5	+5	mV
Input Offset voltage temperature sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{cc} = \pm 15V$	$T = -55^oC$ to 25^oC	-20	20	uV/°C
			$T = 25^oC$ to 125^oC	-20	20	uV/°C
Input bias current 2/	I_{IB}	$\pm V_{cc} = \pm 5V$ to $\pm 15V$	$T_A = 25^oC$	-1	25	nA
			$-55^oC \leq T_A \leq 125^oC$	*-50	75	nA
Input impedance 3/	Z_i		$T_A = 25^oC$	2	-	G Ω
			$-55^oC \leq T_A \leq 125^oC$	1	-	G Ω
Gain error	A_e	$V_{in} = -11.5V$ to $+11.5V$ $R_L = 10K$	$T_A = 25^oC$	-.005	+.005	%
			$-55^oC \leq T_A \leq 125^oC$	-.02	+.02	%
		For device type 02 only $V_{in} = -10V$ to $+10V$ $R_L = 2K$	$T_A = 25^oC$	-.005	+.005	%
			$-55^oC \leq T_A \leq 125^oC$	-.02	+.02	%
		$V_{cc} = \pm 5V$ $V_{in} = -2V$ to $+2V$ $R_L = 10K$	$T_A = 25^o C$	-.02	+.02	%
			$-55^oC \leq T_A \leq 125^oC$	-.04	+.04	%
Input offset voltage adjustment	$V_{IO(ADJ+)}$	$V_{in} = 0V$, $V_{OFFSET\ ADJ}$ at $+V_{cc}$		6	-	mV
	$V_{IO(ADJ-)}$	$V_{in} = 0V$, $V_{OFFSET\ ADJ}$ at 1K from $+V_{cc}$, 20K from 0V		-	-6	mV *
Power supply rejection ratio	+PSRR	$+V_{cc} = +12V$ to $+18V$, $-V_{cc} = -18V$, $V_{in} = 0V$		80	-	dB
	-PSRR	$+V_{cc} = 18V$, $-V_{cc} = -12V$ to $-18V$, $V_{in} = 0V$		80	-	dB

Electrical performance characteristics 1/

Characteristic	Symbol	Conditions for all device types ($\pm V_{CC} = \pm 15$ V and paragraph 3.4 with Figure 7 unless otherwise specified)	Limits Min	Limits Max	Units	
Feedthrough rejection ratio	FRR	V_{in} = ±11.5V, Hold mode, see Figure 8; $T_A = 25^oC$	86	-	dB	*
		$-55^oC \leq T_A \leq +125^oC$	80	-	dB	
4/	FRR_{AC}	V_{in} = 20Vpp @ 1 kHz, Hold mode see Figure 9; $T_A = 25^oC$	86	-	dB	
Series charge resistance 5/	R_{sc}	V_{in} = 0V to 0.4V; Measure current change to ground at pin 6 (hold cap terminal)	100	400	Ω	
Output impedance	Z_o	Hold Mode, See Figure 10; $V_{hold\ cap} = V_{HC}$ = 0V, I_O = ± 1 mA	-	2	Ω	*
"Hold" step 6/	V_{hs}	V_{Logic} = 4V, See Figure 11, $t_r \leq 50$ ns, V_{out} = ± 11.5V; $T_A = 25^oC$	-2	2	mV	
		$-55^oC \leq T_A \leq 125^oC$	-5	5	mV	
Supply current	I_{cc}	V_{cc} = ±15V; $T_A = -55^oC$; Device type 01	1	6.5	mA	
		$T_A = -55^oC$; Device type 02	1	7.0	mA	*
		$25^oC \leq T_A \leq 125^oC$; Device type 01	1	5.5	mA	
		$25^oC \leq T_A \leq 125^oC$; Device type 02	1	6.0	mA	*
Logic input current (high)	I_{IH}	V_{Logic} = 5.5V, $+V_{cc}$ = 8.5V, $-V_{cc}$ = 21.5V	0	10	uA	*
Logic input current (low)	I_{IL}	V_{Logic} = 0V, $+V_{cc}$ = 21.5V, $-V_{cc}$ = -8.5V	-1	1	uA	*
Output short circuit current (positive output)	$I_{OS(+)}$	V_{in} = 10V, $t \leq 25$ ms (short circuit to 0V); Device type 01	-30	-	mA	*
		Device type 02	-35	-	mA	*
Output short circuit current (negative output)	$I_{OS(-)}$	V_{in} = -10V, $t \leq 25$ ms (short circuit to 0V); Device type 01	-	30	mA	*
		Device type 02	-	35	mA	*

Electrical performance characteristics 1/

Characteristic	Symbol	Conditions for all device types ($\pm V_{CC} = \pm 15$ V and paragraph 3.4 with Figure 7 unless otherwise specified)		Limits Min	Limits Max	Limits Units
Hold mode leakage current (positive output)	$I_{HL(+)}$ 7/	V_{in} = 0V, $+V_{CC}$ = 3.5V, $-V_{CC}$ = -26.5V See Figure 12	T_J = 25°C 9/	-100	100	pA
			T_J = 125°C 9/	-50	50	nA *
Hold mode leakage current (negative output)	$I_{HL(-)}$ 7/	V_{in} = 0V, $+V_{CC}$ = 26.5V, $-V_{CC}$ = -3.5V See Figure 12	T_J = 25° C 9/	-100	100	pA
			T_J = 125°C 9/	-50	50	nA
Hold capacitor charge current (positive output)	$I_{CH(+)}$	V_{in} = 11.5V, V_{HC} = 9.5V	T_A = 25°C	-	-3	mA
			-55°C $\leq T_A \leq$ 125°C	-	-2	mA
Hold capacitor charge current (negative output)	$I_{CH(-)}$	V_{in} = -11.5V, V_{HC} = -9.5V	T_A = 25°C	3	-	mA
			-55°C $\leq T_A \leq$ 125°C	2	-	mA
Differential logic threshold	$V_{TH(H)}$	V_{in} = -2V, V_{Logic} = 2V (Check for I_{hold} cap $\geq$ 1 mA)		-	2	V
	$V_{TH(L)}$	V_{in} = -2V, V_{Logic} = .8V (Check for I_{hold} cap $\leq$ 10 uA)		.8	-	V
Acquisition time (0.01% error)	t_{aq} 10/	V_{in} = 0V to 10V, 10V to 0V, 0V to -10V, -10V to 0V C_L = 100 pF, See Figures 13 and 14	T_A = 25°C	-	25	us
Aperture time	t_{ap} 10/	V_{in} = 0 to +10V, 10V to 0V, 0V to -10V, -10V to 0V $V_o \leq$ 1 mV, See Figures 15 and 16	T_A = 25°C	-	300	ns
Transient response (settling time) 8/	$TR_{(ts)}$	V_{in} = 100 mV step, C_H = 1000 pF, R_L = 10K , C_L = 100 pF See Figure 17 (to 10% of final value)	T_A = 25°C	-	2.5	us
Transient Response (Overshoot) 8/	$TR_{(OS)}$	V_{in} = 100 mV step, C_H = 1000 pF, R_L = 10K , C_L = 100 pF See Figure 17	T_A = 25°C	-	40	%

Electrical performance characteristics 1/

Characteristic	Symbol	Conditions for all device types ($\pm V_{CC} = \pm 15$ V and paragraph 3.4 with Figure 7 unless otherwise specified	Limits		
			Min	Max	Units
Noise	$en_{(H)}$, $en_{(S)}$	Hold mode, sample mode $T_A = 25^oC$ 10 Hz to 10 kHz, See Figure 18	-	10	uV_{rms} *
Settling time	ts	$V_{in} = 0V$ $T_A = 25^oC$ $V_o \leq 1$ mV, Hold mode, See Figure 19	-	1.5	us

NOTES:

1/ See definitions as described in 6.4.

2/ This parameter is specified at $V_{CM} = 0V$, -11.5V and +11.5V with $\pm V_{cc} = \pm 15V$, and at $V_{CM} = -2V$ and 2V with $\pm V_{cc} = \pm 5V$.

3/ Input impedance is calculated from the V_{IO} and I_{IB} common mode voltage end point range data.

4/ Feedthrough rejection ratio is very sensitive to stray capacitance between the signal input (pin 3) and the hold capacitor (pin 6). For instance 0.5 pF of external coupling with a .01 uF hold capacitor would equal the specification limit of the device.
(i.e. FRR = 20 log $\frac{(.01uF)}{.5pF}$ = 20 log (2.10^4) = 86 dB)

5/ Series change resistance along with input signal slew rate and an external hold capacitor determine the dynamic sampling error of the device in its application. (i.e. DSE = K $\cdot R_{sc} \cdot$ SR where K is a proportionality constant.)

6/ The external hold capacitor should be either Teflon or polystyrene so that dielectric absorption is minimized. This will insure that excessive "sag back" after capacitor "sample" mode charging does not occur. "Hold" step is sensitive to stray capacitive coupling between input logic signals and the "hold" capacitor.

7/ Hold mode leakage current is actually JFET junction leakage current which doubles (approximately) for each 10°C increase in junction temperature. Measurement at -55°C is not necessary since expected values are to small for typical test systems.

8/ Transient response shall be measured at the common mode voltage limits. (i.e. V_{CM} = -11.5V and +11.5V). Any high frequency ringing shall be over within one microsecond. After its peak the major loop response shall be without further oscillations.

9/ The specification is at T_J instead of T_A to enable automatic testing. A warm-up time delay would be required for T_A testing.

10/ Acquisition time at 125°C typically increases from 20% to 100% above the 25°C value.

11/ Aperture time at 125°C typically increases 100% above the 25°C value.

Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331, and as follows:

a. Input offset voltage - V_{IO}. The "sample" mode output to input D.C. voltage for any rated common mode voltage condition.
b. Input bias current - I_{IB}. The current flowing into the signal input for any rated common mode voltage condition.
c. Gain error - A_E. The ratio of "sample" mode output voltage swing to input common mode voltage swing expressed in percent. To the user this can be interpreted as the percentage deviation from unity gain.
d. Common mode voltage - V_{cm}. The voltage of the input terminal with respect to a voltage midway between + V_{cc} and - V_{cc}.
e. Power supply rejection ratio - + PSRR, - PSSR. The ratio in dB of the change in $+V_{cc}$ or - V_{cc} voltage to the change in offset voltage measured at the output with the opposite - V_{cc} or + V_{cc} voltage held constant.
f. Feedthrough rejection ratio - FRR. The ratio in dB of an input voltage change to a "hold" mode output voltage change.
g. "Hold" step - V_{HS}. The output voltage change with a fixed input voltage when the device is switched from "sample" to "hold" mode with a 4 V logic signal.
h. Logic input correct - I_{IH}, I_{IL}. The current into a mode control input for a forward bias (high state), I_{IH}, condition or a below threshold (low state), I_{IL}, condition.
i. Output short circuit current - $I_{OS(+)}$, $I_{OS(-)}$. The "sample" mode output short circuit current to ground with + 10 V and - 10 V applied at the input for $I_{OS(+)}$ and $I_{OS(-)}$ respectively.
j. Hold mode leakage current - $I_{HL(+)}$, $I_{HL(-)}$. The input bias current of the output buffer amplifier. This leakage current causes a droop rate error of the external hold capacitor.
k. Hold capacitor charge current - $I_{CH(+)}$, $I_{CH(-)}$. The current that the input amplifier can supply to charge up the hold capacitor.
l. Acquisition time - t_{aq}. The time, in terms of minimum sample pulse width, that is required for the device to acquire a 10 Volt full scale change to within a specified error band of final value for a specified hold capacitor size.
m. Aperture time - t_{ap}. The delay required between the "hold" command and a 10 V input signal transition such that the resulting output change is less than 1 mV.
n. Hold settling time - t_s. The time required for the output to settle within 1 mV of final value after the "hold" command is given.
o. Dynamic sampling error - DSE. The error introduced into the held output due to a changing analog input when the "hold" command is given. This error is proportional to the product of input signal slew rate, hold capacitance and the series charge resistor.

Abbreviations, symbols, and definitions. (continued)

p. Transient response (settling time) - TR(t_s). The small signal time interval from the application of a 100 mV pulse to the time when the output enters and remains within 10% of its final value.

q. Transient response (overshoot) - TR(OS). The percentage ratio of signal overshoot to the 100 mV final value. This parameter is related to circuit phase margin and stability.

r. Noise - $e_n(s)$, $e_n(H)$. The total rms noise of the device that exists within a 10 Hz to 10 kHz "brickwall" bandwidth. Both "sample" mode, $e_n(s)$, and "hold" mode, $e_n(H)$, specifications exist.

SECTION V

APPENDIX

SAMPLE/HOLD CIRCUITS

MIL-M-38510/125

MANUFACTURER CODE: A DEVICE TYPE: 198 ; S/N: 28 ; DATE CODE: 7909 26 SEP 80 08:53:11

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	+125 DEG C LO-LIM	+125 DEG C DATA	+125 DEG C HI-LIM	
VIO(+CM) AT 3.5V,-26.5V	-5.00	-826.M	5.00	-3.00	-1.21	3.00	-5.00	-1.49	5.00	MV
VIO(-CM) AT 26.5V,-3.5V	-5.00	-116.M	5.00	-3.00	-673.M	3.00	-5.00	-999.M	5.00	MV
VIO(0CM) AT 15.0V,-15.0V	-5.00	-405.M	5.00	-3.00	-798.M	3.00	-5.00	-1.16	5.00	MV
VIO(-CM) AT 7.0V,-3.0V	-5.00	-384.M	5.00	-3.00	-863.M	3.00	-5.00	-1.18	5.00	MV
VIO(+CM) AT 3.0V,-7.0V	-5.00	-933.M	5.00	-3.00	-1.32	3.00	-5.00	-1.55	5.00	MV
DELTA VIO/DELTA T (0CM)	-20.0	-4.92	20.0	0.00	0.00	0.00	-20.0	3.57	20.0	UV/DEG C
IIB(+CM) AT 3.5V,-26.5V	-75.0	20.5	75.0	1.00	5.43	25.0	-75.0	-1.77	75.0	NA
IIB(-CM) AT 26.5V,-3.5V	-75.0	19.6	75.0	1.00	5.36	25.0	-75.0	-7.96	75.0	NA
IIB(0CM) AT 15.0V,-15.0V	-75.0	19.4	75.0	1.00	5.43	25.0	-75.0	-5.30	75.0	NA
IIB(-CM) AT 7.0V,-3.0V	-75.0	20.5	75.0	1.00	5.50	25.0	-75.0	-2.68	75.0	NA
IIB(+CM) AT 3.0V,-7.0V	-75.0	21.4	75.0	1.00	5.51	25.0	-75.0	-1.28	75.0	NA
INPUT IMPEDANCE (ZI)	1.00	25.7	500.	2.00	365.	500.	1.00	3.71	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	167.M	4.00	0.00	303.M	2.00	0.00	200.M	4.00	OHMS
RBC-SERIES CMG RESISTANCE	100.	275.	600.	100.	303.	400.	100.	372.	600.	OHMS
GAIN ERROR (+/-11.5V CM)	-20.0M	-3.65M	20.0M	-5.00M	-2.09M	5.00M	-20.0M	-4.67M	20.0M	%
GAIN ERROR (+/-2.0V CM)	-40.0M	-16.0M	40.0M	-20.0M	-10.5M	20.0M	-40.0M	-12.5M	40.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	13.6	30.0	6.00	15.7	30.0	6.00	19.1	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-5.32 *	-6.00	-30.0	-6.70	-6.00	-30.0	-7.66	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	102.	200.	80.0	122.	200.	80.0	108.	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	98.7	200.	80.0	104.	200.	80.0	112.	200.	dB
FEEDTHRU REJ 0V TO 15V IN	80.0	92.6	200.	86.0	93.9	200.	80.0	92.9	200.	dB
FEEDTHRU REJ 15V TO 0V IN	80.0	95.7	200.	86.0	92.6	200.	80.0	87.6	200.	dB
FEEDTHRU REJ 0V TO-15V IN	80.0	93.1	200.	86.0	87.2	200.	80.0	87.1	200.	dB
FEEDTHRU REJ -15V TO 0V	80.0	53.7 *	200.	86.0	90.7	200.	80.0	96.9	200.	dB
HOLD STEP VOLTAGE (VHS+)	-5.00	160.M	5.00	-2.00	-315.M	2.00	-5.00	-1.22	5.00	MV
HOLD STEP VOLTAGE (VHS-)	-5.00	-275.M	5.00	-2.00	-815.M	2.00	-5.00	-2.06	5.00	MV
ICC-SUPPLY CURRENT (15V)	0.00	5.11	6.50	0.00	4.53	5.50	0.00	4.05	5.00	MA
IIH-LOGIC INPUT	0.00	2.09	20.0	0.00	1.06	10.0	0.00	675.M	20.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	1.35	20.0	0.00	565.M	10.0	0.00	325.M	20.0	UA
IIL-LOGIC INPUT	-3.00K	-650.M	3.00K	-1.00K	-1.30	1.00K	-3.00K	-1.20	3.00K	MA
IIL-LOGIC REFERENCE INPUT	-3.00K	-1.00	3.00K	-1.00K	-500.M	1.00K	-3.00K	-3.50	3.00K	MA
OUTPUT SHORT CIRCUIT (+)	-20.0	-13.8	0.00	-20.0	-10.2	0.00	-20.0	-6.25	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	13.1	20.0	0.00	12.6	20.0	0.00	9.35	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	0.00	-1.50	0.00	-100.	-14.0	100.	-100.K	-13.7K	100.K	PA
HOLD CAPACITOR LEAKAGE(-)	0.00	-7.00	0.00	-100.	1.00	100.	-100.K	10.3K	100.K	PA
HOLD CAP CHRG CURRENT(+)	-100.	-7.14	-2.00	-100.	-5.91	-3.00	-100.	-4.36	-2.00	MA
HOLD CAP CHRG CURRENT(-)	2.00	5.09	100.	3.00	7.72	100.	2.00	7.05	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	1.17	2.00	800.M	1.26	2.00	800.M	850.M	2.00	V
TAO (VIN-0V TO 10V STEP)	0.00	23.7	50.0	0.00	24.8	25.0	0.00	26.0	50.0	USEC
TAO (VIN-0V TO -10V STEP)	0.00	21.6	50.0	0.00	21.5	25.0	0.00	50.0	50.0	USEC
TAO (VIN=-10V TO 0V STEP)	0.00	22.6	50.0	0.00	22.6	25.0	0.00	50.0	50.0	USEC
TAO (VIN=10V TO 0V STEP)	0.00	21.5	50.0	0.00	21.3	25.0	0.00	30.0	50.0	USEC
TAP (VIN-0V TO 10V STEP)	0.00	60.0	400.	0.00	115.	200.	0.00	245.	400.	NSEC
TAP (VIN-0V TO -10V STEP)	0.00	30.0	400.	0.00	90.0	200.	0.00	185.	400.	NSEC
TAP (VIN=-10V TO 0V STEP)	0.00	55.0	400.	0.00	115.	200.	0.00	500. *	400.	NSEC
TAP (VIN=10V TO 0V STEP)	0.00	35.0	400.	0.00	95.0	200.	0.00	195.	400.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-7. Typical Mfr. Code A Device Data Sheet.

MANUFACTURER CODE: A DEVICE TYPE: 198 ; S/N: 34 ; DATE CODE: 7909 26 SEP 80 08:53:30

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	+125 DEG C LO-LIM	+125 DEG C DATA	+125 DEG C HI-LIM	
VIO(+CM) AT 3.5V,-26.5V	-5.00	-834.M	5.00	-3.00	-795.M	3.00	-5.00	-885.M	5.00	MV
VIO(-CM) AT 26.5V,-3.5V	-5.00	-87.1M	5.00	-3.00	-283.M	3.00	-5.00	-477.M	5.00	MV
VIO(DCM) AT 15.0V,-15.0V	-5.00	-307.M	5.00	-3.00	-288.M	3.00	-5.00	-494.M	5.00	MV
VIO(-CM) AT 7.0V,-3.0V	-5.00	-452.M	5.00	-3.00	-514.M	3.00	-5.00	-681.M	5.00	MV
VIO(+CM) AT 3.0V,-7.0V	-5.00	-987.M	5.00	-3.00	-960.M	3.00	-5.00	-1.01	5.00	MV
DELTA VIO/DELTA T (DCM)	-20.0	838.M	20.0	0.00	0.00	0.00	-20.0	2.06	20.0	UV/DEG C
IIB(+CM) AT 3.5V,-26.5V	-75.0	46.0	75.0	1.00	19.6	25.0	-75.0	4.97	75.0	NA
IIB(-CM) AT 26.5V,-3.5V	-75.0	43.2	75.0	1.00	19.3	25.0	-75.0	-2.79	75.0	NA
IIB(DCM) AT 15.0V,-15.0V	-75.0	43.9	75.0	1.00	19.6	25.0	-75.0	681.M	75.0	NA
IIB(-CM) AT 7.0V,-3.0V	-75.0	44.1	75.0	1.00	19.8	25.0	-75.0	3.97	75.0	NA
IIB(+CM) AT 3.0V,-7.0V	-75.0	45.7	75.0	1.00	20.4	25.0	-75.0	6.03	75.0	NA
INPUT IMPEDANCE (ZI)	1.00	12.3	500.	2.00	68.8	500.	1.00	2.96	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	-49.2	4.00	0.00	556.M	2.00	0.00	573.M	4.00	OHMS
RSC-SERIES CHG RESISTANCE	100.	277.	600.	100.	301.	400.	100.	367.	600.	OHMS
GAIN ERROR (+/-11.5V CM)	-20.0M	-4.04M	20.0M	-5.00M	-2.80M	5.00M	-20.0M	-5.00M	20.0M	%
GAIN ERROR (+/-2.0V CM)	-40.0M	-17.3M	40.0M	-20.0M	-14.2M	20.0M	-40.0M	-12.9M	40.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	15.5	30.0	6.00	18.9	30.0	6.00	22.6	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-7.20	-6.00	-30.0	-8.44	-6.00	-30.0	-9.38	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	95.6	200.	80.0	94.0	200.	80.0	98.7	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	112.	200.	80.0	102.	200.	80.0	104.	200.	dB
FEEDTHRU REJ 0V TO 15V IN	80.0	89.1	200.	86.0	94.6	200.	80.0	86.8	200.	dB
FEEDTHRU REJ 15V TO 0V IN	80.0	95.0	200.	86.0	89.2	200.	80.0	93.8	200.	dB
FEEDTHRU REJ 0V TO-15V IN	80.0	92.3	200.	86.0	83.2 *	200.	80.0	82.4	200.	dB
FEEDTHRU REJ -15V TO 0V	80.0	45.3 *	200.	86.0	74.3 *	200.	80.0	95.9	200.	dB
HOLD STEP VOLTAGE (VHS+)	-5.00	175.M	5.00	-2.00	175.M	2.00	-5.00	90.4M	5.00	MV
HOLD STEP VOLTAGE (VHS-)	-5.00	-34.6M	5.00	-2.00	-500.M	2.00	-5.00	-1.74	5.00	MV
ICC-SUPPLY CURRENT (15V)	0.00	4.74	6.50	0.00	4.50	5.50	0.00	4.48	5.00	MA
IIH-LOGIC INPUT	0.00	4.55	20.0	0.00	2.56	10.0	0.00	1.79	20.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	2.11	20.0	0.00	1.26	10.0	0.00	880.M	20.0	UA
IIL-LOGIC INPUT	-3.00K	-1.05	3.00K	-1.00K	-800.M	1.00K	-3.00K	300.M	3.00K	MA
IIL-LOGIC REFERENCE INPUT	-3.00K	-450.M	3.00K	-1.00K	-1.05	1.00K	-3.00K	-4.25	3.00K	MA
OUTPUT SHORT CIRCUIT (+)	-20.0	-14.5	0.00	-20.0	-10.8	0.00	-20.0	-7.00	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	18.2	20.0	0.00	11.2	20.0	0.00	11.2	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	0.00	-2.50	0.00	-100.	-18.5	100.	-100.K	-13.8K	100.K	PA
HOLD CAPACITOR LEAKAGE(-)	0.00	-3.00	0.00	-100.	9.50	100.	-100.K	-3.99K	100.K	PA
HOLD CAP CHRG CURRENT(+)	-100.	-7.03	-2.00	-100.	-5.75	-3.00	-100.	-4.36	-2.00	MA
HOLD CAP CHRG CURRENT(-)	2.00	5.23	100.	3.00	5.11	100.	2.00	4.17	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	1.44	2.00	800.M	1.26	2.00	800.M	900.M	2.00	V
TAQ (VIN=0V TO 10V STEP)	0.00	22.6	50.0	0.00	24.0	25.0	0.00	26.7	50.0	USEC
TAQ (VIN=0V TO -10V STEP)	0.00	21.6	50.0	0.00	22.5	25.0	0.00	26.0	50.0	USEC
TAQ (VIN=-10V TO 0V STEP)	0.00	23.6	50.0	0.00	23.6	25.0	0.00	26.2	50.0	USEC
TAQ (VIN=10V TO 0V STEP)	0.00	21.9	50.0	0.00	22.1	25.0	0.00	24.6	50.0	USEC
TAP (VIN=0V TO 10V STEP)	0.00	35.0	400.	0.00	80.0	200.	0.00	185.	400.	NSEC
TAP (VIN=0V TO -10V STEP)	0.00	495. *	400.	0.00	50.0	200.	0.00	130.	400.	NSEC
TAP (VIN=-10V TO 0V STEP)	0.00	35.0	400.	0.00	75.0	200.	0.00	170.	400.	NSEC
TAP (VIN=10V TO 0V STEP)	0.00	15.0	400.	0.00	60.0	200.	0.00	140.	400.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-8. Typical Mfr. Code A Device Data Sheet.

MANUFACTURER CODE: B DEVICE TYPE: 198 ; S/N: 54 ; DATE CODE: 7833 26 SEP 80 08:56:01

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	+125 DEG C LO-LIM	+125 DEG C DATA	+125 DEG C HI-LIM	
VIO(+CM) AT 3.5V,-26.5V	-5.00	473.M	5.00	-3.00	936.M	3.00	-5.00	740.M	5.00	MV
VIO(-CM) AT 26.5V,-3.5V	-5.00	972.M	5.00	-3.00	1.44	3.00	-5.00	1.24	5.00	MV
VIO(0CM) AT 16.0V,-15.0V	-5.00	876.M	5.00	-3.00	1.36	3.00	-5.00	1.13	5.00	MV
VIO(-CM) AT 7.0V,-3.0V	-5.00	856.M	5.00	-3.00	1.36	3.00	-5.00	1.20	5.00	MV
VIO(+CM) AT 3.0V,-7.0V	-5.00	525.M	5.00	-3.00	1.04	3.00	-5.00	906.M	5.00	MV
DELTA VIO/DELTA T (0CM)	-20.0	6.08	20.0	0.00	0.00	0.00	-20.0	2.31	20.0	UV/DEG C
IIB(+CM) AT 3.5V,-26.5V	-75.0	21.3	75.0	1.00	6.97	25.0	-75.0	1.02	75.0	NA
IIB(-CM) AT 26.5V,-3.5V	-75.0	21.0	75.0	1.00	7.02	25.0	-75.0	-3.83	75.0	NA
IIB(0CM) AT 15.0V,-15.0V	-75.0	21.1	75.0	1.00	7.28	25.0	-75.0	-1.65	75.0	NA
IIB(-CM) AT 7.0V,-3.0V	-75.0	21.5	75.0	1.00	7.52	25.0	-75.0	758.M	75.0	NA
IIB(+CM) AT 3.0V,-7.0V	-75.0	21.9	75.0	1.00	7.77	25.0	-75.0	1.67	75.0	NA
INPUT IMPEDANCE (ZI)	1.00	72.7	500.	2.00	440.	500.	1.00	4.74	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	130.M	4.00	0.00	182.M	2.00	0.00	241.M	4.00	OHMS
RSC-SERIES CHG RESISTANCE	100.	149.	600.	100.	166.	400.	100.	213.	600.	OHMS
GAIN ERROR (+/-11.5V CM)	-20.0M	-2.17M	20.0M	-5.00M	-2.17M	5.00M	-20.0M	-4.05M	20.0M	%
GAIN ERROR (+/-2.0V CM)	-40.0M	-8.00M	40.0M	-20.0M	-8.18M	20.0M	-40.0M	-9.80M	40.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	13.2	30.0	6.00	16.3	30.0	6.00	18.8	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-10.4	-6.00	-30.0	-13.3	-6.00	-30.0	-17.1	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	104.	200.	80.0	104.	200.	80.0	110.	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	110.	200.	80.0	110.	200.	80.0	107.	200.	dB
FEEDTHRU REJ 0V TO 15V IN	80.0	93.0	200.	86.0	93.9	200.	80.0	89.1	200.	dB
FEEDTHRU REJ 15V TO 0V IN	80.0	95.3	200.	86.0	92.2	200.	80.0	91.6	200.	dB
FEEDTHRU REJ 0V TO-15V IN	80.0	101.	200.	86.0	94.8	200.	80.0	91.9	200.	dB
FEEDTHRU REJ -15V TO 0V	80.0	98.2	200.	86.0	89.7	200.	80.0	87.5	200.	dB
HOLD STEP VOLTAGE (VHS+)	-5.00	481.M	5.00	-2.00	508.M	2.00	-5.00	434.M	5.00	MV
HOLD STEP VOLTAGE (VHS-)	-5.00	-201.M	5.00	-2.00	-823.M	2.00	-5.00	-1.72	5.00	MV
ICC-SUPPLY CURRENT (15V)	0.00	4.92	6.50	0.00	4.34	5.50	0.00	3.72	5.00	MA
IIH-LOGIC INPUT	0.00	3.31	20.0	0.00	1.53	10.0	0.00	895.M	20.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	3.27	20.0	0.00	1.58	10.0	0.00	935.M	20.0	UA
IIL-LOGIC INPUT	-3.00K	-950.M	3.00K	-1.00K	-800.M	1.00K	-3.00K	2.95	3.00K	MA
IIL-LOGIC REFERENCE INPUT	-3.00K	-100.M	3.00K	-1.00K	-750.M	1.00K	-3.00K	-2.05	3.00K	MA
OUTPUT SHORT CIRCUIT (+)	-20.0	-18.7	0.00	-20.0	-13.3	0.00	-20.0	-8.25	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	15.0	20.0	0.00	12.3	20.0	0.00	8.20	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	0.00	-12.3	0.00	-100.	-37.5	100.	-100.K	-13.1K	100.K	PA
HOLD CAPACITOR LEAKAGE(-)	0.00	-5.90	0.00	-100.	-21.2	100.	-100.K	-6.90K	100.K	PA
HOLD CAP CHRG CURRENT(+)	-100.	-10.2	-2.00	-100.	-9.72	-3.00	-100.	-7.37	-8.00	MA
HOLD CAP CHRG CURRENT(-)	2.00	8.15	100.	3.00	7.17	100.	2.00	6.91	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	1.60	2.00	800.M	1.26	2.00	800.M	830.M	2.00	V
TAD (VIN-0V TO 10V STEP)	0.00	12.4	50.0	0.00	12.3	25.0	0.00	14.4	50.0	USEC
TAD (VIN-0V TO -10V STEP)	0.00	11.1	50.0	0.00	12.7	25.0	0.00	18.8	50.0	USEC
TAD (VIN=-10V TO 0V STEP)	0.00	12.2	50.0	0.00	12.3	25.0	0.00	14.3	50.0	USEC
TAD (VIN=10V TO 0V STEP)	0.00	11.0	50.0	0.00	12.2	25.0	0.00	17.6	50.0	USEC
TAP (VIN-0V TO 10V STEP)	0.00	75.0	400.	0.00	140.	200.	0.00	345.	400.	NSEC
TAP (VIN-0V TO -10V STEP)	0.00	120.	400.	0.00	225.	200.	0.00	385.	400.	NSEC
TAP (VIN=-10V TO 0V STEP)	0.00	85.0	400.	0.00	130.	200.	0.00	340.	400.	NSEC
TAP (VIN=10V TO 0V STEP)	0.00	130.	400.	0.00	245.	200.	0.00	385.	400.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-9. Typical Mfr. Code B Device Data Sheet.

MANUFACTURER CODE: B DEVICE TYPE: 198 ; S/N: 56 ; DATE CODE: 7833 26 SEP 80 08:56:19

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	+125 DEG C LO-LIM	+125 DEG C DATA	+125 DEG C HI-LIM	
VIO(+CM) AT 3.5V,-26.5V	-5.00	-7.25M	5.00	-3.00	-21.1M	3.00	-5.00	-78.6M	5.00	MV
VIO(-CM) AT 26.5V,-3.5V	-5.00	364.M	5.00	-3.00	353.M	3.00	-5.00	333.M	5.00	MV
VIO(0CM) AT 15.0V,-15.0V	-5.00	274.M	5.00	-3.00	276.M	3.00	-5.00	203.M	5.00	MV
VIO(-CM) AT 7.0V,-3.0V	-5.00	342.M	5.00	-3.00	356.M	3.00	-5.00	302.M	5.00	MV
VIO(+CM) AT 3.0V,-7.0V	-5.00	101.M	5.00	-3.00	115.M	3.00	-5.00	61.6M	5.00	MV
DELTA VIO/DELTA T (0CM)	-20.0	31.1M	20.0	0.00	0.00	0.00	-20.0	733.M	20.0	UV/DEG C
IIB(+CM) AT 3.5V,-26.5V	-75.0	17.7	75.0	1.00	6.30	25.0	-75.0	404.M	75.0	NA
IIB(-CM) AT 26.5V,-3.5V	-75.0	17.2	75.0	1.00	6.14	25.0	-75.0	-7.71	75.0	NA
IIB(0CM) AT 15.0V,-15.0V	-75.0	17.2	75.0	1.00	6.30	25.0	-75.0	-4.23	75.0	NA
IIB(-CM) AT 7.0V,-3.0V	-75.0	17.7	75.0	1.00	6.38	25.0	-75.0	-879.M	75.0	NA
IIB(+CM) AT 3.0V,-7.0V	-75.0	18.0	75.0	1.00	6.44	25.0	-75.0	433.M	75.0	NA
INPUT IMPEDANCE (ZI)	1.00	48.7	500.	2.00	140.	500.	1.00	2.83	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	125.M	4.00	0.00	175.M	2.00	0.00	200.M	4.00	OHMS
RSC-SERIES CHG RESISTANCE	100.	148.	600.	100.	164.	400.	100.	208.	600.	OHMS
GAIN ERROR (+/-11.5V CM)	-20.0M	-1.63M	20.0M	-5.00M	-1.78M	5.00M	-20.0M	-5.20M	20.0M	%
GAIN ERROR (+/-2.0V CM)	-40.0M	-7.38M	40.0M	-20.0M	-6.50M	20.0M	-40.0M	-9.28M	40.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	12.2	30.0	6.00	14.9	30.0	6.00	17.5	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-11.5	-6.00	-30.0	-14.6	-6.00	-30.0	-18.0	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	116.	200.	80.0	113.	200.	80.0	124.	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	104.	200.	80.0	105.	200.	80.0	103.	200.	dB
FEEDTHRU REJ 0V TO 15V IN	80.0	91.2	200.	86.0	90.3	200.	80.0	87.9	200.	dB
FEEDTHRU REJ 15V TO 0V IN	80.0	95.7	200.	86.0	94.2	200.	80.0	94.0	200.	dB
FEEDTHRU REJ 0V TO-15V IN	80.0	104.	200.	86.0	99.1	200.	80.0	93.9	200.	dB
FEEDTHRU REJ -15V TO 0V	80.0	89.1	200.	86.0	93.3	200.	80.0	91.5	200.	dB
HOLD STEP VOLTAGE (VHS+)	-5.00	180.M	5.00	-2.00	70.4M	2.00	-5.00	-150.M	5.00	MV
HOLD STEP VOLTAGE (VHS-)	-5.00	-265.M	5.00	-2.00	-845.M	2.00	-5.00	-1.34	5.00	MV
ICC-SUPPLY CURRENT (15V)	0.00	4.43	6.50	0.00	4.02	5.50	0.00	3.47	5.00	MA
IIH-LOGIC INPUT	0.00	2.52	20.0	0.00	1.16	10.0	0.00	685.M	20.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	2.86	20.0	0.00	1.32	10.0	0.00	765.M	20.0	UA
IIL-LOGIC INPUT	-3.00K	-1.25	3.00K	-1.00K	-1.05	1.00K	-3.00K	950.M	3.00K	NA
IIL-LOGIC REFERENCE INPUT	-3.00K	-750.M	3.00K	-1.00K	-300.M	1.00K	-3.00K	-1.65	3.00K	NA
OUTPUT SHORT CIRCUIT (+)	-20.0	-18.4	0.00	-20.0	-13.0	0.00	-20.0	-8.00	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	14.9	20.0	0.00	12.4	20.0	0.00	8.20	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	0.00	-17.5	0.00	-100.	-50.5	100.	-100.K	-6.60K	100.K	PA
HOLD CAPACITOR LEAKAGE(-)	0.00	-9.00	0.00	-100.	-24.5	100.	-100.K	-1.22K	100.K	PA
HOLD CAP CHRG CURRENT(+)	-100.	-10.2	-2.00	-100.	-9.48	-3.00	-100.	-7.16	-2.00	MA
HOLD CAP CHRG CURRENT(-)	2.00	7.86	100.	3.00	6.92	100.	2.00	5.70	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	1.62	2.00	800.M	1.28	2.00	800.M	850.M	2.00	V
TRD (VIN=0V TO 10V STEP)	0.00	12.8	50.0	0.00	12.3	25.0	0.00	17.5	50.0	USEC
TRD (VIN=0V TO -10V STEP)	0.00	13.9	50.0	0.00	16.6	25.0	0.00	20.4	50.0	USEC
TRD (VIN=-10V TO 0V STEP)	0.00	18.7	50.0	0.00	12.4	25.0	0.00	17.2	50.0	USEC
TRD (VIN=10V TO 0V STEP)	0.00	13.2	50.0	0.00	15.4	25.0	0.00	18.9	50.0	USEC
TRP (VIN=0V TO 10V STEP)	0.00	55.0	400.	0.00	115.	200.	0.00	205.	400.	NSEC
TRP (VIN=0V TO -10V STEP)	0.00	90.0	400.	0.00	190.	200.	0.00	320.	400.	NSEC
TRP (VIN=-10V TO 0V STEP)	0.00	50.0	400.	0.00	110.	200.	0.00	200.	400.	NSEC
TRP (VIN=10V TO 0V STEP)	0.00	100.	400.	0.00	205.	200.	0.00	345.	400.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-10. Typical Mfr. Code B Device Data Sheet.

MANUFACTURER CODE: B DEVICE TYPE: 198 ; S/N: 57 ; DATE CODE: 7833 26 SEP 80 08:56:38

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	+125 DEG C LO-LIM	+125 DEG C DATA	+125 DEG C HI-LIM	
VIO(+CM) AT 3.5V,-86.5V	-5.00	855.M	5.00	-3.00	1.06	3.00	-5.00	975.M	5.00	MV
VIO(-CM) AT 86.5V,-3.5V	-5.00	1.32	5.00	-3.00	1.52	3.00	-5.00	1.67	5.00	MV
VIO(@CM) AT 15.0V,-15.0V	-5.00	1.24	5.00	-3.00	1.42	3.00	-5.00	1.38	5.00	MV
VIO(-CM) AT 7.0V,-3.0V	-5.00	1.28	5.00	-3.00	1.44	3.00	-5.00	1.40	5.00	MV
VIO(+CM) AT 3.0V,-7.0V	-5.00	948.M	5.00	-3.00	1.13	3.00	-5.00	1.11	5.00	MV
DELTA VIO/DELTA T (@CM)	-20.0	2.26	20.0	0.00	0.00	0.00	-20.0	257.M	20.0	UV/DEG C
IIB(+CM) AT 3.5V,-86.5V	-75.0	16.5	75.0	1.00	6.12	25.0	-75.0	227.M	75.0	NA
IIB(-CM) AT 86.5V,-3.5V	-75.0	16.2	75.0	1.00	5.93	25.0	-75.0	-14.6	75.0	NA
IIB(@CM) AT 15.0V,-15.0V	-75.0	16.2	75.0	1.00	5.97	25.0	-75.0	-8.28	75.0	NA
IIB(-CM) AT 7.0V,-3.0V	-75.0	16.6	75.0	1.00	6.11	25.0	-75.0	-1.48	75.0	NA
IIB(+CM) AT 3.0V,-7.0V	-75.0	16.8	75.0	1.00	6.23	25.0	-75.0	612.M	75.0	NA
INPUT IMPEDANCE (ZI)	1.00	79.3	500.	2.00	122.	500.	1.00	1.55	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	75.0M	4.00	0.00	163.M	2.00	0.00	175.M	4.00	OHMS
RSC-SERIES CHG RESISTANCE	100.	143.	600.	100.	160.	400.	100.	200.	600.	OHMS
GAIN ERROR (+/-11.5V CM)	-20.0M	-2.24M	20.0M	-5.00M	-2.09M	5.00M	-20.0M	-8.77M	20.0M	%
GAIN ERROR (+/-2.0V CM)	-40.0M	-8.13M	40.0M	-20.0M	-8.07M	20.0M	-40.0M	-11.7M	40.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	13.4	30.0	6.00	16.0	30.0	6.00	18.5	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-9.81	-6.00	-30.0	-13.3	-6.00	-30.0	-16.8	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	110.	200.	80.0	104.	200.	80.0	105.	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	104.	200.	80.0	108.	200.	80.0	104.	200.	dB
FEEDTHRU REJ 0V TO 15V IN	80.0	98.9	200.	86.0	91.9	200.	80.0	90.1	200.	dB
FEEDTHRU REJ 15V TO 0V IN	80.0	89.9	200.	86.0	92.4	200.	80.0	97.3	200.	dB
FEEDTHRU REJ 0V TO-15V IN	80.0	96.8	200.	86.0	96.7	200.	80.0	93.8	200.	dB
FEEDTHRU REJ -15V TO 0V	80.0	94.0	200.	86.0	87.9	200.	80.0	94.0	200.	dB
HOLD STEP VOLTAGE (VHS+)	-5.00	263.M	5.00	-2.00	59.4M	2.00	-5.00	-89.1M	5.00	MV
HOLD STEP VOLTAGE (VHS-)	-5.00	-491.M	5.00	-2.00	-1.24	2.00	-5.00	-2.14	5.00	MV
ICC-SUPPLY CURRENT (15V)	0.00	5.06	6.50	0.00	4.23	5.50	0.00	3.60	5.00	MA
IIH-LOGIC INPUT	0.00	2.50	20.0	0.00	1.13	10.0	0.00	650.M	20.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	2.47	20.0	0.00	1.10	10.0	0.00	620.M	20.0	UA
IIL-LOGIC INPUT	-3.00K	-1.45	3.00K	-1.00K	-1.65	1.00K	-3.00K	400.M	3.00K	MA
IIL-LOGIC REFERENCE INPUT	-3.00K	-450.M	3.00K	-1.00K	-450.M	1.00K	-3.00K	-2.45	3.00K	MA
OUTPUT SHORT CIRCUIT (+)	-20.0	-20.5 *	0.00	-20.0	-14.4	0.00	-20.0	-8.95	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	14.0	20.0	0.00	11.4	20.0	0.00	7.70	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	0.00	-9.40	0.00	-100.	-36.7	100.	-100.K	-12.9K	100.K	PA
HOLD CAPACITOR LEAKAGE(-)	0.00	-5.80	0.00	-100.	-9.00	100.	-100.K	-5.03K	100.K	PA
HOLD CAP CHRG CURRENT(+)	-100.	-10.2	-2.00	-100.	-9.87	-3.00	-100.	-7.41	-2.00	MA
HOLD CAP CHRG CURRENT(-)	2.00	8.27	100.	3.00	7.15	100.	2.00	6.82	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	1.59	2.00	800.M	1.25	2.00	800.M	880.M	2.00	V
TAD (VIN=0V TO 10V STEP)	0.00	11.4	50.0	0.00	13.7	85.0	0.00	17.5	50.0	USEC
TAD (VIN=0V TO -10V STEP)	0.00	13.9	50.0	0.00	15.8	85.0	0.00	20.1	50.0	USEC
TAD (VIN=-10V TO 0V STEP)	0.00	11.3	50.0	0.00	12.6	85.0	0.00	17.0	50.0	USEC
TAD (VIN=10V TO 0V STEP)	0.00	12.9	60.0	0.00	15.0	25.0	0.00	19.0	50.0	USEC
TAP (VIN=0V TO 10V STEP)	0.00	80.0	400.	0.00	155.	200.	0.00	275.	400.	NSEC
TAP (VIN=0V TO -10V STEP)	0.00	115.	400.	0.00	225. *	200.	0.00	370.	400.	NSEC
TAP (VIN=-10V TO 0V STEP)	0.00	75.0	400.	0.00	150.	200.	0.00	265.	400.	NSEC
TAP (VIN=10V TO 0V STEP)	0.00	125.	400.	0.00	245. *	200.	0.00	405. *	400.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-11. Typical Mfr. Code B Device Data Sheet.

MANUFACTURER CODE: C DEVICE TYPE: 5537 ; S/N: 82 ; DATE CODE: 7946 28 SEP 80 00:01:00

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	+125 DEG C LO-LIM	+125 DEG C DATA	+125 DEG C HI-LIM	
VIO(+CM) AT 3.5V,-26.5V	-5.00	418.M	5.00	-3.00	-200.M	3.00	-5.00	-1.21	5.00	MV
VIO(-CM) AT 26.5V,-3.5V	-5.00	1.33	5.00	-3.00	659.M	3.00	-5.00	-162.M	5.00	MV
VIO(0CM) AT 15.0V,-15.0V	-5.00	767.M	5.00	-3.00	149.M	3.00	-5.00	-683.M	5.00	MV
VIO(-CM) AT 7.0V,-3.0V	-5.00	788.M	5.00	-3.00	165.M	3.00	-5.00	-684.M	5.00	MV
VIO(+CM) AT 3.0V,-7.0V	-5.00	364.M	5.00	-3.00	-208.M	3.00	-5.00	-1.04	5.00	MV
DELTA VIO/DELTA T (0CM)	-20.0	-7.73	20.0	0.00	0.00	0.00	-20.0	8.32	20.0	UV/DEG C
IIB(+CM) AT 3.5V,-26.5V	-75.0	8.28	75.0	1.00	3.03	25.0	-75.0	-3.29	75.0	NA
IIB(-CM) AT 26.5V,-3.5V	-75.0	8.00	75.0	1.00	2.88	25.0	-75.0	-11.3	75.0	NA
IIB(0CM) AT 15.0V,-15.0V	-75.0	8.15	75.0	1.00	3.02	25.0	-75.0	-6.61	75.0	NA
IIB(-CM) AT 7.0V,-3.0V	-75.0	8.23	75.0	1.00	2.91	25.0	-75.0	-4.12	75.0	NA
IIB(+CM) AT 3.0V,-7.0V	-75.0	8.36	75.0	1.00	2.85	25.0	-75.0	-2.76	75.0	NA
INPUT IMPEDANCE (ZI)	1.00	82.6	500.	2.00	155.	500.	1.00	2.86	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	50.0M	4.00	0.00	100.M	2.00	0.00	125.M	4.00	OHMS
RSC-SERIES CHG RESISTANCE	100.	273.	600.	100.	288.	400.	100.	359.	600.	OHMS
GAIN ERROR (+/-11.5V CM)	-20.0M	-4.05M	20.0M	-5.00M	-3.80M	5.00M	-20.0M	-7.21M	20.0M	%
GAIN ERROR (+/-2.0V CM)	-40.0M	-11.0M	40.0M	-20.0M	-9.00M	20.0M	-40.0M	-12.1M	40.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	10.7	30.0	6.00	12.4	30.0	6.00	13.8	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-14.7	-6.00	-30.0	-19.2	-6.00	-30.0	-23.6	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	99.6	200.	80.0	99.8	200.	80.0	93.6	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	142.	200.	80.0	122.	200.	80.0	116.	200.	dB
FEEDTHRU REJ 0V TO 15V IN	80.0	93.0	200.	86.0	96.3	200.	80.0	87.2	200.	dB
FEEDTHRU REJ 15V TO 0V IN	80.0	92.6	200.	86.0	90.9	200.	80.0	88.1	200.	dB
FEEDTHRU REJ 0V TO-15V IN	80.0	91.2	200.	86.0	93.3	200.	80.0	93.9	200.	dB
FEEDTHRU REJ -15V TO 0V	80.0	95.0	200.	86.0	90.9	200.	80.0	90.8	200.	dB
HOLD STEP VOLTAGE (VHS+)	-5.00	14.9M	5.00	-2.00	-1.33	2.00	-5.00	-2.44	5.00	MV
HOLD STEP VOLTAGE (VHS-)	-5.00	-440.M	5.00	-2.00	-2.14	2.00	-5.00	-3.52	5.00	MV
ICC-SUPPLY CURRENT (15V)	0.00	5.71	6.50	0.00	5.23	5.50	0.00	4.87	5.00	MA
IIH-LOGIC INPUT	0.00	1.67	20.0	0.00	800.M	10.0	0.00	500.M	20.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	845.M	20.0	0.00	455.M	10.0	0.00	285.M	20.0	UA
IIL-LOGIC INPUT	-3.00K	-800.M	3.00K	-1.00K	-1.05	1.00K	-3.00K	-1.25	3.00K	MA
IIL-LOGIC REFERENCE INPUT	-3.00K	-250.M	3.00K	-1.00K	-700.M	1.00K	-3.00K	-8.80	3.00K	MA
OUTPUT SHORT CIRCUIT (+)	-20.0	-27.5	0.00	-20.0	-20.0	0.00	-20.0	-12.5	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	20.8	20.0	0.00	17.3	20.0	0.00	12.0	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	0.00	400.M	0.00	-100.	-500.M	100.	-100.K	-13.5K	100.K	PA
HOLD CAPACITOR LEAKAGE(-)	0.00	-3.25	0.00	-100.	9.00	100.	-100.K	6.63K	100.K	PA
HOLD CAP CHRG CURRENT(+)	-100.	-7.25	-2.00	-100.	-6.16	-3.00	-100.	-4.77	-2.00	MA
HOLD CAP CHRG CURRENT(-)	2.00	4.66	100.	3.00	4.70	100.	2.00	4.12	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	1.60	2.00	800.M	1.27	2.00	800.M	850.M	2.00	V
TAQ (VIN-0V TO 10V STEP)	0.00	21.3	50.0	0.00	22.5	25.0	0.00	33.2	50.0	USEC
TAQ (VIN-0V TO -10V STEP)	0.00	22.6	50.0	0.00	22.7	25.0	0.00	26.3	50.0	USEC
TAQ (VIN=-10V TO 0V STEP)	0.00	21.5	50.0	0.00	22.2	25.0	0.00	25.1	50.0	USEC
TAQ (VIN-10V TO 0V STEP)	0.00	22.5	50.0	0.00	22.6	25.0	0.00	25.8	50.0	USEC
TAP (VIN-0V TO 10V STEP)	0.00	40.0	400.	0.00	120.	200.	0.00	220.	400.	NSEC
TAP (VIN-0V TO -10V STEP)	0.00	55.0	400.	0.00	185.	200.	0.00	305.	400.	NSEC
TAP (VIN=-10V TO 0V STEP)	0.00	36.0	400.	0.00	125.	200.	0.00	230.	400.	NSEC
TAP (VIN-10V TO 0V STEP)	0.00	55.0	400.	0.00	175.	200.	0.00	320.	400.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-12. Typical Mfr. Code C Device Data Sheet.

MANUFACTURER CODE: C DEVICE TYPE: 5537 ; S/N: 83 ; DATE CODE: 7946 26 SEP 80 09:01:19

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	+125 DEG C LO-LIM	+125 DEG C DATA	+125 DEG C HI-LIM	
VIO(+CM) AT 3.5V,-86.5V	-5.00	1.83	5.00	-3.00	764.M	3.00	-5.00	8.25M	5.00	MV
VIO(-CM) AT 86.5V,-3.5V	-5.00	8.15	5.00	-3.00	1.68	3.00	-5.00	989.M	5.00	MV
VIO(0CM) AT 15.0V,-15.0V	-5.00	1.59	5.00	-3.00	1.18	3.00	-5.00	496.M	5.00	MV
VIO(-CM) AT 7.0V,-3.0V	-5.00	1.63	5.00	-3.00	1.80	3.00	-5.00	528.M	5.00	MV
VIO(+CM) AT 3.0V,-7.0V	-5.00	1.17	5.00	-3.00	815.M	3.00	-5.00	161.M	5.00	MV
DELTA VIO/DELTA T (0CM)	-20.0	-5.18	20.0	0.00	0.00	0.00	-20.0	6.83	20.0	UV/DEG C
IIB(+CM) AT 3.5V,-86.5V	-75.0	9.16	75.0	1.00	2.89	25.0	-75.0	-2.21	75.0	NA
IIB(-CM) AT 86.5V,-3.5V	-75.0	8.73	75.0	1.00	2.94	25.0	-75.0	-9.37	75.0	NA
IIB(0CM) AT 15.0V,-15.0V	-75.0	8.80	75.0	1.00	3.08	25.0	-75.0	-5.36	75.0	NA
IIB(-CM) AT 7.0V,-3.0V	-75.0	9.19	75.0	1.00	3.08	25.0	-75.0	-3.28	75.0	NA
IIB(+CM) AT 3.0V,-7.0V	-75.0	9.26	75.0	1.00	3.11	25.0	-75.0	-2.08	75.0	NA
INPUT IMPEDANCE (ZI)	1.00	53.5	500.	2.00	450.	500.	1.00	3.21	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	75.0M	4.00	0.00	125.M	2.00	0.00	100.M	4.00	OHMS
RSC-SERIES CMG RESISTANCE	100.	270.	600.	100.	287.	400.	100.	356.	600.	OHMS
GAIN ERROR (+/-11.5V CM)	-20.0M	-4.12M	20.0M	-5.00M	-3.89M	5.00M	-20.0M	-6.64M	20.0M	%
GAIN ERROR (+/-2.0V CM)	-40.0M	-11.6M	40.0M	-20.0M	-10.1M	20.0M	-40.0M	-12.4M	40.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	11.6	30.0	6.00	13.6	30.0	6.00	15.1	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-14.6	-6.00	-30.0	-18.9	-6.00	-30.0	-23.0	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	98.7	200.	80.0	98.9	200.	80.0	94.9	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	112.	200.	80.0	116.	200.	80.0	126.	200.	dB
FEEDTHRU REJ 0V TO 15V IN	80.0	92.3	200.	86.0	89.2	200.	80.0	91.3	200.	dB
FEEDTHRU REJ 15V TO 0V IN	80.0	94.2	200.	86.0	95.2	200.	80.0	88.5	200.	dB
FEEDTHRU REJ 0V TO-15V IN	80.0	99.7	200.	86.0	93.8	200.	80.0	92.7	200.	dB
FEEDTHRU REJ -15V TO 0V	80.0	94.8	200.	86.0	92.0	200.	80.0	91.9	200.	dB
HOLD STEP VOLTAGE (VHS+)	-5.00	84.4M	5.00	-2.00	-1.28	2.00	-5.00	-2.38	5.00	MV
HOLD STEP VOLTAGE (VHS-)	-5.00	-290.M	5.00	-2.00	-2.05 *	2.00	-5.00	-3.52	5.00	MV
ICC-SUPPLY CURRENT (15V)	0.00	5.59	6.50	0.00	5.12	5.50	0.00	4.81	5.00	MA
IIH-LOGIC INPUT	0.00	1.77	20.0	0.00	865.M	10.0	0.00	545.M	20.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	855.M	20.0	0.00	450.M	10.0	0.00	285.M	20.0	UA
IIL-LOGIC INPUT	-3.00K	-850.M	3.00K	-1.00K	-1.35	1.00K	-3.00K	-1.20	3.00K	MA
IIL-LOGIC REFERENCE INPUT	-3.00K	-800.M	3.00K	-1.00K	-300.M	1.00K	-3.00K	-6.85	3.00K	MA
OUTPUT SHORT CIRCUIT (+)	-20.0	-27.5 *	0.00	-20.0	-19.9	0.00	-20.0	-12.7	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	20.5 *	20.0	0.00	17.0	20.0	0.00	12.1	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	0.00	250.M	0.00	-100.	7.50	100.	-100.K	-13.6K	100.K	PA
HOLD CAPACITOR LEAKAGE(-)	0.00	-6.00	0.00	-100.	10.5	100.	-100.K	5.33K	100.K	PA
HOLD CAP CHRG CURRENT(+)	-100.	-7.33	-2.00	-100.	-6.18	-3.00	-100.	-4.82	-2.00	MA
HOLD CAP CHRG CURRENT(-)	2.00	4.34	100.	3.00	4.48	100.	2.00	4.08	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	1.60	2.00	800.M	1.27	2.00	800.M	860.M	2.00	V
TAG (VIN=0V TO 10V STEP)	0.00	21.4	50.0	0.00	21.9	25.0	0.00	25.6	50.0	USEC
TAG (VIN=0V TO -10V STEP)	0.00	22.3	50.0	0.00	22.6	25.0	0.00	25.5	50.0	USEC
TAG (VIN=-10V TO 0V STEP)	0.00	21.1	50.0	0.00	22.1	25.0	0.00	24.7	50.0	USEC
TAG (VIN=10V TO 0V STEP)	0.00	22.3	50.0	0.00	22.4	25.0	0.00	25.2	50.0	USEC
TAP (VIN=0V TO 10V STEP)	0.00	35.0	400.	0.00	120.	200.	0.00	285.	400.	NSEC
TAP (VIN=0V TO -10V STEP)	0.00	40.0	400.	0.00	175.	200.	0.00	305.	400.	NSEC
TAP (VIN=-10V TO 0V STEP)	0.00	35.0	400.	0.00	125.	200.	0.00	230.	400.	NSEC
TAP (VIN=10V TO 0V STEP)	0.00	45.0	400.	0.00	175.	200.	0.00	315.	400.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-13. Typical Mfr. Code C Device Data Sheet.

MANUFACTURER CODE: C DEVICE TYPE: 5537 ; S/N: 85 ; DATE CODE: 7946 26 SEP 80 09:01:38

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	+125 DEG C LO-LIM	+125 DEG C DATA	+125 DEG C HI-LIM	
VIO(+CM) AT 3.5V,-86.5V	-5.00	133.M	5.00	-3.00	-432.M	3.00	-5.00	-1.21	5.00	MV
VIO(-CM) AT 86.5V,-3.5V	-6.00	1.06	5.00	-3.00	535.M	3.00	-5.00	-287.M	5.00	MV
VIO(DCM) AT 15.0V,-15.0V	-5.00	517.M	5.00	-3.00	50.9M	3.00	-5.00	-768.M	5.00	MV
VIO(-CM) AT 7.0V,-3.0V	-5.00	500.M	5.00	-3.00	38.4M	3.00	-5.00	-755.M	5.00	MV
VIO(+CM) AT 3.0V,-7.0V	-5.00	48.5M	5.00	-3.00	-340.M	3.00	-5.00	-1.08	5.00	MV
DELTA VIO/DELTA T (DCM)	-20.0	-5.82	20.0	0.00	0.00	0.00	-20.0	8.19	20.0	UV/DEG C
IIB(+CM) AT 3.5V,-86.5V	-75.0	25.6	75.0	1.00	8.32	25.0	-75.0	-37.0M	75.0	NA
IIB(-CM) AT 86.5V,-3.5V	-75.0	24.3	75.0	1.00	8.49	25.0	-75.0	-9.07	75.0	NA
IIB(DCM) AT 15.0V,-15.0V	-75.0	24.8	75.0	1.00	8.86	25.0	-75.0	-3.88	75.0	NA
IIB(-CM) AT 7.0V,-3.0V	-75.0	25.2	75.0	1.00	8.94	25.0	-75.0	-1.35	75.0	NA
IIB(+CM) AT 3.0V,-7.0V	-75.0	25.7	75.0	1.00	9.21	25.0	-75.0	264.M	75.0	NA
INPUT IMPEDANCE (ZI)	1.00	17.5	500.	2.00	136.	500.	1.00	2.55	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	150.M	4.00	0.00	150.M	2.00	0.00	175.M	4.00	OHMS
RDC-SERIES CMG RESISTANCE	100.	255.	600.	100.	274.	400.	100.	340.	600.	OHMS
GAIN ERROR (+/-11.5V CM)	-20.0M	-4.43M	20.0M	-5.00M	-4.13M	5.00M	-20.0M	-7.10M	20.0M	%
GAIN ERROR (+/-2.0V CM)	-40.0M	-11.7M	40.0M	-20.0M	-10.2M	20.0M	-40.0M	-13.4M	40.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	11.1	30.0	6.00	13.0	30.0	6.00	14.4	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-17.2	-6.00	-30.0	-21.4	-6.00	-30.0	-25.7	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	99.4	200.	80.0	99.3	200.	80.0	102.	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	125.	200.	80.0	112.	200.	80.0	106.	200.	dB
FEEDTHRU REJ 0V TO 15V IN	80.0	91.0	200.	86.0	87.8	200.	80.0	90.3	200.	dB
FEEDTHRU REJ 15V TO 0V IN	80.0	92.2	200.	86.0	95.9	200.	80.0	88.2	200.	dB
FEEDTHRU REJ 0V TO-15V IN	80.0	95.6	200.	86.0	92.0	200.	80.0	93.1	200.	dB
FEEDTHRU REJ -15V TO 0V	80.0	88.9	200.	86.0	91.9	200.	80.0	93.4	200.	dB
HOLD STEP VOLTAGE (VHS+)	-5.00	317.M	5.00	-2.00	-745.M	2.00	-5.00	-2.09	5.00	MV
HOLD STEP VOLTAGE (VHS-)	-5.00	-32.1M	5.00	-2.00	-1.58	2.00	-5.00	-3.32	5.00	MV
ICC-SUPPLY CURRENT (15V)	0.00	5.75	6.50	0.00	5.39	5.50	0.00	5.04 *	5.00	MA
IIH-LOGIC INPUT	0.00	3.36	20.0	0.00	1.64	10.0	0.00	1.03	20.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	1.79	20.0	0.00	1.04	10.0	0.00	700.M	20.0	UA
IIL-LOGIC INPUT	-3.00K	-900.M	3.00K	-1.00K	-1.20	1.00K	-3.00K	-900.M	3.00K	NA
IIL-LOGIC REFERENCE INPUT	-3.00K	-350.M	3.00K	-1.00K	-50.0M	1.00K	-3.00K	-9.80	3.00K	NA
OUTPUT SHORT CIRCUIT (+)	-20.0	-29.3 *	0.00	-20.0	-21.5 *	0.00	-20.0	-13.8	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	21.4 *	20.0	0.00	18.1	20.0	0.00	13.3	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	0.00	-5.15	0.00	-100.	-8.00	100.	-100.K	-13.5K	100.K	PA
HOLD CAPACITOR LEAKAGE(-)	0.00	-18.7	0.00	-100.	-500.M	100.	-100.K	-1.92K	100.K	PA
HOLD CAP CHRG CURRENT(+)	-100.	-7.68	-2.00	-100.	-6.48	-3.00	-100.	-5.03	-2.00	MA
HOLD CAP CHRG CURRENT(-)	2.00	3.78	100.	3.00	4.27	100.	2.00	3.93	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	1.62	2.00	800.M	1.29	2.00	800.M	880.M	2.00	V
TAD (VIN=0V TO 10V STEP)	0.00	20.2	50.0	0.00	21.0	25.0	0.00	33.5	50.0	USEC
TAD (VIN=0V TO -10V STEP)	0.00	21.0	50.0	0.00	21.0	25.0	0.00	27.6	50.0	USEC
TAD (VIN=-10V TO 0V STEP)	0.00	20.3	50.0	0.00	20.6	25.0	0.00	23.6	50.0	USEC
TAD (VIN=10V TO 0V STEP)	0.00	21.0	50.0	0.00	20.7	25.0	0.00	28.4	50.0	USEC
TAP (VIN=0V TO 10V STEP)	0.00	35.0	400.	0.00	110.	200.	0.00	225.	400.	NSEC
TAP (VIN=0V TO -10V STEP)	0.00	25.0	400.	0.00	130.	200.	0.00	270.	400.	NSEC
TAP (VIN=-10V TO 0V STEP)	0.00	25.0	400.	0.00	110.	200.	0.00	220.	400.	NSEC
TAP (VIN=10V TO 0V STEP)	0.00	30.0	400.	0.00	130.	200.	0.00	280.	400.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-14. Typical Mfr. Code C Device Data Sheet.

MANUFACTURER CODE: A ; DEVICE TYPE: LF198; DATE CODE:7909 25 SEP 80 11:23:50

PARAMETER	LO-LIM	S/N 6	S/N 9	S/N19	S/N23	+25 DEG C S/N28	S/N34	S/N35	S/N41	S/N45	S/N48	HI-LIM	
VIO(+CM) AT 3.5V,-26.5V	-3.00	-1.55	-70.2M	195.M	-19.5M	-1.21	-795.M	-643.M	-924.M	551.M	-683.M	3.00	MV
VIO(-CM) AT 26.5V,-3.5V	-3.00	-1.16	381.M	684.M	418.M	-673.M	-223.M	-27.3M	-419.M	861.M	-88.4M	3.00	MV
VIO(OCM) AT 15.0V,-15.0V	-3.00	-1.25	306.M	570.M	371.M	-798.M	-288.M	-209.M	-591.M	752.M	-183.M	3.00	MV
VIO(-CM) AT 7.0V,-3.0V	-3.00	-1.36	179.M	462.M	75.5M	-863.M	-514.M	-364.M	4.76 X	881.M	-384.M	3.00	MV
VIO(+CM) AT 3.0V,-7.0V	-3.00	-1.80	-194.M	-5.85M	-452.M	-1.32	-960.M	-834.M	-1.14	326.M	-973.M	3.00	MV
DELTA VIO/DELTA T (OCM)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	UV/DEG C
IIB(+CM) AT 3.5V,-26.5V	-1.00	6.53	6.81	6.36	7.10	5.43	19.6	5.52	4.48	4.84	9.65	25.0	NA
IIB(-CM) AT 26.5V,-3.5V	-1.00	6.36	6.73	6.10	6.23	5.36	19.3	5.10	4.54	4.63	9.28	25.0	NA
IIB(OCM) AT 15.0V,-15.0V	-1.00	6.33	7.05	6.17	6.42	5.43	19.6	5.29	4.53	4.56	9.37	25.0	NA
IIB(-CM) AT 7.0V,-3.0V	-1.00	6.31	7.18	6.40	6.46	5.50	19.8	5.22	4.61	4.32	9.38	25.0	NA
IIB(OCM) AT 3.0V,-7.0V	-1.00	6.32	7.25	6.58	6.63	5.51	20.4	5.32	4.89	4.68	9.63	25.0	NA
INPUT IMPEDANCE (ZI)	2.00	137.	274.	88.7	26.4	365.	68.8	54.5	377.	107.	61.7	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	200.M	455.M	175.M	400.M	303.M	556.M	300.M	510.M	175.M	425.M	2.00	OHMS
RDC-SERIES CMG RESISTANCE	100.	321.	315.	297.	385.	303.	301.	294.	276.	301.	360.	400.	OHMS
GAIN ERROR (+/-11.5V CM)	-5.00M	-1.87M	-1.67M	-2.41M	-2.17M	-2.09M	-2.80M	-3.00M	-1.91M	-1.21M	-2.98M	5.00M	%
GAIN ERROR (+/-2.0V CM)	-20.0M	-10.6M	-8.50M	-13.2M	-14.5M	-10.5M	-14.2M	-12.9M	-151.M%	-16.1M	-16.3M	20.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	15.7	17.6	18.7	18.2	15.7	18.9	16.6	17.8	18.1	17.6	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-7.78	-6.79	-6.07	-5.53 X	-6.70	-8.44	-5.45 X	-5.19 X	-5.79 X	-5.99 X	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	98.7	98.9	101.	95.5	122.	94.0	95.6	99.3	106.	88.0	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	122.	111.	132.	100.	104.	102.	116.	104.	106.	91.0	200.	dB
FEEDTHRU REJ 0V TO 11.5V	86.0	90.1	88.5	95.2	90.4	93.9	94.6	91.4	91.5	93.2	90.4	200.	dB
FEEDTHRU REJ 11.5V TO 0V	86.0	94.5	90.6	94.6	94.8	92.6	89.2	87.9	87.4	90.4	94.7	200.	dB
FEEDTHRU REJ 0V TO -11.5V	86.0	90.1	88.5	88.2	87.9	87.2	83.2 X	88.0	67.5 X	89.6	88.8	200.	dB
FEEDTHRU REJ -11.5V TO 0V	86.0	90.6	91.9	91.8	89.1	90.7	74.3 X	92.0	95.9	98.8	88.7	200.	dB
HOLD STEP VOLTAGE (VHS+)	-2.00	25.4M	5.40M	-285.M	-370.M	-315.M	175.M	-385.M	120.M	-370.M	-280.M	2.00	MV
HOLD STEP VOLTAGE (VHS-)	-2.00	-475.M	-507.M	-1.14	-1.01	-815.M	-500.M	-885.M	-840.M	-780.M	-1.02	2.00	MV
ICC-SUPPLY CURRENT (@15V)	0.00	4.26	4.25	4.84	3.93	4.53	4.50	4.22	5.03	4.29	4.50	5.50	MA
IIH-LOGIC INPUT	0.00	980.M	1.18	1.31	1.15	1.06	2.56	1.14	1.25	970.M	1.32	10.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	605.M	615.M	630.M	635.M	565.M	1.26	530.M	595.M	440.M	700.M	10.0	UA
IIL-LOGIC INPUT	-1.00K	-1.20	-1.40	-1.60	-700.M	-1.30	-800.M	-1.15	-950.M	-950.M	-1.35	1.00K	MA
IIL-LOGIC REFERENCE INPUT	-1.00K	-300.M	-500.M	-500.M	-1.20	-500.M	-1.05	-700.M	-400.M	-1.00	-300.M	1.00K	MA
OUTPUT SHORT CIRCUIT (+)	-20.0	-10.2	-9.85	-11.6	-8.70	-10.2	-10.8	-9.90	-11.3	-10.4	-9.75	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	12.8	13.3	14.4	11.2	12.6	11.2	12.5	15.2	12.0	12.3	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	-100.	-7.50	-14.0	-20.5	-44.0	-14.0	-18.5	-18.0	-15.5	-20.7	-27.5	100.	PA
HOLD CAPACITOR LEAKAGE(-)	-100.	3.00	7.50	14.5	8.00	1.00	9.50	9.50	13.5	8.50	4.50	100.	PA
HOLD CAP CHRG CURRENT(+)	-100.	-5.67	-5.45	-5.73	-4.44	-5.81	-5.75	-5.91	-6.34	-5.81	-4.80	-3.00	MA
HOLD CAP CHRG CURRENT(-)	3.00	4.83	5.09	5.47	4.12	7.72	5.11	7.86	5.63	4.90	4.50	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	1.26	1.23	1.26	1.25	1.26	1.26	1.26	1.26	1.25	1.25	2.00	V
TAD (VIN-0V TO 10V STEP)	0.00	25.1 X	25.1 X	22.9	29.7 X	24.8	24.0	22.2	20.4	22.8	29.0 X	25.0	USEC
TAD (VIN-0V TO -10V STEP)	0.00	23.7	23.4	22.0	30.4 X	21.5	22.5	20.7	20.7	22.2	32.5 X	25.0	USEC
TAD (VIN--10V TO 0V STEP)	0.00	24.0	24.1	23.0	29.8 X	22.6	23.6	21.3	20.7	22.6	26.9 X	25.0	USEC
TAD (VIN-10V TO 0V STEP)	0.00	23.3	23.1	21.7	29.8 X	21.3	22.1	20.1	20.2	21.8	27.5 X	25.0	USEC
TAP (VIN-0V TO 10V STEP)	0.00	120.	90.0	95.0	105.	115.	80.0	120.	130.	105.	105.	200.	NSEC
TAP (VIN-0V TO -10V STEP)	0.00	85.0	55.0	70.0	85.0	90.0	60.0	95.0	90.0	80.0	85.0	200.	NSEC
TAP (VIN--10V TO 0V STEP)	0.00	120.	90.0	90.0	95.0	115.	75.0	115.	130.	105.	100.	200.	NSEC
TAP (VIN-10V TO 0V STEP)	0.00	85.0	60.0	80.0	90.0	95.0	60.0	85.0	95.0	85.0	90.0	200.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-15. Mfr. Code A Devices at 25°C.

MANUFACTURER CODE: B ; DEVICE TYPE: LF198; DATE CODE:7909 25 SEP 80 11:26:13

PARAMETER	LO-LIM	S/N61	S/N52	S/N53	S/N54	+25 DEG C S/N56	S/N57	S/N58	S/N59	S/N60	S/N61	HI-LIM	
VIO(+CM) AT 3.5V,-26.5V	-3.00	-644.M	690.M	1.69	936.M	-21.1M	1.06	431.M	665.M	164.M	-397.M	3.00	MV
VIO(-CM) AT 26.5V,-3.5V	-3.00	-137.M	1.10	2.03	1.44	353.M	1.52	999.M	1.17	590.M	-6.75M	3.00	MV
VIO(0CM) AT 15.0V,-15.0V	-3.00	-235.M	1.09	2.05	1.36	276.M	1.42	894.M	1.08	566.M	-75.8M	3.00	MV
VIO(-CM) AT 7.0V,-3.0V	-3.00	-100.M	1.14	2.05	1.36	356.M	1.44	891.M	1.10	582.M	25.3M	3.00	MV
VIO(+CM) AT 3.0V,-7.0V	-3.00	-446.M	878.M	1.79	1.04	115.M	1.13	581.M	823.M	323.M	-242.M	3.00	MV
DELTA VIO/DELTA T (0CM)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	UV/DEG C
IIB(+CM) AT 3.5V,-26.5V	-1.00	14.1	4.87	7.54	6.97	6.30	6.12	3.51	3.35	6.39	11.4	25.0	NA
IIB(-CM) AT 26.5V,-3.5V	-1.00	13.7	4.76	7.12	7.02	6.14	5.93	4.17	3.79	6.44	11.1	25.0	NA
IIB(0CM) AT 15.0V,-15.0V	-1.00	13.8	5.52	7.75	7.28	6.30	5.97	4.11	3.89	7.08	11.3	25.0	NA
IIB(-CM) AT 7.0V,-3.0V	-1.00	14.1	5.62	8.20	7.52	6.38	6.11	4.30	4.23	7.28	11.5	25.0	NA
IIB(0CM) AT 3.0V,-7.0V	-1.00	14.3	5.74	8.47	7.77	6.44	6.23	4.50	4.53	7.55	11.8	25.0	NA
INPUT IMPEDANCE (ZI)	2.00	62.3	210.	54.9	440.	140.	122.	34.7	53.0	395.	76.8	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	150.M	150.M	179.M	182.M	175.M	153.M	75.0M	163.M	175.M	152.M	2.00	OHMS
RSC-SERIES CHG RESISTANCE	100.	159.	162.	161.	166.	164.	160.	183.	173.	161.	150.	400.	OHMS
GAIN ERROR (+/-11.5V CM)	-5.00M	-2.00M	-1.73M	-1.56M	-2.17M	-1.78M	-2.09M	-2.19M	-1.87M	-1.83M	-1.83M	5.00M	%
GAIN ERROR (+/-2.0V CM)	-20.0M	-6.50M	-6.67M	-6.78M	-8.18M	-6.50M	-8.07M	-8.51M	-7.55M	-6.50M	-7.50M	20.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	14.5	15.7	17.3	16.3	14.9	16.0	15.3	15.3	15.4	14.6	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-17.5	-14.2	-12.8	-13.3	-14.6	-13.3	-14.4	-12.8	-15.9	-16.4	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	99.3	109.	122.	104.	113.	104.	104.	102.	104.	122.	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	122.	105.	105.	110.	105.	108.	112.	111.	115.	106.	200.	dB
FEEDTHRU REJ 0V TO 11.5V	86.0	87.9	91.7	99.9	93.9	90.3	91.9	91.6	91.0	91.0	100.	200.	dB
FEEDTHRU REJ 11.5V TO 0V	86.0	103.	94.0	92.0	92.2	94.2	92.4	93.7	95.3	94.4	96.5	200.	dB
FEEDTHRU REJ 0V TO -11.5V	86.0	96.6	91.9	93.4	94.8	99.1	96.7	102.	99.0	92.1	93.8	200.	dB
FEEDTHRU REJ -11.5V TO 0V	86.0	90.6	94.1	91.7	89.7	93.3	87.9	94.1	89.6	90.6	89.9	200.	dB
HOLD STEP VOLTAGE (VHS+)	-2.00	285.M	-64.1M	500.M	508.M	70.4M	59.4M	167.M	6.90M	199.M	460.M	2.00	MV
HOLD STEP VOLTAGE (VHS-)	-2.00	-570.M	-1.01	-680.M	-823.M	-845.M	-1.24	-934.M	-1.08	-941.M	-1.01	2.00	MV
ICC-SUPPLY CURRENT (@15V)	0.00	3.92	4.00	4.48	4.34	4.02	4.23	4.12	4.19	4.06	4.77	5.50	MA
IIH-LOGIC INPUT	0.00	1.48	1.13	1.56	1.53	1.16	1.13	1.10	970.M	1.40	1.79	10.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	1.63	1.22	1.92	1.58	1.32	1.10	1.09	560.M	1.37	1.66	10.0	UA
IIL-LOGIC INPUT	-1.00K	-1.05	-1.40	-1.25	-800.M	-1.05	-1.65	-900.M	-850.M	-650.M	-750.M	1.00K	NA
IIL-LOGIC REFERENCE INPUT	-1.00K	-150.M	-150.M	-850.M	-750.M	-300.M	-450.M	-700.M	-600.M	-1.00	-900.M	1.00K	NA
OUTPUT SHORT CIRCUIT (+)	-20.0	-13.0	-12.8	-13.8	-13.3	-13.0	-14.4	-12.7	-11.9	-13.3	-15.8	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	12.2	11.9	13.3	12.3	12.4	11.4	11.9	12.3	11.9	13.7	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	-100.	-42.5	-41.8	-29.0	-37.5	-50.5	-36.7	-36.7	-14.8	-38.1	-39.0	100.	PA
HOLD CAPACITOR LEAKAGE(-)	-100.	-8.50	-21.0	30.4	-21.2	-24.5	-9.00	-17.0	7.00	-17.0	-19.0	100.	PA
HOLD CAP CHRG CURRENT(+)	-100.	-9.22	-9.50	-9.97	-9.72	-9.48	-9.87	-9.34	-9.04	-9.72	-10.2	-3.00	MA
HOLD CAP CHRG CURRENT(-)	3.00	6.82	6.94	7.30	7.17	6.92	7.15	6.88	6.68	7.15	7.70	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	1.28	1.27	1.26	1.26	1.28	1.25	1.26	1.29	1.27	1.27	2.00	V
TAG (VIN-0V TO 10V STEP)	0.00	16.8	13.6	12.3	12.3	12.3	13.7	13.9	13.5	12.0	11.4	85.0	USEC
TAG (VIN-0V TO -10V STEP)	0.00	16.9	15.9	12.4	12.7	16.6	15.6	15.2	14.0	15.1	15.1	85.0	USEC
TAG (VIN=-10V TO 0V STEP)	0.00	16.6	12.1	12.3	12.3	12.4	12.8	14.2	13.6	12.2	11.4	85.0	USEC
TAG (VIN-10V TO 0V STEP)	0.00	16.1	15.0	11.9	12.2	15.4	15.0	14.5	13.5	14.7	13.7	85.0	USEC
TAP (VIN-0V TO 10V STEP)	0.00	115.	125.	135.	140.	115.	155.	135.	100.	145.	120.	800.	NSEC
TAP (VIN-0V TO -10V STEP)	0.00	170.	200.	200.	285. *	190.	225. *	210. *	200. *	210. *	190.	800.	NSEC
TAP (VIN=-10V TO 0V STEP)	0.00	105.	120.	125.	130.	110.	150.	130.	150.	135.	105.	800.	NSEC
TAP (VIN-10V TO 0V STEP)	0.00	185.	220. *	220. *	845. *	805. *	845. *	885. *	340. *	885. *	210. *	800.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-16. Mfr. Code B Devices at 25°C.

MANUFACTURER CODE: C ; DEVICE TYPE: LF198; DATE CODE:7909 25 SEP 80 11:28:32

+25 DEG C

PARAMETER	LO-LIM	S/N78	S/N79	S/N81	S/N82	S/N83	S/N85	S/N86	S/N87	S/N88	S/N89	HI-LIM	
VIO(+CM) AT 3.5V,-38.5V	-3.00	17.5M	660.M	-974.M	-208.M	764.M	-432.M	41.4M	373.M	-777.M	141.M	3.00	MV
VIO(-CM) AT 38.5V,-3.5V	-3.00	665.M	1.43	-31.4M	659.M	1.68	535.M	929.M	1.27	188.M	1.12	3.00	MV
VIO(@CM) AT 15.0V,-15.0V	-3.00	188.M	968.M	-565.M	149.M	1.18	50.9M	459.M	737.M	-345.M	629.M	3.00	MV
VIO(-CM) AT 7.0V,-3.0V	-3.00	266.M	1.06	-546.M	165.M	1.20	38.4M	420.M	760.M	-379.M	576.M	3.00	MV
VIO(+CM) AT 3.0V,-7.0V	-3.00	-6.55M	814.M	-919.M	-806.M	815.M	-340.M	41.7M	393.M	-805.M	148.M	3.00	MV
DELTA VIO/DELTA T (@CM)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	UV/DEG C
IIB(+CM) AT 3.5V,-38.5V	-1.00	3.57	2.36	3.62	3.03	2.89	8.32	9.33	3.10	9.58	7.09	25.0	NA
IIB(-CM) AT 38.5V,-3.5V	-1.00	3.50	2.70	3.51	2.88	2.84	8.49	8.95	3.00	9.04	5.31	25.0	NA
IIB(@CM) AT 15.0V,-15.0V	-1.00	3.49	2.95	3.76	3.02	3.08	8.86	9.14	3.10	9.23	6.98	25.0	NA
IIB(-CM) AT 7.0V,-3.0V	-1.00	3.45	3.18	3.86	2.91	3.08	8.94	9.19	3.19	9.43	7.31	25.0	NA
IIB(@CM) AT 3.0V,-7.0V	-1.00	3.48	3.47	3.98	2.85	3.11	9.21	9.50	3.19	9.58	7.57	25.0	NA
INPUT IMPEDANCE (ZI)	2.00	313.	67.6	213.	155.	450.	136.	61.1	229.	42.8	12.9	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	175.M	195.M	100.M	100.M	125.M	150.M	175.M	100.M	150.M	175.M	2.00	OHMS
RDC-SERIES CMG RESISTANCE	100.	267.	261.	282.	288.	287.	274.	275.	293.	268.	269.	400.	OHMS
GAIN ERROR (+/-11.5V CM)	-5.00M	-2.94M	-3.21M	-4.37M	-3.80M	-3.89M	-4.13M	-4.04M	-3.80M	-4.50M	-4.89M	5.00M	%
GAIN ERROR (+/-2.0V CM)	-20.0M	-6.25M	-6.99M	-11.0M	-9.00M	-10.1M	-10.2M	-11.5M	-10.4M	-11.7M	-12.0M	20.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	12.7	13.8	11.8	12.4	13.6	13.0	13.5	13.0	12.4	13.5	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-18.7	-17.8	-20.7	-19.2	-18.9	-21.4	-21.3	-18.8	-21.8	-20.7	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	108.	106.	96.5	99.8	98.9	99.3	98.7	98.9	95.6	96.6	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	121.	128.	122.	122.	116.	112.	117.	113.	122.	126.	200.	dB
FEEDTHRU REJ 0V TO 11.5V	86.0	87.4	91.6	91.1	96.3	89.2	87.8	88.9	98.4	92.7	83.1 *	200.	dB
FEEDTHRU REJ 11.5V TO 0V	86.0	91.5	87.7	88.5	90.9	95.2	95.9	91.1	91.6	88.2	83.2 *	200.	dB
FEEDTHRU REJ 0V TO -11.5V	86.0	93.5	89.3	93.1	93.3	93.8	92.0	94.1	93.8	96.7	96.2	200.	dB
FEEDTHRU REJ -11.5V TO 0V	86.0	89.7	93.0	93.1	90.9	92.0	91.9	92.6	92.1	90.3	89.6	200.	dB
HOLD STEP VOLTAGE (VHS+)	-2.00	-1.27	-1.67	-1.15	-1.33	-1.28	-745.M	-660.M	-1.33	-810.M	-584.M	2.00	MV
HOLD STEP VOLTAGE (VHS-)	-2.00	-2.14 *	-2.67 *	-2.09 *	-2.14 *	-2.05 *	-1.58	-1.42	-2.15 *	-1.66	-451.M	2.00	MV
ICC-SUPPLY CURRENT (@15V)	0.00	3.77	4.05	5.21	5.23	5.12	5.39	5.18	5.09	5.48	5.32	5.50	MA
IIH-LOGIC INPUT	0.00	840.M	915.M	1.22	800.M	865.M	1.64	1.62	795.M	1.66	1.42	10.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	490.M	530.M	990.M	455.M	450.M	1.04	955.M	435.M	900.M	740.M	10.0	UA
IIL-LOGIC INPUT	-1.00K	-1.10	-750.M	-850.M	-1.05	-1.35	-1.20	-1.25	-800.M	-850.M	-1.20	1.00K	MA
IIL-LOGIC REFERENCE INPUT	-1.00K	-150.M	-200.M	-1.00	-700.M	-300.M	-50.0M	-100.M	-1.00	-600.M	-650.M	1.00K	MA
OUTPUT SHORT CIRCUIT (+)	-20.0	-15.8	-15.2	-20.4 *	-20.0	-19.9	-21.5 *	-21.3 *	-19.6	-22.1 *	-21.3 *	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	12.1	12.1	17.1	17.3	17.0	18.1	18.1	17.0	18.1	18.3	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	-100.	-7.50	-10.0	-4.00	-500.M	7.50	-8.00	-6.00	-1.50	-5.50	-4.00	100.	PA
HOLD CAPACITOR LEAKAGE(-)	-100.	-27.0	-8.50	8.00	9.00	10.5	-500.M	1.00	7.00	500.M	2.50	100.	PA
HOLD CAP CHRG CURRENT(+)	-100.	-6.97	-6.93	-6.32	-6.16	-6.18	-6.48	-6.42	-6.11	-6.64	-6.52	-3.00	MA
HOLD CAP CHRG CURRENT(-)	3.00	4.56	4.63	4.56	4.70	4.48	4.27	4.13	4.57	4.38	4.14	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	1.30	1.29	1.27	1.27	1.27	1.29	1.30	1.27	1.29	1.30	2.00	V
TAQ (VIN-0V TO 10V STEP)	0.00	21.0	19.2	21.8	22.5	21.9	21.0	21.9	24.7	22.0	20.6	25.0	USEC
TAQ (VIN-0V TO -10V STEP)	0.00	22.1	19.0	22.0	22.7	22.6	21.0	20.7	23.2	20.7	20.5	25.0	USEC
TAQ (VIN=-10V TO 0V STEP)	0.00	19.2	19.3	21.1	22.2	22.1	20.6	20.7	22.4	20.2	19.9	25.0	USEC
TAQ (VIN-10V TO 0V STEP)	0.00	18.4	18.7	21.9	22.6	22.4	20.7	20.5	22.9	20.3	20.4	25.0	USEC
TAP (VIN-0V TO 10V STEP)	0.00	115.	140.	125.	120.	120.	110.	105.	120.	110.	90.0	200.	NSEC
TAP (VIN-0V TO -10V STEP)	0.00	190.	215. *	190.	185.	175.	130.	125.	185.	135.	110.	200.	NSEC
TAP (VIN=-10V TO 0V STEP)	0.00	120.	155.	125.	125.	125.	110.	100.	125.	110.	90.0	200.	NSEC
TAP (VIN-10V TO 0V STEP)	0.00	190.	215. *	185.	175.	175.	130.	120.	185.	135.	110.	200.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-17. Mfr. Code C Devices at 25°C.

MANUFACTURER CODE: A ; DEVICE TYPE: LF198; DATE CODE:7909 25 SEP 80 11:41:32

PARAMETER	LO-LIM	S/N 6	S/N 9	S/N19	S/N23	+125 DEG C S/N28	S/N34	S/N35	S/N41	S/N45	S/N48	HI-LIM	
VIO(+CM) AT 3.5V,-86.5V	-5.00	-1.96	-520.M	-127.M	374.M	-1.49	-885.M	-767.M	-811.M	-10.3M	-1.16	5.00	MV
VIO(-CM) AT 86.5V,-3.5V	-5.00	-1.58	-99.1M	361.M	836.M	-999.M	-477.M	-111.M	-149.M	427.M	-591.M	5.00	MV
VIO(@CM) AT 15.0V,-15.0V	-5.00	-1.74	-182.M	178.M	756.M	-1.16	-494.M	-356.M	-517.M	221.M	-653.M	5.00	MV
VIO(-CM) AT 7.0V,-3.0V	-5.00	-1.88	-281.M	116.M	403.M	-1.18	-681.M	-480.M	-508.M	267.M	-803.M	5.00	MV
VIO(+CM) AT 3.0V,-7.0V	-5.00	-2.20	-603.M	-281.M	-10.1M	-1.55	-1.01	-889.M	-1.06	-141.M	-1.26	5.00	MV
DELTA VIO/DELTA T (@CM)	-20.0	4.88	4.88	3.92	-3.86	3.57	2.06	1.46	-741.M	5.31	4.70	20.0	UV/DEG C
IIB(+CM) AT 3.5V,-86.5V	-75.0	-1.35	-800.M	-2.34	-1.96	-1.77	4.97	-1.47	-1.51	-2.03	1.00M	75.0	NA
IIB(-CM) AT 86.5V,-3.5V	-75.0	-7.66	-7.50	-11.0	-18.1	-7.96	-2.79	-7.94	-8.37	-9.17	-8.67	75.0	NA
IIB(@CM) AT 15.0V,-15.0V	-75.0	-4.96	-4.61	-7.48	-9.54	-5.30	681.M	-5.50	-5.64	-6.26	-4.89	75.0	NA
IIB(-CM) AT 7.0V,-3.0V	-75.0	-2.54	-1.94	-3.77	-3.97	-2.68	3.97	-2.94	-3.01	-3.49	-1.42	75.0	NA
IIB(@CM) AT 3.0V,-7.0V	-75.0	-1.10	-366.M	-1.90	-1.32	-1.28	6.03	-1.39	-1.55	-1.84	547.M	75.0	NA
INPUT IMPEDANCE (ZI)	1.00	3.65	3.43	2.67	1.42	3.71	2.96	3.56	3.35	3.22	2.65	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	25.0M	350.M	-50.0M	580.M	200.M	573.M	200.M	450.M	325.M	543.M	4.00	OHMS
RSC-SERIES CMG RESISTANCE	100.	392.	396.	356.	479.	372.	367.	360.	339.	370.	452.	600.	OHMS
GAIN ERROR (+/-11.5V CM)	-20.0M	-4.20M	-4.42M	-5.57M	-8.69M	-4.67M	-5.00M	-5.37M	-5.40M	-4.57M	-5.94M	20.0M	%
GAIN ERROR (+/-2.0V CM)	-40.0M	-11.8M	-13.1M	-13.9M	-16.3M	-12.5M	-12.9M	-13.9M	-18.3M	-13.8M	-17.6M	40.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	19.4	20.8	21.8	22.2	19.1	22.6	19.6	21.4	21.4	20.7	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-9.07	-8.31	-7.13	-5.97 x	-7.66	-9.38	-6.09	-5.87 x	-7.16	-7.35	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	94.7	104.	99.5	93.8	108.	98.7	93.3	94.7	102.	101.	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	98.7	116.	110.	96.1	112.	104.	102.	105.	117.	108.	200.	dB
FEEDTHRU REJ 0V TO 11.5V	80.0	97.9	91.4	95.9	89.3	92.9	86.8	93.4	88.1	92.0	93.4	200.	dB
FEEDTHRU REJ 11.5V TO 0V	80.0	89.0	87.0	94.5	93.2	87.6	93.8	95.5	89.1	92.1	87.0	200.	dB
FEEDTHRU REJ 0V TO -11.5V	80.0	88.2	87.2	90.6	88.0	87.1	82.4	87.1	84.4	88.3	88.5	200.	dB
FEEDTHRU REJ -11.5V TO 0V	80.0	94.2	95.6	92.0	97.4	96.9	95.9	95.6	93.8	90.6	95.0	200.	dB
HOLD STEP VOLTAGE (VHS+)	-5.00	-725.M	-675.M	-555.M	-666.M	-1.22	90.4M	-1.06	-800.M	-1.25	-685.M	5.00	MV
HOLD STEP VOLTAGE (VHS-)	-5.00	-1.34	-1.61	-2.33	-2.14	-2.06	-1.74	-2.04	-2.05	-1.95	-2.27	5.00	MV
ICC-SUPPLY CURRENT (@15V)	0.00	3.79	3.99	4.80	3.82	4.05	4.48	3.95	4.60	4.10	4.34	5.00	MA
IIH-LOGIC INPUT	0.00	645.M	805.M	905.M	710.M	675.M	1.79	730.M	780.M	635.M	895.M	20.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	415.M	415.M	425.M	410.M	325.M	880.M	330.M	360.M	290.M	480.M	20.0	UA
IIL-LOGIC INPUT	-3.00K	-950.M	-1.05	-1.20	-1.45	-1.20	300.M	-1.00	-1.35	-2.00	-1.05	3.00K	MA
IIL-LOGIC REFERENCE INPUT	-3.00K	-3.85	-3.55	-4.60	-2.95	-3.50	-4.25	-3.90	-3.75	-3.05	-3.45	3.00K	MA
OUTPUT SHORT CIRCUIT (+)	-20.0	-6.20	-6.15	-7.55	-5.45	-6.25	-7.00	-6.30	-7.25	-6.65	-6.15	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	8.85	9.65	10.6	8.45	9.35	11.2	9.45	10.0	9.40	7.80	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	-100.K	-12.3K	-13.8K	-12.7K	-13.7K	-13.7K	-13.8K	-10.3K	-13.7K	-13.8K	-13.6K	100.K	PA
HOLD CAPACITOR LEAKAGE(-)	-100.K	13.8K	4.88K	13.7K	1.85K	10.3K	-3.99K	13.6K	13.7K	11.4K	588.	100.K	PA
HOLD CAP CHRG CURRENT(+)	-100.	-4.02	-4.01	-4.42	-3.33	-4.36	-4.36	-4.45	-4.82	-4.33	-3.56	-2.00	MA
HOLD CAP CHRG CURRENT(-)	2.00	3.80	3.83	4.21	3.15	7.05	4.17	7.18	7.58	6.99	3.40	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	840.M	830.M	840.M	840.M	850.M	900.M	850.M	850.M	830.M	850.M	2.00	V
TRD (VIN=0V TO 10V STEP)	0.00	29.8	27.7	25.7	34.3	26.0	25.7	24.4	23.7	25.5	33.1	50.0	USEC
TRD (VIN=0V TO -10V STEP)	0.00	50.0	49.3	50.0	50.0	50.0	50.0	50.0	24.7	26.7	47.4	50.0	USEC
TRD (VIN=-10V TO 0V STEP)	0.00	34.2	27.1	25.7	35.7	50.0	25.2	25.3	22.8	25.3	30.7	50.0	USEC
TRD (VIN=10V TO 0V STEP)	0.00	26.8	27.2	24.9	34.4	30.9	24.6	28.1	23.6	25.5	31.3	50.0	USEC
TRP (VIN=0V TO 10V STEP)	0.00	250.	190.	210.	220.	245.	185.	240.	200.	205.	230.	400.	NSEC
TRP (VIN=0V TO -10V STEP)	0.00	170.	185.	155.	180.	185.	130.	180.	185.	170.	185.	400.	NSEC
TRP (VIN=-10V TO 0V STEP)	0.00	500. x	190.	500. x	210.	500. x	170.	500. x	275.	205.	220.	400.	NSEC
TRP (VIN=10V TO 0V STEP)	0.00	185.	135.	160.	185.	195.	140.	190.	200.	180.	185.	400.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-18. Mfr. Code A Devices at 125°C.

MANUFACTURER CODE: 8 ; DEVICE TYPE: LF198; DATE CODE:7909 25 SEP 80 11:43:32

+125 DEG C

PARAMETER	LO-LIM	S/N61	S/N62	S/N63	S/N64	S/N56	S/N57	S/N58	S/N59	S/N60	S/N61	HI-LIM	
VIO(+CM) AT 3.5V,-26.5V	-5.00	-1.42	300.M	1.50	740.M	-78.6M	975.M	384.M	-80.7M	-130.M	-255.M	5.00	MV
VIO(-CM) AT 26.5V,-3.5V	-5.00	-1.05	716.M	1.83	1.24	333.M	1.57	901.M	327.M	258.M	112.M	5.00	MV
VIO(0CM) AT 15.0V,-15.0V	-5.00	-1.19	630.M	1.80	1.13	203.M	1.39	771.M	239.M	175.M	-5.7SM	5.00	MV
VIO(-CM) AT 7.0V,-3.0V	-5.00	-1.02	738.M	1.84	1.20	302.M	1.40	826.M	368.M	238.M	174.M	5.00	MV
VIO(+CM) AT 3.0V,-7.0V	-5.00	-1.24	502.M	1.61	905.M	61.6M	1.11	541.M	105.M	3.60M	-73.9M	5.00	MV
DELTA VIO/DELTA T (0CM)	-20.0	9.50	4.58	2.42	2.31	733.M	257.M	1.24	8.36	3.91	-700.M	20.0	UV/DEG C
IIB(+CM) AT 3.5V,-26.5V	-75.0	2.71	334.M	28.4M	1.02	404.M	227.M	-192.M	5.00M	1.32	3.35	75.0	NA
IIB(-CM) AT 26.5V,-3.5V	-75.0	-14.8	-3.80	-20.5	-3.83	-7.71	-14.6	-5.87	-2.54	-3.89	-1.20	75.0	NA
IIB(0CM) AT 15.0V,-15.0V	-75.0	-8.00	-2.03	-14.8	-1.65	-4.23	-8.28	-3.18	-1.66	-1.90	311.M	75.0	NA
IIB(-CM) AT 7.0V,-3.0V	-75.0	632.M	-184.M	-2.93	758.M	-879.M	-1.48	-756.M	-110.M	502.M	2.41	75.0	NA
IIB(0CM) AT 3.0V,-7.0V	-75.0	3.19	881.M	604.M	1.67	433.M	612.M	317.M	621.M	1.78	3.54	75.0	NA
INPUT IMPEDANCE (ZI)	1.00	1.31	5.56	1.12	4.74	2.83	1.55	4.05	9.03	4.42	5.06	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	200.M	233.M	177.M	241.M	200.M	175.M	150.M	197.M	232.M	175.M	4.00	OHMS
RSC-SERIES CMG RESISTANCE	100.	202.	209.	204.	213.	208.	209.	231.	224.	205.	192.	600.	OHMS
GAIN ERROR (+/-11.5V CM)	-20.0M	-8.88M	-3.42M	-9.15M	-4.05M	-5.20M	-8.77M	-4.72M	-2.76M	-3.93M	-3.44M	20.0M	%
GAIN ERROR (+/-2.0V CM)	-40.0M	-13.0M	-8.70M	-13.9M	-9.80M	-9.28M	-11.7M	-9.99M	-8.51M	-7.13M	-8.63M	40.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	16.1	17.9	19.7	18.8	17.5	18.5	17.9	17.1	17.7	17.3	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-20.9	-17.9	-16.4	-17.1	-18.0	-16.8	-17.9	-16.9	-19.5	-19.3	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	110.	117.	102.	110.	124.	105.	106.	116.	120.	110.	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	104.	106.	102.	107.	103.	104.	107.	107.	109.	104.	200.	dB
FEEDTHRU REJ 0V TO 11.5V	80.0	89.5	93.6	89.3	89.1	87.9	90.1	89.5	89.0	93.8	88.1	200.	dB
FEEDTHRU REJ 11.5V TO 0V	80.0	89.9	93.2	92.2	91.6	94.0	97.3	88.8	89.2	97.6	95.6	200.	dB
FEEDTHRU REJ 0V TO -11.5V	80.0	94.4	93.8	96.3	91.9	93.9	93.8	93.1	92.3	92.9	95.8	200.	dB
FEEDTHRU REJ -11.5V TO 0V	80.0	89.4	91.1	88.5	87.5	91.5	94.0	91.8	88.6	90.2	88.4	200.	dB
HOLD STEP VOLTAGE (VHS+)	-5.00	-9.60M	-358.M	390.M	434.M	-150.M	-89.1M	-72.1M	-230.M	-89.6M	-170.M	5.00	MV
HOLD STEP VOLTAGE (VHS-)	-5.00	-1.75	-1.87	-1.64	-1.72	-1.34	-2.14	-1.80	-2.06	-1.90	-2.69	5.00	MV
ICC-SUPPLY CURRENT (@15V)	0.00	3.49	3.47	3.92	3.72	3.47	3.60	3.52	3.59	3.51	4.23	5.00	MA
IIH-LOGIC INPUT	0.00	885.M	670.M	930.M	895.M	685.M	650.M	650.M	575.M	830.M	1.05	20.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	955.M	710.M	1.09	935.M	765.M	620.M	630.M	330.M	810.M	965.M	20.0	UA
IIL-LOGIC INPUT	-3.00K	400.M	2.25	-250.M	2.95	950.M	400.M	900.M	300.M	2.05	2.35	3.00K	NA
IIL-LOGIC REFERENCE INPUT	-3.00K	-3.25	-1.25	-6.10	-2.05	-1.65	-2.45	-1.50	-1.20	-1.80	-2.10	3.00K	NA
OUTPUT SHORT CIRCUIT (+)	-20.0	-8.15	-7.90	-8.65	-8.25	-8.00	-8.95	-7.90	-7.35	-8.15	-9.90	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	7.90	8.10	8.50	8.20	8.20	7.70	7.65	7.70	8.15	8.90	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	-100.K	-7.78K	-8.85K	-13.1K	-13.1K	-6.60K	-12.9K	-13.9K	-12.3K	-8.69K	-12.3K	100.K	PA
HOLD CAPACITOR LEAKAGE(-)	-100.K	1.41K	-4.14K	-199.	-6.90K	-1.22K	-5.03K	-9.07K	-6.66K	-4.06K	-2.71K	100.K	PA
HOLD CAP CHRG CURRENT(+)	-100.	-7.21	-7.20	-7.68	-7.37	-7.16	-7.41	-7.10	-6.90	-7.41	-7.96	-2.00	MA
HOLD CAP CHRG CURRENT(-)	2.00	5.76	5.72	6.12	5.91	5.70	5.82	5.56	5.56	5.90	6.38	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	860.M	840.M	840.M	830.M	850.M	820.M	840.M	820.M	850.M	840.M	2.00	V
TAQ (VIN=0V TO 10V STEP)	0.00	18.9	17.3	14.2	14.4	17.5	17.5	16.2	15.6	16.8	15.6	50.0	USEC
TAQ (VIN=0V TO -10V STEP)	0.00	20.9	20.0	17.7	18.2	20.4	20.1	17.0	19.2	19.5	17.8	50.0	USEC
TAQ (VIN=-10V TO 0V STEP)	0.00	18.8	17.1	14.0	14.3	17.2	17.0	16.3	15.5	16.5	15.2	50.0	USEC
TAQ (VIN=10V TO 0V STEP)	0.00	20.5	19.1	16.5	17.6	18.9	19.0	16.2	19.1	19.6	17.2	50.0	USEC
TAP (VIN=0V TO 10V STEP)	0.00	210.	230.	245.	245.	205.	275.	240.	285.	255.	235.	400.	NSEC
TAP (VIN=0V TO -10V STEP)	0.00	325.	340.	335.	365.	320.	370.	350.	480. #	360.	340.	400.	NSEC
TAP (VIN=-10V TO 0V STEP)	0.00	210.	225.	235.	240.	200.	265.	230.	280.	245.	235.	400.	NSEC
TAP (VIN=10V TO 0V STEP)	0.00	345.	365.	365.	395.	345.	405. #	375.	490. #	375.	370.	400.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-19. Mfr. Code B Devices at 125°C.

MANUFACTURER CODE: C ; DEVICE TYPE: LF198; DATE CODE:7909 25 SEP 80 11:45:46

PARAMETER	LO-LIM	S/N78	S/N79	S/N81	S/N82	+125 DEG C S/N83	S/N85	S/N86	S/N87	S/N88	S/N89	HI-LIM	
VIO(+CM) AT 3.5V,-26.5V	-5.00	-935.M	-159.M	-1.94	-1.21	8.25M	-1.21	-1.05	-591.M	-1.91	-1.27	5.00	MV
VIO(-CM) AT 26.5V,-3.5V	-5.00	-93.1M	556.M	-848.M	-162.M	989.M	-287.M	-154.M	448.M	-903.M	245.M	5.00	MV
VIO(0CM) AT 15.0V,-15.0V	-5.00	-534.M	105.M	-1.38	-683.M	496.M	-768.M	-605.M	-90.6M	-1.39	-401.M	5.00	MV
VIO(-CM) AT 7.0V,-3.0V	-5.00	-440.M	221.M	-1.41	-684.M	528.M	-755.M	-612.M	-74.7M	-1.37	-542.M	5.00	MV
VIO(+CM) AT 3.0V,-7.0V	-5.00	-742.M	-21.1M	-1.76	-1.04	161.M	-1.08	-927.M	-421.M	-1.73	-1.09	5.00	MV
DELTA VIO/DELTA T (0CM)	-20.0	7.22	8.62	8.27	8.32	6.83	8.19	10.6	8.28	10.5	10.3	20.0	UV/DEG C
IIB(+CM) AT 3.5V,-26.5V	-75.0	-548.M	-855.M	-3.48	-3.29	-2.21	-37.0M	1.25	-2.57	-1.24	-2.22	75.0	NA
IIB(-CM) AT 26.5V,-3.5V	-75.0	-4.99	-6.03	-11.2	-11.3	-9.37	-9.07	-5.12	-9.80	-11.6	-21.6	75.0	NA
IIB(0CM) AT 15.0V,-15.0V	-75.0	-2.98	-3.39	-6.64	-6.51	-5.36	-3.[illegible]	-1.29	-5.62	-5.45	-10.3	75.0	NA
IIB(-CM) AT 7.0V,-3.0V	-75.0	-1.31	-1.82	-4.22	-4.12	-3.28	[illegible].36	504.M	-3.54	-2.46	-4.72	75.0	NA
IIB(0CM) AT 3.0V,-7.0V	-75.0	-308.M	-824.M	-2.75	-2.76	-2.08	264.M	1.85	-2.20	-531.M	-649.M	75.0	NA
INPUT IMPEDANCE (ZI)	1.00	5.18	4.45	2.98	2.86	3.21	2.55	3.61	3.18	2.22	1.19	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	250.M	250.M	125.M	125.M	100.M	175.M	150.M	100.M	125.M	150.M	4.00	OHMS
RSC-SERIES CHG RESISTANCE	100.	328.	311.	348.	359.	356.	340.	345.	364.	339.	340.	600.	OHMS
GAIN ERROR (+/-11.5V CM)	-20.0M	-5.43M	-4.94M	-7.20M	-7.21M	-6.64M	-7.10M	-5.99M	-6.81M	-8.04M	-15.7M	20.0M	%
GAIN ERROR (+/-2.0V CM)	-40.0M	-10.5M	-8.74M	-11.9M	-12.1M	-12.4M	-13.4M	-12.0M	-12.2M	-14.0M	-22.3M	40.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	14.7	15.1	13.3	13.8	15.1	14.4	14.7	14.4	13.7	14.7	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-23.0	-22.1	-25.1	-23.6	-23.0	-25.7	-25.6	-23.2	-26.2	-25.1	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	97.5	97.0	92.0	93.6	94.9	102.	95.6	94.0	94.3	89.8	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	200.	108.	122.	116.	126.	106.	200.	105.	122.	110.	200.	dB
FEEDTHRU REJ 0V TO 11.5V	80.0	88.2	83.9	89.9	87.2	91.3	90.3	90.5	86.3	95.9	85.7	200.	dB
FEEDTHRU REJ 11.5V TO 0V	80.0	87.1	88.8	95.3	88.1	88.5	88.2	87.4	94.7	91.3	88.5	200.	dB
FEEDTHRU REJ 0V TO -11.5V	80.0	89.0	88.9	93.5	93.9	92.7	93.1	92.8	92.0	93.3	96.7	200.	dB
FEEDTHRU REJ -11.5V TO 0V	80.0	90.1	89.1	91.0	90.8	91.9	93.4	92.9	91.3	92.8	90.1	200.	dB
HOLD STEP VOLTAGE (VHS+)	-5.00	-2.61	-3.07	-2.42	-2.44	-2.38	-2.09	-1.90	-2.50	-2.21	-2.17	5.00	MV
HOLD STEP VOLTAGE (VHS-)	-5.00	-3.47	-4.56	-3.68	-3.52	-3.52	-3.32	-3.01	-3.61	-3.48	-1.66	5.00	MV
ICC-SUPPLY CURRENT (@15V)	0.00	3.31	3.62	4.87	4.87	4.81	5.04 #	4.89	4.74	5.10 #	5.03 #	5.00	MA
IIH-LOGIC INPUT	0.00	485.M	555.M	800.M	500.M	545.M	1.03	1.02	500.M	1.03	895.M	20.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	290.M	325.M	675.M	285.M	285.M	700.M	615.M	275.M	570.M	470.M	20.0	UA
IIL-LOGIC INPUT	-3.00K	-1.05	-1.85	-1.20	-1.25	-1.20	-900.M	-800.M	-2.00	-1.25	-1.30	3.00K	MA
IIL-LOGIC REFERENCE INPUT	-3.00K	-3.40	-5.00	-9.15	-8.80	-6.85	-9.80	-6.60	-7.65	-10.9	-6.90	3.00K	MA
OUTPUT SHORT CIRCUIT (+)	-20.0	-9.55	-9.60	-12.8	-12.5	-12.7	-13.8	-13.5	-12.3	-13.9	-13.5	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	9.55	9.85	12.2	12.0	12.1	13.3	13.2	11.9	13.3	13.1	80.0	MA
HOLD CAPACITOR LEAKAGE(+)	-100.K	-13.4K	-13.5K	-13.4K	-13.5K	-13.6K	-13.5K	-13.6K	-13.6K	-13.4K	-13.4K	100.K	PA
HOLD CAPACITOR LEAKAGE(-)	-100.K	-13.6K	-13.5K	5.15K	6.63K	5.33K	-1.92K	-2.74K	3.74K	-4.01K	13.1K	100.K	PA
HOLD CAP CHRG CURRENT(+)	-100.	-5.29	-5.39	-4.88	-4.77	-4.82	-5.03	-4.98	-4.74	-6.11	-5.02	-2.00	MA
HOLD CAP CHRG CURRENT(-)	2.00	4.07	4.11	4.11	4.12	4.08	3.93	4.00	4.11	3.94	3.83	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	880.M	870.M	850.M	850.M	860.M	880.M	900.M	850.M	880.M	890.M	2.00	V
TAQ (VIN=0V TO 10V STEP)	0.00	22.1	22.2	27.8	33.2	25.6	33.5	28.2	27.8	33.0	38.7	60.0	USEC
TAQ (VIN=0V TO -10V STEP)	0.00	33.4	25.7	33.4	26.3	25.5	27.6	25.2	26.2	30.6	28.8	60.0	USEC
TAQ (VIN=-10V TO 0V STEP)	0.00	21.7	22.0	24.7	25.1	24.7	23.6	23.4	25.6	24.4	23.2	60.0	USEC
TAQ (VIN=10V TO 0V STEP)	0.00	25.4	49.9	49.9	25.8	25.2	28.4	24.9	25.9	49.9	28.8	60.0	USEC
TAP (VIN=0V TO 10V STEP)	0.00	210.	255.	235.	220.	225.	225.	220.	225.	225.	190.	400.	NSEC
TAP (VIN=0V TO -10V STEP)	0.00	320.	365.	305.	305.	305.	270.	250.	305.	270.	230.	400.	NSEC
TAP (VIN=-10V TO 0V STEP)	0.00	215.	270.	230.	230.	230.	220.	230.	230.	215.	195.	400.	NSEC
TAP (VIN=10V TO 0V STEP)	0.00	335.	370.	325.	320.	315.	290.	270.	320.	285.	285.	400.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-20. Mfr. Code C Devices at 125°C.

MANUFACTURER CODE: A ; DEVICE TYPE: LF198; DATE CODE:7909 25 SEP 80 11:38:19

-55 DEG C

PARAMETER	LO-LIM	S/N 6	S/N 9	S/N19	S/N23	S/N28	S/N34	S/N35	S/N41	S/N45	S/N48	HI-LIM	
VIO(+CM) AT 3.5V,-26.5V	-5.00	-2.00	131.M	23.3M	-268.M	-826.M	-834.M	-137.M	-957.M	1.31	213.M	5.00	MV
VIO(-CM) AT 26.5V,-3.5V	-5.00	-1.41	679.M	674.M	472.M	-116.M	-27.1M	685.M	2.94	1.64	1.02	5.00	MV
VIO(DCM) AT 15.0V,-15.0V	-5.00	-1.60	468.M	479.M	274.M	-405.M	-307.M	369.M	-592.M	1.48	-142. *	5.00	MV
VIO(-CM) AT 7.0V,-3.0V	-5.00	-1.71	363.M	384.M	82.3M	-384.M	-452.M	232.M	16.0 *	6.85 *	531.M	5.00	MV
VIO(+CM) AT 3.0V,-7.0V	-5.00	-2.31	-132.M	-229.M	-632.M	-933.M	-987.M	-376.M	-1.19	1.03	-228.M	5.00	MV
DELTA VIO/DELTA T (DCM)	-20.0	4.31	-2.02	1.13	1.21	-4.92	232.M	-7.24	11.9M	-9.10	1.77K*	20.0	UV/DEG C
IIB(+CM) AT 3.5V,-26.5V	-75.0	13.9	18.7	15.4	14.8	20.5	45.0	21.5	20.2	14.8	22.8	75.0	NA
IIB(-CM) AT 26.5V,-3.5V	-75.0	13.4	18.1	14.8	14.2	19.6	43.2	20.4	17.9	14.2	21.9	75.0	NA
IIB(DCM) AT 15.0V,-15.0V	-75.0	13.6	18.2	15.0	14.2	19.4	43.9	20.6	18.9	14.4	-1.40K*	75.0	NA
IIB(-CM) AT 7.0V,-3.0V	-75.0	13.7	18.2	15.2	14.3	20.5	44.1	21.4	14.3	12.9	20.9	75.0	NA
IIB(DCM) AT 3.0V,-7.0V	-75.0	14.0	18.7	15.6	14.4	21.4	45.7	22.3	21.9	15.4	21.7	75.0	NA
INPUT IMPEDANCE (ZI)	1.00	44.7	33.4	41.0	35.6	25.7	12.3	20.8	9.92	34.5	25.9	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	75.0M	305.M	50.0M	300.M	167.M	-49.2	175.M	200.M	-150.M	300.M	4.00	OHMS
RSC-SERIES CMG RESISTANCE	100.	287.	285.	275.	345.	275.	277.	268.	256.	1.00K*	324.	600.	OHMS
GAIN ERROR (+/-11.5V CM)	-20.0M	-2.83M	-2.83M	-3.07M	-3.35M	-3.65M	-4.04M	-4.02M	-18.6M	-1.91M	-3.78M	20.0M	%
GAIN ERROR (+/-2.0V CM)	-40.0M	-16.9M	-13.5M	-16.3M	-19.6M	-16.0M	-17.3M	-15.4M	-451.M*	-150.M*	-22.1M	40.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	12.4	14.3	15.2	14.4	13.6	15.5	14.3	14.6	15.1	15.0	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-7.09	-5.37 *	-5.19 *	-4.46 *	-5.32 *	-7.20	-3.81 *	-3.26 *	-3.64 *	-4.00 *	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	96.5	98.9	97.2	97.3	102.	95.6	95.1	100.	108.	96.9	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	106.	132.	114.	132.	98.7	112.	142.	122.	105.	200.	200.	dB
FEEDTHRU REJ 0V TO 11.5V	80.0	98.1	89.3	91.6	91.3	92.6	89.1	89.4	89.4	114.	90.4	200.	dB
FEEDTHRU REJ 11.5V TO 0V	80.0	90.6	92.7	98.0	95.7	95.7	95.0	93.3	107.	97.1	96.7	200.	dB
FEEDTHRU REJ 0V TO -11.5V	80.0	93.5	96.6	94.5	94.4	93.1	92.3	96.3	53.4 *	95.8	95.5	200.	dB
FEEDTHRU REJ -11.5V TO 0V	80.0	92.0	88.5	94.1	91.7	53.7 *	45.3 *	53.6 *	95.2	59.5 *	92.4	200.	dB
HOLD STEP VOLTAGE (VHS+)	-5.00	235.M	322.M	50.4M	215.M	160.M	175.M	45.4M	590.M	230.M	216.M	5.00	MV
HOLD STEP VOLTAGE (VHS-)	-5.00	-9.60M	-60.6M	-459.M	-173.M	-275.M	-34.6M	-300.M	-110.M	-154.M	-184.M	5.00	MV
ICC-SUPPLY CURRENT (@15V)	0.00	4.66	4.68	5.20	4.30	5.11	4.74	4.68	5.75	4.67	4.94	6.50	MA
IIH-LOGIC INPUT	0.00	1.77	2.19	2.28	3.31	2.09	4.55	2.66	3.18	2.09	2.47	20.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	950.M	1.04	1.08	1.32	1.35	2.11	1.18	1.48	885.M	1.18	20.0	UA
IIL-LOGIC INPUT	-3.00K	-1.70	-1.65	-700.M	-900.M	-650.M	-1.05	-1.70	-800.M	-1.65	-1.65	3.00K	NA
IIL-LOGIC REFERENCE INPUT	-3.00K	-450.M	-350.M	-800.M	-350.M	-1.00	-450.M	-200.M	-1.15	-1.15	-200.M	3.00K	NA
OUTPUT SHORT CIRCUIT (+)	-20.0	-13.8	-13.8	-15.9	-12.4	-13.8	-14.5	-13.9	-16.1	-14.6	-13.7	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	15.8	17.5	18.8	14.2	13.1	18.2	15.6	16.5	16.1	11.9	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	0.00	2.00	-1.50	3.50	5.00	-1.50	-2.50	-1.50	11.5	8.85	-1.25	0.00	PA
HOLD CAPACITOR LEAKAGE(-)	0.00	0.00	-1.10	2.50	1.00	-7.00	-3.00	-4.70	5.50	-5.75	-600.M	0.00	PA
HOLD CAP CHRG CURRENT(+)	-100.	-6.83	-6.83	-6.97	-5.60	-7.14	-7.03	-7.32	-8.07	-8.10	-6.01	-2.00	MA
HOLD CAP CHRG CURRENT(-)	2.00	5.12	5.63	6.34	4.42	5.09	5.23	5.49	6.45	5.07	5.11	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	1.49	1.43	1.48	1.48	1.17	1.44	1.54	1.54	1.47	1.48	2.00	V
TAD (VIN=0V TO 10V STEP)	0.00	24.8	23.1	22.6	28.2	23.7	82.6	21.7	17.9	23.5	25.7	50.0	USEC
TAD (VIN=0V TO -10V STEP)	0.00	22.7	24.0	24.6	28.2	21.6	21.5	20.8	20.3	22.0	28.3	50.0	USEC
TAD (VIN=-10V TO 0V STEP)	0.00	22.7	22.7	22.4	27.5	22.6	23.5	20.9	29.7	38.3	25.9	50.0	USEC
TAD (VIN=10V TO 0V STEP)	0.00	22.5	22.3	21.2	28.1	21.5	21.9	20.4	20.0	21.6	25.7	50.0	USEC
TAP (VIN=0V TO 10V STEP)	0.00	60.0	45.0	45.0	45.0	60.0	35.0	60.0	70.0	55.0	50.0	400.	NSEC
TAP (VIN=0V TO -10V STEP)	0.00	25.0	15.0	25.0	25.0	30.0	495. *	35.0	45.0	310.	25.0	400.	NSEC
TAP (VIN=-10V TO 0V STEP)	0.00	60.0	40.0	45.0	45.0	55.0	35.0	60.0	65.0	495. *	45.0	400.	NSEC
TAP (VIN=10V TO 0V STEP)	0.00	30.0	15.0	25.0	30.0	35.0	15.0	40.0	40.0	30.0	30.0	400.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-21. Mfr. Code A Devices at -55°C.

MANUFACTURER CODE: B ; DEVICE TYPE: LF198; DATE CODE:7909 25 SEP 80 11:35:20

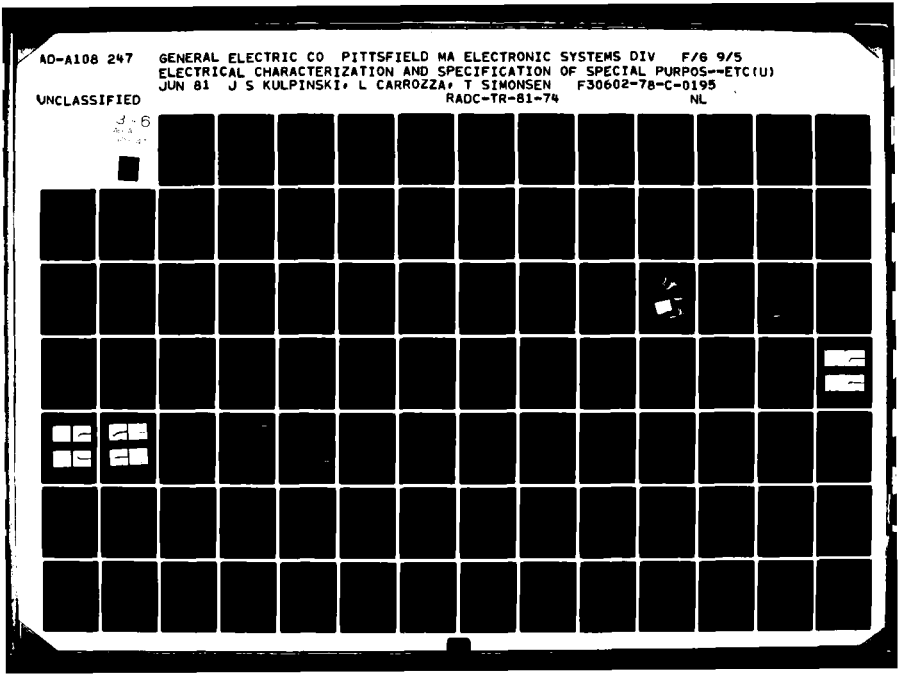
-55 DEG C

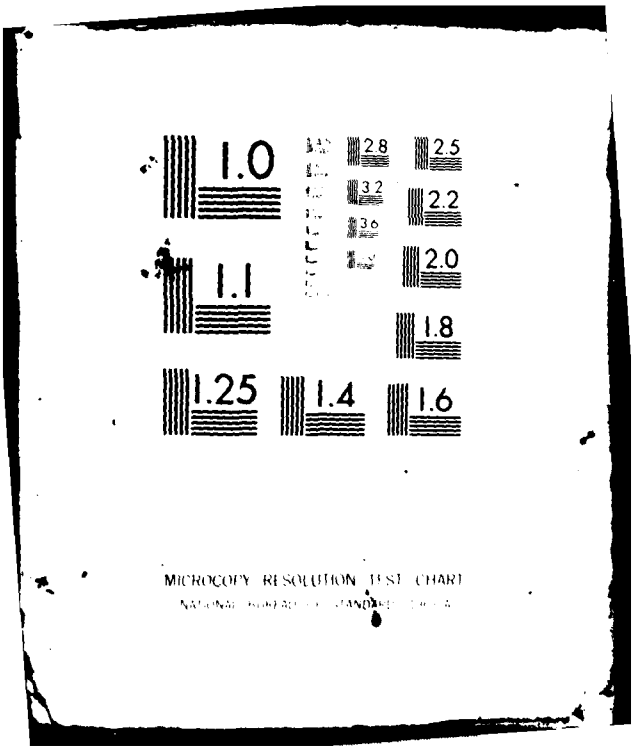
PARAMETER	LO-LIM	S/N51	S/N52	S/N53	S/N54	S/N56	S/N57	S/N58	S/N59	S/N60	S/N61	HI-LIM	
VIO(+CM) AT 3.5V,-36.5V	-5.00	-183.M	742.M	1.07	473.M	-7.25M	855.M	110.M	624.M	19.5M	-659.M	5.00	MV
VIO(-CM) AT 36.5V,-3.5V	-5.00	190.M	1.14	1.45	972.M	364.M	1.32	593.M	1.06	417.M	-289.M	5.00	MV
VIO(@CM) AT 15.0V,-15.0V	-5.00	110.M	1.06	1.41	876.M	274.M	1.24	492.M	959.M	327.M	-348.M	5.00	MV
VIO(-CM) AT 7.0V,-3.0V	-5.00	146.M	1.07	1.39	856.M	342.M	1.28	471.M	949.M	309.M	-270.M	5.00	MV
VIO(+CM) AT 3.0V,-7.0V	-5.00	-94.5M	817.M	1.08	525.M	101.M	948.M	158.M	668.M	43.1M	-559.M	5.00	MV
DELTA VIO/DELTA T (@CM)	-20.0	-4.32	413.M	7.92	6.08	31.1M	2.26	5.03	1.46	2.99	3.40	20.0	UV/DEG C
IIB(+CM) AT 3.5V,-36.5V	-75.0	32.9	15.8	24.0	21.3	17.7	16.5	13.1	12.7	21.2	37.5	75.0	NA
IIB(-CM) AT 36.5V,-3.5V	-75.0	32.4	15.6	23.5	21.0	17.2	16.2	12.8	12.4	20.7	36.7	75.0	NA
IIB(@CM) AT 15.0V,-15.0V	-75.0	32.5	15.6	23.5	21.1	17.2	16.2	12.8	12.5	20.7	36.7	75.0	NA
IIB(-CM) AT 7.0V,-3.0V	-75.0	33.3	15.9	24.1	21.5	17.7	16.6	13.2	12.8	21.3	37.8	75.0	NA
IIB(@CM) AT 3.0V,-7.0V	-75.0	33.8	16.2	24.5	21.9	18.0	16.8	13.5	13.0	21.7	38.6	75.0	NA
INPUT IMPEDANCE (ZI)	1.00	44.1	108.	43.0	72.7	48.7	79.3	74.3	94.4	45.7	27.7	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	150.M	127.M	135.M	130.M	125.M	75.0M	100.M	138.M	140.M	100.M	4.00	OHMS
RSC-SERIES CHG RESISTANCE	100.	147.	147.	148.	149.	148.	143.	164.	155.	147.	136.	600.	OHMS
GAIN ERROR (+/-11.5V CM)	-20.0M	-1.89M	-1.83M	-1.76M	-2.17M	-1.63M	-2.24M	-2.35M	-2.11M	-1.91M	-1.87M	20.0M	%
GAIN ERROR (+/-2.0V CM)	-40.0M	-7.75M	-6.75M	-9.00M	-8.00M	-7.38M	-8.13M	-9.12M	-6.38M	-6.13M	-8.87M	40.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	12.4	13.0	14.0	13.2	12.2	13.4	12.3	12.5	12.5	11.7	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-14.3	-11.0	-10.2	-10.4	-11.5	-9.81	-11.2	-9.61	-12.7	-13.7	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	106.	108.	107.	104.	116.	110.	103.	108.	103.	116.	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	108.	106.	116.	110.	104.	104.	110.	104.	113.	104.	200.	dB
FEEDTHRU REJ 0V TO 11.5V	80.0	92.8	91.5	93.7	93.0	91.2	98.9	92.2	91.4	91.0	95.2	200.	dB
FEEDTHRU REJ 11.5V TO 0V	80.0	96.1	94.5	98.7	95.3	95.7	89.9	94.6	93.9	93.3	96.2	200.	dB
FEEDTHRU REJ 0V TO -11.5V	80.0	94.8	95.2	94.5	101.	104.	96.8	115.	100.	92.6	95.1	200.	dB
FEEDTHRU REJ -11.5V TO 0V	80.0	98.1	89.7	93.2	98.2	89.1	94.0	92.4	88.9	94.6	97.8	200.	dB
HOLD STEP VOLTAGE (VHS+)	-5.00	290.M	166.M	533.M	481.M	180.M	263.M	344.M	316.M	386.M	540.M	5.00	MV
HOLD STEP VOLTAGE (VHS-)	-5.00	400.U	-275.M	-89.6M	-201.M	-265.M	-491.M	-293.M	-379.M	-202.M	-120.M	5.00	MV
ICC-SUPPLY CURRENT (@15V)	0.00	4.25	4.41	4.94	4.92	4.43	5.06	4.69	4.79	4.46	5.47	6.50	MA
IIH-LOGIC INPUT	0.00	2.96	2.41	3.38	3.31	2.52	2.50	2.45	2.22	2.99	4.02	20.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	3.21	2.66	4.46	3.27	2.86	2.47	2.40	1.17	2.92	3.73	20.0	UA
IIL-LOGIC INPUT	-3.00K	-1.05	-850.M	-1.75	-950.M	-1.25	-1.45	-1.65	-1.00	-1.00	-1.30	3.00K	MA
IIL-LOGIC REFERENCE INPUT	-3.00K	-450.M	-650.M	-200.M	-100.M	-750.M	-450.M	-350.M	-1.00	-500.M	-100.M	3.00K	MA
OUTPUT SHORT CIRCUIT (+)	-20.0	-17.7	-18.1	-19.0	-18.7	-18.4	-20.5 *	-18.0	-17.1	-18.5	-21.9 *	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	14.0	14.4	16.0	15.0	14.9	14.0	14.5	15.4	14.2	16.3	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	0.00	-12.5	-15.8	-6.00	-12.3	-17.5	-9.40	-11.7	-4.05	-11.3	-11.0	0.00	PA
HOLD CAPACITOR LEAKAGE(-)	0.00	-6.00	-9.45	-2.85	-5.90	-9.00	-5.80	-4.50	3.85	-6.50	-9.50	0.00	PA
HOLD CAP CHRG CURRENT(+)	-100.	-7.86	-10.2	-10.2	-10.2	-10.2	-10.2	-10.2	-10.2	-10.2	-10.2	-2.00	MA
HOLD CAP CHRG CURRENT(-)	2.00	7.53	7.86	8.15	8.15	7.86	8.27	7.56	7.60	8.07	8.74	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	1.62	1.61	1.61	1.60	1.62	1.59	1.61	1.74	1.61	1.61	2.00	V
TAQ (VIN=0V TO 10V STEP)	0.00	16.7	12.6	12.6	12.4	12.8	11.4	13.7	13.2	12.7	12.2	50.0	USEC
TAQ (VIN=0V TO -10V STEP)	0.00	15.9	14.3	11.1	11.1	13.9	13.9	14.1	12.9	13.2	13.2	50.0	USEC
TAQ (VIN=-10V TO 0V STEP)	0.00	15.8	12.6	12.7	12.2	12.7	11.3	13.8	13.1	12.7	12.8	50.0	USEC
TAQ (VIN=10V TO 0V STEP)	0.00	15.0	13.6	10.8	11.0	13.2	12.9	13.6	12.6	13.2	12.4	50.0	USEC
TAP (VIN=0V TO 10V STEP)	0.00	50.0	60.0	65.0	75.0	55.0	80.0	65.0	80.0	70.0	65.0	400.	NSEC
TAP (VIN=0V TO -10V STEP)	0.00	75.0	95.0	100.	120.	90.0	115.	105.	175.	105.	85.0	400.	NSEC
TAP (VIN=-10V TO 0V STEP)	0.00	45.0	55.0	60.0	65.0	50.0	75.0	60.0	75.0	65.0	60.0	400.	NSEC
TAP (VIN=10V TO 0V STEP)	0.00	80.0	105.	110.	130.	100.	125	115.	185.	115.	100.	400.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-22. Mfr. Code B Devices at -55°C.

AD-A108 247 GENERAL ELECTRIC CO PITTSFIELD MA ELECTRONIC SYSTEMS DIV F/G 9/5
ELECTRICAL CHARACTERIZATION AND SPECIFICATION OF SPECIAL PURPOS--ETC(U)
JUN 81 J S KULPINSKI, L CARROZZA, T SIMONSEN F30602-78-C-0195
UNCLASSIFIED RADC-TR-81-74 NL




1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
MICROCOPY RESOLUTION TEST CHART

MANUFACTURER CODE: C ; DEVICE TYPE: LF198; DATE CODE:7909 25 SEP 80 11:33:13

-55 DEG C

PARAMETER	LO-LIM	S/N78	S/N79	S/N81	S/N82	S/N83	S/N85	S/N86	S/N87	S/N88	S/N89	HI-LIM	
VIO(+CM) AT 3.5V,-26.5V	-5.00	453.M	714.M	-477.M	418.M	1.23	133.M	587.M	873.M	-428.M	1.15	5.00	MV
VIO(-CM) AT 26.5V,-3.5V	-5.00	1.17	1.50	498.M	1.33	2.15	1.06	1.50	1.78	575.M	2.10	5.00	MV
VIO(0CM) AT 15.0V,-15.0V	-5.00	491.M	953.M	-69.8M	767.M	1.59	517.M	991.M	1.20	14.9M	1.59	5.00	MV
VIO(-CM) AT 7.0V,-3.0V	-5.00	572.M	989.M	-45.7M	788.M	1.63	509.M	961.M	1.23	-15.8M	1.55	5.00	MV
VIO(+CM) AT 3.0V,-7.0V	-5.00	237.M	645.M	-475.M	364.M	1.17	48.5M	496.M	802.M	-510.M	1.03	5.00	MV
DELTA VIO/DELTA T (0CM)	-20.0	-3.79	182.M	-6.06	-7.73	-5.18	-5.82	-6.65	-5.84	-4.50	-12.0	20.0	UV/DEG C
IIB(+CM) AT 3.5V,-26.5V	-75.0	10.0	11.1	10.5	8.28	9.16	25.6	25.8	8.58	25.1	21.0	75.0	NA
IIB(-CM) AT 26.5V,-3.5V	-75.0	9.45	10.5	10.1	8.00	8.73	24.3	24.7	8.13	23.9	20.0	75.0	NA
IIB(0CM) AT 15.0V,-15.0V	-75.0	7.98	10.6	10.3	8.15	8.80	24.8	25.2	8.20	24.4	20.3	75.0	NA
IIB(-CM) AT 7.0V,-3.0V	-75.0	8.23	10.7	10.5	8.23	9.19	25.2	25.4	8.29	24.6	20.5	75.0	NA
IIB(0CM) AT 3.0V,-7.0V	-75.0	8.35	10.9	10.8	8.36	9.26	25.7	26.0	8.45	25.1	21.0	75.0	NA
INPUT IMPEDANCE (ZI)	1.00	40.5	40.9	60.1	82.6	53.5	17.5	20.1	51.0	19.4	22.9	500.	GOHM
OUTPUT IMPEDANCE (ZO)	0.00	125.M	175.M	75.0M	50.0M	75.0M	150.M	175.M	50.0M	150.M	175.M	4.00	OHMS
RSC-SERIES CMG RESISTANCE	100.	252.	248.	264.	273.	270.	255.	257.	273.	252.	251.	600.	OHMS
GAIN ERROR (+/-11.5V CM)	-20.0M	-3.24M	-3.39M	-3.98M	-4.05M	-4.12M	-4.43M	-4.04M	-3.95M	-4.80M	-4.50M	20.0M	%
GAIN ERROR (+/-2.0V CM)	-40.0M	-8.37M	-8.00M	-11.4M	-11.0M	-11.6M	-11.7M	-12.2M	-11.3M	-12.2M	-14.0M	40.0M	%
V-ADJ(+) AT 15.0V,-15.0V	6.00	11.1	11.4	10.1	10.7	11.6	11.1	11.7	11.2	10.6	12.0	30.0	MV
V-ADJ(-) AT 15.0V,-15.0V	-30.0	-14.8	-14.2	-16.3	-14.7	-14.6	-17.2	-17.0	-14.3	-17.6	-16.0	-6.00	MV
+PSRR AT 12.0V,-18.0V	80.0	103.	101.	99.3	99.6	98.7	99.4	97.9	98.9	98.7	96.5	200.	dB
-PSRR AT 18.0V,-12.0V	80.0	128.	116.	112.	142.	112.	125.	142.	126.	116.	122.	200.	dB
FEEDTHRU REJ 0V TO 11.5V	80.0	89.4	90.0	101.	93.0	92.3	91.0	91.5	92.0	98.1	81.8	200.	dB
FEEDTHRU REJ 11.5V TO 0V	80.0	90.1	94.1	94.2	92.6	94.2	92.2	92.6	93.5	94.4	80.3	200.	dB
FEEDTHRU REJ 0V TO -11.5V	80.0	92.5	107.	93.1	91.2	99.7	95.6	94.5	92.0	94.1	93.6	200.	dB
FEEDTHRU REJ -11.5V TO 0V	80.0	89.7	89.4	93.4	95.0	94.8	88.9	91.7	93.9	96.8	92.8	200.	dB
HOLD STEP VOLTAGE (VHS+)	-5.00	-372.M	-136.M	135.M	14.9M	84.4M	317.M	380.M	13.9M	325.M	382.M	5.00	MV
HOLD STEP VOLTAGE (VHS-)	-5.00	-687.M	-716.M	-302.M	-440.M	-290.M	-32.1M	105.M	-413.M	-105.M	905.M	5.00	MV
ICC-SUPPLY CURRENT (@15V)	0.00	4.04	4.31	5.67	5.71	5.59	5.75	5.60	5.55	5.75	5.73	6.50	MA
IIH-LOGIC INPUT	0.00	1.67	1.91	2.27	1.67	1.77	3.36	3.32	1.65	3.37	2.86	20.0	UA
IIH-LOGIC REFERENCE INPUT	0.00	885.M	995.M	1.50	845.M	855.M	1.79	1.70	820.M	1.62	1.38	20.0	UA
IIL-LOGIC INPUT	-3.00K	-1.65	-800.M	-700.M	-800.M	-850.M	-900.M	-900.M	-800.M	-700.M	-1.65	3.00K	MA
IIL-LOGIC REFERENCE INPUT	-3.00K	-350.M	-1.15	-1.00	-250.M	-800.M	-350.M	-600.M	-1.25	-900.M	-650.M	3.00K	MA
OUTPUT SHORT CIRCUIT (+)	-20.0	-20.8 *	-20.4 *	-27.9 *	-27.5 *	-27.5 *	-29.3 *	-29.1 *	-27.0 *	-30.0 *	-28.9 *	0.00	MA
OUTPUT SHORT CIRCUIT (-)	0.00	14.0	14.2	20.3 *	20.8 *	20.5 *	21.4 *	21.3 *	20.5 *	21.3 *	21.6 *	20.0	MA
HOLD CAPACITOR LEAKAGE(+)	0.00	-2.00	3.60	1.00	400.M	250.M	-5.15	-4.25	1.35	-5.00	-2.30	0.00	PA
HOLD CAPACITOR LEAKAGE(-)	0.00	-8.40	-600.M	-8.50	-3.25	-6.00	-18.7	-16.9	-3.20	-2.30	-10.5	0.00	PA
HOLD CAP CHRG CURRENT(+)	-100.	-7.96	-7.99	-7.46	-7.25	-7.33	-7.68	-7.61	-7.21	-7.83	-7.78	-2.00	MA
HOLD CAP CHRG CURRENT(-)	2.00	4.57	4.52	4.47	4.66	4.34	3.78	3.52	4.49	4.01	3.55	100.	MA
VTH(+)-LOGIC THRSHLD POS.	800.M	1.63	1.62	1.60	1.60	1.60	1.62	1.62	1.61	1.62	1.62	2.00	V
TAD (VIN=0V TO 10V STEP)	0.00	19.4	18.5	21.8	21.3	21.4	20.2	20.5	21.2	20.3	19.9	50.0	USEC
TAD (VIN=0V TO -10V STEP)	0.00	19.4	19.5	21.5	22.6	22.3	21.0	21.1	22.7	20.7	20.7	50.0	USEC
TAD (VIN=-10V TO 0V STEP)	0.00	19.4	18.7	20.4	21.5	21.1	20.3	20.8	21.5	20.0	19.8	50.0	USEC
TAD (VIN=10V TO 0V STEP)	0.00	19.4	19.5	21.4	22.5	22.3	21.0	21.0	22.6	20.7	20.9	50.0	USEC
TAP (VIN=0V TO 10V STEP)	0.00	40.0	50.0	40.0	40.0	35.0	35.0	30.0	40.0	35.0	25.0	400.	NSEC
TAP (VIN=0V TO -10V STEP)	0.00	80.0	80.0	45.0	55.0	40.0	25.0	80.0	50.0	25.0	15.0	400.	NSEC
TAP (VIN=-10V TO 0V STEP)	0.00	40.0	50.0	35.0	35.0	35.0	25.0	25.0	35.0	30.0	80.0	400.	NSEC
TAP (VIN=10V TO 0V STEP)	0.00	75.0	80.0	50.0	55.0	45.0	30.0	25.0	55.0	30.0	80.0	400.	NSEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-23. Mfr. Code C Devices at -55°C.

Table 5-24. Transient Response Data.

CONDITIONS: V_{in} = 100mV Step, C_H = .001 uF

C_L = 100 pF, R_L = 10KΩ

V_{cm} = -11.5V and +11.5V

LIMITS: TR (OS) = 40% (max.)

TR (ts) = 2.5 us (max.) to 10% of Final Value

MFR. CODE S/N	V_{cm} = -11.5V			V_{cm} = +11.5V		
	TR(OS) (%)	TR(ts) (us)	NOTES	TR(OS) (%)	TR(ts) (us)	NOTES
A-6	23	0.56		10	0.28	(1)
A-7	36	1.04	(1)	10	0.21	
A-8	32	0.22	(1)	20	0.22	
A-9	26	0.94		14	0.26	
A-14	28	0.23		16	0.21	
A-15	31	0.25		16	0.22	
A-16	24	0.23		10.5	0.21	
A-17	38	0.22	(1)	24	0.22	
A-18	7	0.65		7	0.64	
A-21	22	0.9?	(1)	18	0.24	
A-22	16	0.25		16	0.22	
A-23	17	0.3		12	0.3	
A-24	13.5	0.52		15	1.12	
A-25	13	0.3		16	0.4	
A-42	11	0.32		10	0.25	
A-43	28	0.21		14	0.21	
A-44	38	0.52		17	0.21	
A-45	13	0.29		9	0.28	
A-46	38	0.88		22	0.34	
B-51	14	1.04		15.5	1.2	
B-52	14.5	0.92		14.5	1.0	
B-53	12.5	0.8		13.5	0.92	
B-54	12	0.88		13	.92	
B-55	12	0.88		13	.92	
B-56	13	1.0		14	1.04	
B-57	16	0.84	(1)	17	1.04	
B-58	12	0.82		12	.85	
B-59	13	0.92		13.5	.96	
B-60	14	0.96		13	.96	
B-61	12	0.86		13.5	.78	
B-63	15	1.0		14.5	1.0	
B-64	11	0.98		14	1.04	
B-65	12	1.04		14.5	1.08	

NOTES: (1) Ringing is barely evident after one microsecond.

Table 5-25. Broadband Noise Data.

(Using a 10,000 V/V Gain Circuit
and 10 Hz to 10 kHz Bandwidth)

Limit = 10 uVrms (max)

Mfr. Code S/N	Sample Mode (uVrms)	Hold Mode (uVrms)
A-6	4.27	3.62
A-7	4.62	3.40
A-8	3.76	3.12
A-9	3.99	3.44
A-10	3.79	3.22
A-11	3.93	3.09
A-12	4.14	3.20
A-13	4.05	3.01
A-15	4.01	3.46
A-16	3.90	3.38
A-17	3.91	3.10
A-18	4.07	1.43
A-19	4.01	4.04
A-20	4.03	5.00
A-21	3.77	3.14
B-51	3.88	3.36
B-52	3.84	3.21
B-53	3.70	3.25
B-54	3.78	3.28
B-55	3.79	3.36
B-56	3.85	3.26
B-57	4.18	5.71
B-59	3.89	3.49
B-61	3.71	3.68
B-63	3.72	3.08
B-64	3.84	3.46

Mfr. Code S/N	Sample Mode (uVrms)	Hold Mode (uVrms)
B-65	3.86	3.37
B-66	3.56	3.87
B-67	3.78	3.36
B-68	4.02	4.55
B-4	4.18	3.56
B-5	4.15	3.72
B-6	4.14	3.44
C-74	4.09	3.62
C-75	4.32	3.83
C-77	4.16	4.21
C-78	4.40	4.17
C-79	4.17	5.18
C-81	4.16	3.75
C-82	4.19	3.85
C-83	4.13	3.77
C-85	3.95	3.55
C-87	4.22	3.93
C-88	3.91	3.67
C-89	3.94	3.97
C-90	4.01	4.50
C-71	5.52	4.49
C-72	4.20	4.48

Table 5-26. Hold Mode Settling Time Data.

(V_{in} = 0V, V_o ≤ 1 mV in hold mode)

Limit = 1.5 usec (max)

Mfr. Code S/N	Settling Time (usec)
A-6	0.63
A-7	0.85
A-8	0.70
A-9	0.55
A-10	0.72
A-11	1.24
A-12	0.90
A-13	0.74
A-14	0.80
A-15	0.56
A-16	0.50
A-17	1.15
A-18	0.37
A-19	0.36
A-20	0.55
A-21	1.38
B-51	0.51
B-52	0.64
B-53	0.52
B-54	0.59
B-56	0.64
B-57	1.60
B-59	0.68
B-61	0.64

Mfr. Code S/N	Settling Time (usec)
B-63	0.60
B-64	0.64
B-65	0.65
B-66	0.60
B-67	0.60
B-68	0.60
B-4	0.52
B-5	0.70
B-6	0.80
C-71	0.68
C-72	0.69
C-73	0.74
C-74	0.66
C-75	0.68
C-76	0.80
C-77	0.70
C-78	0.68
C-79	0.71
C-81	0.62
C-82	0.66
C-83	0.66
C-85	0.58
C-87	0.64
C-88	0.57

SECTION VI

SURVEY OF DATA CONVERTER DEVICES

TABLE OF CONTENTS

SECTION VI

SURVEY OF DATA CONVERTERS

Data converters are widely used in instrumentation, control, simulation, telemetry, video, radar, data processing, communications, and most recently, on-line digital signal processing. As costs decline and performance improves (the current trend), applications continue to grow as traditional analog techniques are replaced by digital signal processing approaches.

Introduction

In November of 1979, a study of available converter microcircuits (monolithics and hybrids), suitable for future JAN 38510 specification, was initiated. The intent was to identify devices which might become suitable standard devices in future military systems. Plans for detailed slash sheet development could be formulated from the results of the study.

The approach taken was to solicit recommendations from both users and device manufacturers. A survey letter was prepared and mailed to twenty-eight device manufacturers and twenty-two user companies. Copies of the survey letters are included in Figure 6-1 (manufacturers) and Figure 6-2 (users).

Additional usage information was obtained from various EIA, DESC, and RADC device lists. Industry data sheets, device catalogs, and technical articles provided additional technical information.

Assessment of Converter Technology

Data converter devices are produced by a majority of the major semiconductor houses, in addition to a host of thick-film and thin-film hybrid manufacturers, as well as discrete module manufacturers. Data converter technology is evolving rapidly and without any significant degree of standardization. The lack of standardization is not surprising when one considers the variables associated with data converter devices:

semiconductor technology ... bipolar, I^2L, CMOS, NMOS, CCD.
manufacturing technology ... monolithic, hybrid, multi-chip, discrete.
conversion technique ... successive approximation, dual slope, quad slope, parallel, companding, etc.
converter resolution ... one to twenty bits
converter codes ... true or complementary binary or BCD, offset binary, sign magnitude binary, one's complement, 2's complement, gray code.
output circuit options ... parallel/serial, voltage/current

logic control options
internal or external voltage reference
internal or external clock
microprocessor compatibility --- tristate output buffers/latches, digital control interfacing
range of analog signals, reference
parameter differences... accuracy (absolute and relative), conversion speed, linearity (end point or best fit), noise, rejection, etc.
power dissipation
case outline

The survey excludes discrete modular devices, since it focuses upon MIL-M-38510, which is a microcircuit specification. Compared to monolithics, hybrid data converters offer superior speed-accuracy compromises with more features and fewer external components, but at higher cost. Monolithics are displacing hybrids in many user applications, due to cost and reliability considerations as well as function/performance. More functions are included in the newer devices, and with on-chip trimming and/or innovative circuit techniques, the levels of device performance continue to improve.

Twelve bit D/A converters on a chip are readily available, as are 10-bit A/D converters. Some 12-bit integration-type monolithic A/D converters are also available but the popular 12-bit successive approximation A/D *on-a-chip is not here yet.* The two-chip (AD574) 12-bit A/D is evidence of how close the technology is to that goal, however.

Self-contained microprocessor compatibility is a popular feature of many new devices, whereby tri-state output buffers and certain digital control interfacing capability is included on the chip.

Whereas successive approximation converters are the most popular, the much slower integrating types are needed for high noise rejection and high accuracy, especially in system instrumentation applications. At the other extreme, the very fast parallel (flash) converters are needed for video signal processing and are now being produced with LSI technology.

Responses to Survey Letters

Responses to the survey letters were light, with six of twenty-two users and ten of twenty-eight manufacturers responding. None-the-less, the responses are summarized in Tables 6-1, 6-2 and 6-3. To protect the business interests of manufacturers, military programs are not named in the tables. Also, discrete modular type devices are eliminated since MIL-M-38510 is a microcircuit specification. Devices already specified in 38510, or in-process for 38510 specification, are also excluded from the responses.

GENERAL ELECTRIC

ELECTRONIC SYSTEMS DIVISION

GENERAL ELECTRIC COMPANY, 100 PLASTICS AVENUE, PITTSFIELD, MASS 01201
Phone DIAL COMM 8 236- (413) 494-3661

ORDNANCE SYSTEMS

5320-427-JSK:ms
November 14, 1979

MEMO TO DATA CONVERTER DEVICE MANUFACTURERS

GE Ordnance Systems is currently under contract to Rome Air Development Center to characterize data converter devices for MIL-M-38510 (JAN) slash sheets. As part of this effort, we are performing a study of available converter micro-circuits (monolithics, hybrids) suitable for future JAN 38510 specification. Manufacturer recommendations are an important consideration, and that is what we are seeking via this letter.

Devices suited for military programs should be of high quality and reliability, capable of operating in the temperature range of -55°C to +125°C, and capable of meeting the general requirements of MIL-M-38510D. Please list eligible devices which you manufacture, in order of your chosen priority, on the attached form, and return as soon as possible (Dec. 15 deadline).

For your information, the following devices are already specified in this program:

MIL-M-38510/113	DAC08, DAC08A 8-bit D/A Converters
MIL-M-38510/120	MN5200, MN5210 family, 12-bit A/D Converters
MIL-M-38510/121	AD562, HI562 12-bit D/A Converters

It is anticipated that characterization effort will commence on the following devices in the very near future:

AD563 - addition to /121

7520, -21, -23, -41 CMOS 8, -10, -12-bit DACs

Any questions concerning this request should be directed to the undersigned.

J. S. Kulpinski
Circuit Design Engineering
Room 2372 - Extension 3661

Enclosure

Figure 6-1 Manufacturer Survey Letter

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ORDNANCE SYSTEMS

5320-450-JSK:ms
December 4, 1979

MEMO TO DATA CONVERTER DEVICE USERS

GE Ordnance Systems is currently under contract to Rome Air Development Center to characterize data converter devices for MIL-M-38510 (JAN) slash sheets. As part of this effort, we are performing a study of available converter micro-circuits (monolithics, hybrids) suitable for future JAN 38510 specification. User recommendations are an important consideration, and that is what we are seeking via this letter.

On the attached form, please list data converter devices which you are currently using in Military applications, or which you are considering for usage in future designs. D/A, A/D, trignometric converters, and even associated products such as V/F converters, sample holds, references, analog multiplexers, etc. are of interest to us.

The results of this survey will be compared with manufacturer recommendations to formulate a basis for future JAN specification development efforts.

In return for your completion of this survey, we will send you a list of current JAN linear interface specs issued, in-process, and planned, on a recurring basis.

This survey has been authorized by Thomas Dellecave of RADC (315-330-2946). Response is requested by Dec. 20.

Please forward this survey to an appropriate individual within your company. Thank you for your cooperation.

J. S. Kulpinski, Lead Engineer
Circuit Design Engineering
Room 2372

Enclosure

Figure 6-2 User Survey Letter

Table 6-1. Summary of Survey Responses
D/A Converters

	Device Type	#Bits Resolution	User Recommending	Usage P = Planned C = Considered U = In use	Mfr. Rec.
1.	DAC01	6	GE-ESPD	U	-
2.	ADH030	12	-		ILC-DDC
3.	DAC80	12	GE-SSD	U	-
4.	DAC85	12	-	-	Burr-Brown Analog Devices
5.	DAC87	12	-	-	Burr-Brown Analog Devices
6.	DAC100	10	NASA/GSFC GE-SSD	U U	PMI
7.	DAC331	10, 12, 14	NASA/GSFC	P	Hybrid Systems
8.	DAC335	12			Hybrid Systems
9.	DAC337	8, 10	-	-	Hybrid Systems
10.	DAC347, -348	10, 12	-	-	Hybrid Systems
11.	DAC356	12	-	-	Hybrid Systems
12.	DAC397	12	-	-	Hybrid Systems
13.	AD561	10	GEOS	U	Analog Devices
14.	AD565, H1565	12	GE-ESPD GEOS	U C	Analog Devices, Harris, Fairchild
15.	AD566	12	GEOS	C	Analog Devices
16.	DAC1000 -1008	8, 9, 10	-	-	National Semic
17.	DAC1020, -21,-22	10	-	-	National Semic
18.	DAC1220, -21,-22	10	-	-	National Semic
19.	MN3850	12	Rockwell	U	-
20.	AM6012	12	-	-	AMD
21.	AD7524	12	GEOS	P	-
22.	AD7530	10	NASA/GSGC	P	-
23.	8641	12	-	-	Teledyne
24.	DACSL	12	Rockwell	U	ILC-DDC

Table 6-1. Summary of Survey Responses
D/A Converters (Cont'd)

	Description/Features	Technology
1.	3-input 3-output options, low power	Monolithic, bipolar
2.	30 nsec settling, low glitch, int. ref.	Hybrid, thin film + MSI
3.	300 nsec settling, int. ref. + op amp	Hybrid
4.	300 nsec settling, low cost, v or i output	Hybrid
5.	High accuracy vs temp.	Hybrid
6.	Low non-linearity vs temp.	2-chip bipolar
7.	4-quad mult, low pwr, 1-supply, 7521-41 equiv.	Hybrid, thin film
8.	Low power, DAC85 equiv	Hybrid
9.	Adjust-free, int. ref. + output amp.	Hybrid, thin film
10.	Low power, high perf, gen'l purpose	Hybrid, thin film
11.	Low power, low cost	Hybrid
12.	20 nsec settling, ECL compatible	Hybrid
13.	High accuracy, temp-stable	Monolithic, bipolar/Si-Cr
14.	200 nsec settling, stable int ref	Monolithic, bipolar/Si-Cr
15.	Low cost, 200n sec settling, low power	Monolithic, bipolar/Si-Cr
16.	uP compatible, double-buffered like AD7520	Monolithic, CMOS/Si-Cr
17.	MDAC, low power, AD7521 equiv	Monolithic, CMOS
18.	MDAC, low power, AD7531 equiv	Monolithic, CMOS
19.	Int. ref. and fast output amp, high perf	Hybrid
20.	No-trim, segmented, 250 nsec settling, low cost	Monolithic bipolar
21.	4 quad mult., uP interface, low cost	Monolithic bipolar
22.	Low power, low tempco, 500 nsec settling	Monolithic, CMOS
23.	MDAC, low power, AD7541 equiv.	Monolithic, CMOS
24.	Input register with strobe	Hybrid

Table 6-2. Summary of Survey Responses
A/D Converters

	Device Type	#Bits Resolution	User Recommending	Usage P = Planned C = Considered U = In use	Mfr. Rec.
1.	ADC0801	8	-	-	National Semi
2.	TDC1001J	8	NASA/GSFC	P	-
3.	MN5122	8	Rockwell	U	-
4.	JCL7132	8	-	-	Intersil
5.	8703*	8	-	-	Teledyne Semic
6.	8704*	10	-	-	Teledyne Semic
7.	AD571	10	JPL,NASA/GSFC	P	Analog Devices,
			NWSC	U	Fairchild
8.	ADC85	12	NASA/GSFC	P	-
			Lockheed	U	
9.	ADH8586	12	-	-	ILC-DDC
10.	AD574	12	GE-ESPD	P	Analog Devices,
			NWSC	U	Fairchild
11.	ADC581B	12	-	-	Hybrid Systems
12.	ADC582B	12	-	-	Hybrid Systems
13.	ICL7109	12	-	-	Intersil
14.	ADC7556	12	GE-ESPD	U	-
15.	ADH8516	12	-	-	ILC-DDC
16.	8705*	12	-	-	Teledyne Semic.
17.	AD7550	13	NASA/GSFC	P	-
18.	8750*	3 1/2 digits	-	-	Teledyne Semic.
19.	8751*	3 1/2 digits	-	-	Teledyne Semic.

Table 6-2. Summary of Survey Responses
A/D Converters (Cont'd)

	Description/Features	Technology
1.	uP compatible, low cost, general purpose, S-A,int. ref.	Monolithic CMDS
2.	2.5 mHz conv. rate, +/- 1/2 LSB linearity	Bipolar LSI
3.	Low cost, no adjustments, S-A, 2-5 usec.	Hybrid, thin film
4.	uP compatible, low cost, general purpose, S-A, int .ref. ADC0801 equiv.	Monolithic CMOS
5.	Charge balancing conv, low cost, uP interface,1.8 msec	Monolithic CMOS
6.	Charge balancing conv, low cost, uP interface, 6 msec	Monolithic CMOS
7.	Self-contained int. ref. + clock, 25 usec, S-A	Monolithic
8.	Self-contained, int ref + clock, 10 usec	Hybrid, thin film
9.	Self-contained, int. ref. + clock 5 usec	Hybrid, thin film + MSI
10.	uP interface, int ref. + clock, S-A	2-chip monolithic
11.	ADC85 equiv, /DW power, 20 upc	Hybrid, thin film
12.	Equiv to MN5216	-
13.	Dual-slope integrating, uP interface	Monolithic CMOS
14.	Low power, low cost, uP compatible, S-A, 50 usec.	Hybrid
15.	uP interface, 2 usec, int./ext. clock	Hybrid, thin film + MSI
16.	Charge balancing conv, low cost, uP interface, 24 msec	Monolithic CMOS
17.	uP interface, quad slope, precision	Monolithic CMOS
18.	High accuracy (.025%), low power, 12 msec	Monolithic CMOS
19.	Auto zero, auto polarity, low-power, int./ext clock	Monolithic CMOS

Existing MIL-M-38510 Data Converter Specifications

Data converters presently specified in MIL-M-38510 slash sheets are listed in Table 6-3. The DAC08, -08A devices are popular 8-bit monolithic (bipolar) D/A converters with dual complementary current outputs, are fully output voltage compliant, low cost and multi sourced. The 562 is a higher resolution, 12-bit D/A converter, slower than the DAC08, and lacking output voltage compliance, but otherwise a high performance device sourced by two manufacturers at a medium-high cost. The CMOS 7520 MDAC family now being characterized fills in the gap of lower cost, four-quadrant multiplying DACs with low power consumption and relatively fast settling time.

The A/D converter family presently being characterized for MIL-M-38510 is the first hybrid device to be specified in the linear/interface category. These 12-bit converters are successive approximation, medium-high conversion speed (12 usec for the 5210 series), high cost devices sourced by three vendors (not all types, and not yet available from all).

Table 6.3. JAN 38510 Data Converters.

	Device Type							
Generic Family	01 (09)	02 (10)	03 (11)	04 (12)	05 (13)	06 (14)	07 (15)	08 (16)
/113 D/A Converters 8-Bit	DAC08	DAC08A						
/121 D/A Converters 12-Bit	AD562	HI562	AD563					
/127 D/A Converters (CMOS) 8, 10, 12-Bit	7523	7520	7521	7541	1020	1220	1218	
/120 A/D Converters 12-Bit	5200 (5210)	5203 (5213)	5201 (5211)	5204 (5214)	5202 (5212)	5205 (5215)	5206 (5216)	5207 (5217)

Recommendations for Specification Development

Recommendations for future JAN 38510 specifications are influenced by several factors (listing sequence is not significant):

- o Expressed manufacturer interest in supporting slash sheet development evidenced by line certification and participation at JC-41 meetings.
- o Availability of devices at distributors and from manufacturers for use in characterization. Preferably, devices from manufacturers should be supplied with data.
- o User need, as determined from organized committees, government procurement lists, or expressed need from military system manufacturing companies.
- o Availability of multiple sources. This is desirable but not an absolute constraint. Often, second source devices are not totally interchangeable with the original part.
- o Device technology. At this time, there is more emphasis on monolithic devices over hybrid devices, due to difficulties in the certification of hybrid manufacturers. Hybrids are necessary to achieve certain performance requirements in some cases, however (e.g. 12-bit A/D Converters).
- o Device vintage. There is a stronger tendency to develop slash sheets for devices of recent vintage, which may have superior performance parameters due to technological advances. This is accompanied by a risk factor that the part may have some problem that has not yet surfaced, or that the part may not be well-received by users and may therefore be discontinued by the manufacturer.
- o Device features. Devices which offer performance, packaging, or reliability advantages beyond those devices presently specified in MIL-M-38510 are preferred over devices which are roughly equivalent to existing 38510 parts.

In making recommendations for future characterization, GEOS does not intend to identify specific devices, due to the sensitivity involved in selecting one manufacturer's product over that of another. Instead, there are general recommendations and guidelines for device selection that can be made based upon the current technology vs. the existing MIL-M-38510 converter devices. The following is a list of GEOS recommendations for future device selection.

- o Low to medium cost A/D converters having 8 bit to 12 bit resolution should be given high priority for specification development. Monolithic devices are preferred at present until certification requirements for hybrids are finalized. Successive approximation (S/A) converters are the most popular and versatile, and therefore should be given priority. While monolithic 12 bit S/A A/D converters do not yet exist, there are 2-chip devices available. Devices designed for the other extremes of conversion speed - i.e. the slow integrating type and the very fast flash converters - should eventually be included in the JAN 38510 system to satisfy growing user needs for these products.

- o For both D/A and A/D converters, devices having microprocessor-compatibility should be given priority. Microprocessor compatibility is especially desirable for 8-bit devices.

- o Improved versions of existing JAN 38510 devices should be fully considered, since the characterization effort is lessened, and such devices can be added to existing slash sheets.

- o Higher resolution data converters (beyond 12 bits) should not be considered for JAN 38510, due to anticipated problems in developing and correlating automatic tests for them. When more experience is realized with the current 12-bit converters, higher resolution devices can then be considered.

SECTION VII

MIL-M-38510/121

12-Bit D/A Converters

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SECTION VII

12-Bit D/A Converters

MIL-M-38510/121

7.1 Introduction

The increased use of microprocessors in military systems has stimulated interest in JAN 38510 specification development of data converters and associated devices which are needed to interface analog sources, sensors, loads and displays with digital processing hardware. In 1978, the first JAN D/A Converter slash sheet was developed, MIL-M-38510/113. The DAC08 and DAC08A devices, 8-bit monolithics with dual complementary current outputs, fully voltage compliant, low cost and multi-sourced were selected for the slash sheet.

The need for higher-resolution D/A Converters will be met by MIL-M-38510/121, 12-bit D/A Converters. Monolithic 12-bit converters have only recently begun to displace the hybrid devices which have predominated the marketplace in past years, and there is reason to believe this trend will continue. The 562 is one of the first 12-bit monolithics that is multi-sourced and has been identified by users as a desirable component for military systems.

While multi-sourcing has many advantages, it presents some difficulty in preparing a common specification for data converters. Of three manufacturers which offer the 562, no reasonable compromise of specifications could be negotiated to include even two manufacturers on one device type. Consequently, there are two device types in the slash sheet, each sourced by only one manufacturer; the third device is not included at this time. Instead of characterizing 562 devices from three different manufacturers, a 563 D/A Converter was added to the specification as device type 12103.

Table 7-1 lists the device types specified for this characterization.

Table 7-1. Device Types Specified

Device Type	Generic Type	Manufacturer	Case Type	No of Term	Reference
12101	AD562	Analog Devices	DIP	24	Ext.
12102	HI562	Harris	DIP	24	Ext.
12103	AD563	Analog Devices	DIP	24	Int.

7.2 Description of Device Types

The 562 is a monolithic 12 bit D/A Converter with guaranteed monotonicity over the full military operating temperature range, -55°C to +125°C. The device is mounted in a hermetically sealed ceramic 24 lead dual in-line package. The 562 accepts a reference voltage of 0 to + 10 V and provides a binary weighted output current proportional to the product of the digital address input and the reference voltage. When the reference voltage is variable the device is a two quadrant DAC. On the other hand, when the reference voltage is fixed the device is simply a DAC with a nominal output current of -2 mA for device type 01 and -5mA for device type 02. Laser-trimmed internal gain, voltage-range and bipolar offset resistors are incorporated to provide accurate output voltages when used in conjunction with an external amplifier. Scaling errors are minimized because of low resistor tracking TCR; approximately 1 ppm/C°. The following ranges can be pin-programmed:

0 to + 10 V, 0 to + 5 V,
- 5 to + 5 V, -2.5 to + 2.5 V,
-10 to + 10 V

In the unipolar mode, the digital code for the device is natural binary "positive true". In the bipolar mode, the digital code is offset binary.

Address In	Unipolar	Bipolar
0000 0000 0000	0 V	- 10.000 V
1000 0000 0000	+ 5.000V	0 V
1111 1111 1111	+ 9.99878 V	+ 9.99572 V

The device is CMOS or TTL compatible. With pin 2 connected to pin 1 the device is CMOS compatible and the internal logic threshold is $V_{CC}/2$ and the voltage may be 4.75 to + 15.8 V. With pin 2 open for device type 01 and grounded for device type 02 the logic threshold is approximately + 1.4 V and the device is TTL compatible with V_{CC} = + 5 V ± 10%.

In device type 01 and 03, the current output is the weighted sum of the outputs of three similar groups of binary scaled quad current generators, controlled by V_R. The logic inputs steer these currents through non-saturation bipolar-transistor current switches to either ground or the respective quad output bus. The output currents from the 2nd and 3rd quads are attenuated by 16:1 and 256:1 respectively. The attenuated output are then summed with the unattenuated output of the 1st quad. The output current is then the sum of 12 individually switched currents having a binary relationship.

The current generating transistors from each quad group have emitter areas in the ratio of 8:4:2:1. The ladder network resistances are in the ratio of 1:2:4:8. With equal voltages applied to the resistors, the emitter currents are therefore in a binary ratio. Because of the weighted emitter area, the transistors operate at equal emitter current densities and therefore have nearly equal V_{BE}'s and h_{FE}'s. The control amplifier (A1) drives the bases ot the constant current transistors and a reference transistor, which has h_{FE} and V_{BE} matched to those of the constant current and bit switching transistors.

Figure 7-1 is a Functional Block Diagram and an Operational Diagram of the AD562.

In device type 02, the 562 current output is derived from an R-2R resistive ladder network. The input currents to this ladder network is generated by twelve identical bipolar current sources. These currents are steered to either the device ground pin or to separate junction nodes of the resistor ladder network. The R-2R ladder network provides proper weighting to each of the input currents so that the output current has a binary relationship to the input current. Since each source contributes current independent of the other sources, the output current is the sum of the weighted currents applied to the network.

Figure 7-2 is a Block Diagram of the HI-562 and Figure 7-3 is an Operational Diagram of the HI-562.

7.3 Test Development

Devices used in these characterizations were selected by a joint decision of RADC and the Circuit Design Engineering Activity of GEOS. Devices were obtained from three manufacturers on the JC-41 Committee. Table 7-2 lists the device types characterized.

Table 7-2. Device Types Characterized.

Device Type	S/N	Manufacturer	Date Codes
12101	5,19,20,	AD	7824
	21,25,35,48	AD	7824
	4310-4315	AD	7917
	1-5*	AD	-
12102	6,7,13,22	Harris	7838
	9[illegible],50,87,88	Harris	-
-	1-5	PMI	-

*S/N's 1-5 supplied by Analog Devices were rejected devices to be used for test circuit development.

Test Parameter Development

The test parameters were developed by GEOS and the cognizant vendors supplying devices for characterization. MIL-M-38510 slash sheets developed for digital devices were reviewed and the standard digital input parameters were selected for inclusion into MIL-M-38510/121. In addition, the standard analog test parameters were also included as well as the test parameters unique to D/A Converters. Table 7-3 is a list of the test parameters measured during characterization of the 562 D/A Converters.

Table 7-3. Test Parameters for Characterization.

Item No	Symbol	Parameter
1	I_{cc}	Supply current from V_{cc}; V_{cc} = 15 V
2	I_{ee}	Supply current from V_{ee}; V_{ee} = - 15 V
3	I_{IH}	Logic "1" input current; V_{cc} = 15 V
4	I_{IL}	Logic "0" input current; V_{cc} = 15 V
5	I_{FS}	Full scale current; all bits on
6	I_{ZS1}	Zero scale current (TTL); all bits off

Table 7-3. Test Parameters for Characterization. (cont'd)

Item No	Symbol	Parameter (See Page for definitions)
7	I_{ZS2}	Zero scale current (CMOS); all bits off
8	D-I_{ZS}/D-T	Zero scale current drift; V_{cc} = 5 V
9	V_{FSI1}	Gain error (TTL); V_{cc} = 5 V
10	V_{FSI2}	Gain error (CMOS); V_{cc} = 15 V
11	D-V_{FS}/D-T	Gain drift; V_{cc} = 5 V
12	BPOE	Bipolar offset error; V_{cc} = 5 V
13	D-BPO /D-T	Bipolar offset drift; V_{cc} = 5 V
14	V_{FSI3}	Bipolar gain error; V_{cc} = 5 V
15	+PSS1	Power supply sensitivity at full scale from V_{cc} (TTL) V_{cc} = 5 V
16	+PSS2	Power supply sensitivity at full scale from V_{cc} (CMOS) V_{cc} = 15 V
17	-PSS1	Power supply sensitivity at full scale from V_{ee}. V_{ee} = - 15 V
18	L	Bit linearity error; V_{cc} = 5 V
19	BWE	Bit weight errors
20	$\sum$BWE	Summation of bit weight errors
21	MC	Major carry error; V_{cc} = 5 V
22	M	Monotonicity
23	t_{SLH}	Output current settling time 0 to FS; V_{cc} = 5 V
24	t_{SHL}	Output current settling time FS to 0; V_{cc} = 5 V

The test circuits for items 1 through 19 were developed for the S3260/70 Automatic Tester interface, and test circuits for items 23 and 24 were developed for bench type testing at 25°C only.

For the purpose of characterization, the bit linearity error test was performed on all of the 4096 different codes. Because of the measurement problems, and the time required to perform bit linearity error test for all codes, the vendors were very adamant about performing some abbreviated test that would insure device performance.

Initially, the vendors and GEOS agreed to a test that would measure the bit linearity error polarity and magnitude as each bit is turned on one at a time with all other bits turned off. In this test approach it is assumed that the total error at the output of the module is the superimposed contribution of the individual errors and that the maximum positive error can be located by simultaneously activating those bits having individual positive errors. Similarly, it was assumed that the maximum negative error can be located by simultaneously activating those bits having individual negative errors. The characterization of devices received from two manufacturers showed that this abbreviated test approach worked well for one manufacturer but did not work at all for the other manufacturer.. Devices from both AD and Harris, however, passed the all codes bit linearity error test. PMI devices were removed from the characterization effort.

By using the all codes bit linearity error data, GEOS examined several possible abbreviated methods. These methods involved:

a) variations of the single bit superposition method, described above,

b) successive approximation techniques where bits are turned on one at a time as in a), however, after each bit is turned on a decision is made to determine if the action added to or subtracted from the previous error measurement.

c) segmentation of the code word pattern and measurement of the bit linearity error at the code words which begin segment.

d) combinations of the above methods.

The final method recommended by GEOS to the JC-41 Committee Members was a method that combined the single bit superposition method for the lower eight bits with a 16-segment method that measured the worst case positive and the worse case negative bit linearity error for the upper four bits.

Test Adapter Development

At the beginning of the test development, the accuracy and capability of the S3260/70 Automatic Test Set is determined for each parameter. Because of the limitations of the test set in the measurement of precision linear devices a special interface test adapter was developed.

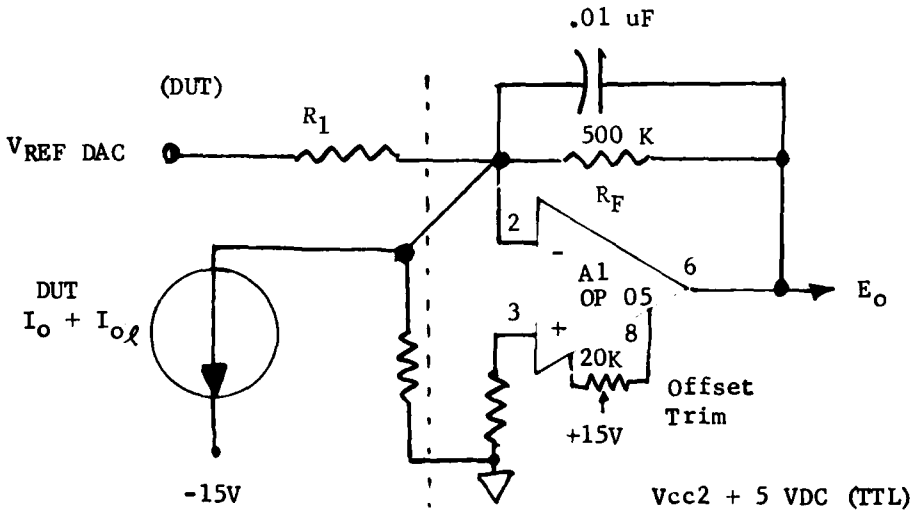
One of the primary considerations in attempting to test a 12 bit D/A Converter on the Tektronix S3260/70 is, "How does one measure DAC output linearity to ± .001% and fast enough" that the S3260/70 isn't tied up for long periods of time? GEOS chose to implement a comparative type test which utilizes a Reference Module in conjunction with the S3260/70 test adapter to test the device's linearity and accuracy. The reference module contains an 18 bit D/A Converter (12 MSBs used) some switches, some buffer amplifiers, and active ground drivers. It was designed to interface with D/A Converters with 12 bits of resolution. It contains switching, logic, and buffer amplifiers and is capable of interfacing accurately with D/A converters of various ranges and codes. It was primarily designed to interface with the 562 series of 12 bit D/A Converters. A schematic of the adapter test circuit for static test measurement is shown in Figure 7-4.

Another consideration in testing devices with such accuracy on the S3260/70, is grounding and line drops. If the test circuits were designed for bench test, the circuitry would be kept close together and unipoint grounding employed. All of the precautions would be taken to minimize voltage drops on critical wires, avoid ground loops, and prevent oscillations. However, maintaining the close proximity and unipoint grounding on the S3260/70 is next to impossible. Therefore, an alternate approach was taken. Active ground drivers (See Fig. 7-5) consisting of a cascaded connection of an OP 05 amplifier and a hybrid driver (LH0002) in the voltage follower configuration were employed to drive the DUT and adapter grounds separately to the same ground potential as the reference module ground. Care was taken in the selection of adapter devices to minimize power consumption (by using low power Schottky for example) and keeping the driven grounds disconnected from machine ground. Offset voltage trims were implemented on the OP 05s to enable adjustment of the DUT and adapter grounds to 0 V relative to the Ref. D/A ground. The technique worked exceptionally well and contributed largely to the ultimate success in obtaining better than ± .05 LSB measurement accuracy on linearity measurements. A 12 bit D/A converter in the unipolar mode on the 0 to 10 V range has an LSB voltage increment value of 2.44 mV., ± .05 LSB equals ±.122 mV.

Also employed, as shown in Figure 7-4, are buffer amplifiers for the Reference Voltage output (A3) and for the Reference D/A output (A4). The amplifiers are differential and remote ground and output sense lines are employed to prevent line drop from deteriorating measurement accuracies.

It should be noted that the reference module when used with the S3260/70 test adapter provides a simple setup for bench testing. Aside from some test equipment, all that is required is the undersocket card interface. This feature enables the DUT to be tested with access to all of the adapter circuitry on the under socket card that is not readily accessible on the S3260/70.

The method employed for testing the linearity and accuracy of the 562 is illustrated in Figure 7-4 and in the following simplified schematic.



Simplified schematic of error amplifier.

The reference D/A output voltage is fed to the 10 volt span resistor (DUT pin 10) via relays K1 and K5. Both Reference D/A output drive and Reference D/A output sense lines are switched separately and connected together at DUT pin 10. For any given DUT address the difference between the DUT output and the Reference D/A output are compared,

inverted and amplified. (Use of the 10 volt span resistor is possible because the span resistors are laser trimmed to compensate for full scale current deviations from nominal and provide nominal output voltage when used in conjunction with a zero offset external op amp. If full scale current is low by 10% from nominal then the span resistor will be high by 10%.)

With all relays deenergized the error amplifier offset voltage is trimmed to 0V, E_o = 0 V. The Reference voltage is adjusted to + 10.0000 V at adapter pin 22, as read on a Fluke 8502 DVM. The Reference D/A address inputs are set to all zeros, relays K1 and K5 are energized and the Reference D/A output voltage at DUT pin 10 is adjusted to (offset adj) to - 10.000 V, as read on the Fluke 8500. The Reference D/A address inputs are then set to all ones and the Reference D/A output voltage at DUT pin 10 is adjusted (gain adj) to + 9.9951 V, as read on the Fluke 8500. The Reference D/A output voltage, the Reference voltage, and the error amplifier have been calibrated. With the DUT address bits all zeros, the Reference D/A output voltage is incremented by a small but finite voltage (14 bits) and the change in voltage at the error amplifier output noted. Dividing the change in output voltage by the change in input voltage provides the error amplifier gain (inverted). This gain value is then used by the automatic test set to calculate the true device output current errors. It should be noted that the Reference DAC employed required complimentary logic. In Table III of the slash sheet the codes are shown as such, eg all 0's applied to the DUT provides a nominal - 9.997 V (equivalent) output. All 1's applied to the Reference D/A provide a nominal + 9.9975 V output and all "0"s applied to the Reference D/A provide a nominal 0 V output.

To measure linearity, the DUT equivalent output voltages (I_o R_1) at zero and full scale are obtained by measuring E_o (adapter pin 21) for all DUT and Reference D/A out bits off and for all DUT and Reference D/A out bits on. The DUT equivalent output voltages are calculated using the following relationship

$$I_o R_1 = -\frac{E_o}{G} + \text{Reference D/A out; (where G = error amp gain)}$$

A straight line is established between these two points and subsequent measurements of DUT outputs for any given address are compared to the straight line which is the ideal linearity curve.

One other important factor to consider in testing 12 bit D/A converters is temperature stability. Warm up time before test varies from vendor to vendor. The device dissipates as much as 600 mW and it will take a

finite amount of time for the temperature to stabilize after turn on. Just how long a stabilization period should be allowed depends upon how fast the codes are tested. Tests using an abbreviated test method for measuring linearity are not as sensitive to the thermal shifts as tests using all codes test method. While testing the devices on the S3260/70 in the all codes linearity test mode, the data obtained was very sensitive to stabilization time just as the data would be in a bench test setup. All final test data was taken after a temperature stabilization of 12 minutes.

Bench Test Development

The only bench test characterization performed on the 562 D/A Converter was the measurement of settling time. Figure 7-8 shows the schematic of the settling time test circuit used by GEOS during characterization.

Transistor Q1 is a high frequency grounded base amplifier that clamps the DUT output to ground. Resistor "R" and voltage "V_L" are adjusted for zero current in the Schottky diodes when the DUT output is at its final value. The grounded base amplifier output is connected to one half of a common collector differential amplifier. The other half of the differential amplifier is connected to the supply side of the Schottky diodes. This circuit provides cancellation of any noise variations on the + 5 volt supply output as a result of its inability to regulate with fast switching load changes. The oscilloscope input gain is adjusted when the DUT output is at its final value. To do this, the LSB input to the DUT is toggled (not shown) on Figure 7-8 between a logic "1" and a logic "0". As this is done, the oscilloscope preamp gain is adjusted for a 2 cm vertical change on the oscilloscope. This results in a display which represents 1/2 LSB/cm. Once the test circuit and the oscilloscope have been calibrated for the desired DUT output final value check, a square wave is applied to the DUT digital inputs and settling time is measured on the oscilloscope to ± 1/2 LSB of the final value.

Tester Correlation

Correlation of test adapter was accomplished by comparing the automatic tester data with bench data in a simple test circuit setup and by comparing these data results with vendor supplied data on the parts to be characterized. All sets of data were eventually shown to be well within the 20% of parameter limit criteria used by GEOS and government test facilities. GEOS was unable to correlate data on device settling

time. GEOS received, on loan, the settling time test box from one of the manufacturers supplying parts for characterization. Devices were tested at GEOS on this test box and the results were compared with those obtained using the circuit shown in Figure 7-8. The settling time test results obtained with the GEOS test circuit were about 1-1.5 us faster than those obtained with the vendors test circuit. The vendor was contacted concerning this problem, however, he feels that the AD562 meets the needs of a general purpose D/A Converter and that his tests is adequate for these needs.

7.4 Test Results and Data

Most of the static test parameter measurements were straight forward and the data results were within the specified parameter limits. Four devices marginally failed the gain error drift over the temperature range of -55°C to +125°C and six others marginally passed the limit. If the gain error drift is calculated over the temperature range of -55°C to + 125°C, the four above mentioned failures pass the spec limit. Examples of the test data results are presented in Tables 7-4 and 7-5.

Bit linearity error testing was done both by measuring all codes data and by measuring the individually activated bits one at a time with all other bits turned off. The data for errors to the individual bits was reasonably consistant whether it was obtained by a quick abbreviated test measurement or whether it was extracted from the all codes measurement. The correlation between these two measurement techniques is illustrated in Figure 7-9. The all codes bit linearity errors were measured at 125°C, 25°C and -55°C for positive power supply voltages of +5 Vdc and +15 Vdc. The errors were graphed versus address code and sample graphs are presented in Figure 7-10 and 7-11. In addition, sample histograms of the bit linearity error distribution are shown in Figure 7-12 and 7-13.

Bench test data was obtained on the settling time parameter for both device type 01 and 02. Output Settling Time Data for device types 01 and 02 is presented in Table 7-6. Sample oscillographs of the settling times are presented in Figure 7-14 and 7-15 for device types 01 and 02, respectively. In addition, settling time data was obtained using both the GEOS test circuit shown in Figure 7-8 and the ADI test circuit shown in Figure 7-17. The AD settling time test adapter was loaned to GEOS for this characterization.

7.5 Discussion of Data

Static data was measured on the S3260/70 at -55°C, 25°C and 125°C. Samples of the 25°C measurements are presented in Tables 7-4 and 7-5 and in Figures 7-9 through 7-13.

All of the devices supplied for device type 01 characterization met the 25°C parameter limits. However, some devices supplied for device type 02 characterization failed a) the bipolar offset error (BPOE) and/or b) the sum of the positive and negative bit errors (Σ (NL+) + (NL-)). A vendor analysis of the circuit revealed that the bipolar offset error limits were initially set too tight for the device design. The limit for bipolar offset error was subsequently set to ± 40 mV for both device types. With this, all of the devices for characterizations met the bipolar offset error limits at all three temperatures. Failure of the limits for the sum of the positive and negative bit errors disclosed that the parts had a bow in the bit linearity error curve. This is illustrated markedly in Figure 7-11 and 7-13 for Bit Linearity Error and Bit Linearity Error Distribution, respectively. Both of these figures illustrated that, if the bit linearity error curve described a bow, the sum of the positive and negative bit errors parameter, most generally, would not be met. Since the bow caused the device to fail the sum of the positive and negative bit errors parameter but did not, in itself, cause the device to fail bit linearity error, it was felt that the parameter for the sum of the positive and negative bit errors was too severe and unnecessary. The test was therefore deleted from the slash sheet.

Testing of these devices at 125°C did not uncover any additional failures and/or test problems. However, testing at -55°C uncovered both. Analysis of the data taken at -55°C revealed several failures for the digital input current measurements. These failures occurred randomly and could not be repeated. After a great deal of investigation, it was discovered that the velocity of the cooling air to the DUT in the tester had been increased for some unrelated testing but was not set back to its initial value. This meant that the cooling air spent less time in the tester's drying chamber; and consequently, the moisture content of the air was higher than normal. This condition resulted in the formation of frost at the DUT pins and random digital input current failures. Once the tester problem was corrected the random failures were eliminated. GEOS did not retest devices that failed before the tester problem was corrected.

At -55°C, failures were also observed during the measurements of bit weight errors, sum of the positive bit errors and sum of the negative bit errors. The bit weight error measurements were rescheduled with no change in the results. The failures are, therefore, assumed by GEOS to be actual failures.

Possibly the most singularly revealing printouts of the bit linearity error measurements are shown in Figures 7-10 through 7-13. Figures 7-10 and 7-11 are plots of the 4096 bits of linearity error data. Because of the large number of data measurements and the linearity resolution of the computer graphics, the bit linearity error graph, for all 4096 bits, had to be printed on six pages. The two figures show significantly different patterns. The two devices used to obtain these plots were from each of the two different vendors that supplied parts for characterization. Because of the characteristic differences between these two devices, it became apparent that the originally proposed abbreviated test method using the superposition of individual bit errors, would not adequately guarantee device performance. When this test method was applied to devices with bit linearity error characteristics as shown in Figure 7-11, the most positive error could not be defined. After several such observations, the test method was abandoned.

Other abbreviated test methods described in Section 7.3 were analyzed by using the all codes data. A successive approximation technique was analyzed to obtain the maximum positive error by first checking the bit linearity error for code 1000 0000 0000. If this yields a positive bit linearity error then the bit linearity error for the code word 1100 0000 0000 is checked. However, if the initial code word yields a negative bit linearity error, then the next check for bit linearity error is made at code word 0100 0000 0000. This process of decision making continues until all bits have been examined. It is hoped that the final value represents the most positive bit linearity error. The results, however, had the same failings as the single bit superposition method when the bit linearity error curve displays a bow. This method was also abandoned.

The most promising technique involved a method of segmentation, whereby, the 4096 code words were divided into 16 equal increments and the worst case error, as defined by these 16 code words, was defined. Since these code words are established by combinations of the first 4 most significant bits, a method for determining the state of the remaining 8 bits had to be defined. After observing the repetitive nature of the first 128 bits of linearity error data, GEOS concluded that either the single bit superposition method or the successive approximation

technique could be used to determine the state of the lower 8 bits. Since the single bit superposition method for finding the worse case error is the simpler of the two to implement, GEOS recommended this method combined with the 16-segment method for determining the overall worse case bit linearity error.

The technique described above has given good results in defining the worse case error, however, since the D/A Converter bit linearity error is repetitive for the lower bits there may be several code words that yield approximately the same maximum error. This is particularly true if the bit weight error of bit number five is zero. Under these circumstances, the error pattern is repeated twice in each of the 16 segments. Therefore, there will be two code word in each segment, separated by 128 bits, that will yield approximately the same bit linearity error. Table 7-7 compares the results of the worse case bit linearity error measurements obtained by a) the single bit superposition method, b) the 16 segment plus single bit superposition method and c) the all-codes method. Examination of this table shows that the 16 segment and the all codes method have a maximum positive error difference of .024 LSB and a maximum negative error difference of .030 LSB. Also, the superposition method and the all codes method have a maximum positive error difference of .202 LSB and a maximum negative error difference of .396 LSB.

Settling time of the device output current was measured as the digital inputs are changed from all bits on to all bits off and vice versa. Test results are tabulated in Table 7-6 and sample oscillographs of settling time for device types 01 and 02 are shown in Figures 7-14 and 7-15 respectively. These test results were compared with typical results obtained from both vendors. GEOS was not able to correlate settling times with those typically observed by ADI. To assist in the investigation, ADI loaned their production tester to GEOS. Data was taken on both the GEOS settling time tester and on the ADI settling time tester. The results of these measurements are shown in Figure 7-16 and are consistent with results predicted earlier.

7.6 Slash Sheet Development

The slash sheet, MIL-M-38510/121, was developed as a joint effort of GEOS and the cognizant members of the JC-41 Committee. Most of the test parameters were established early in the slash sheet development, however, bit linearity error test methods were significantly changed from the initial draft and noise and reference input impedance were added later.

Initally, the slash sheet was supposed to specify devices from three different vendors, except that, during the characterization effort a design problem was uncovered with the PMI submission and they chose to withdraw their parts until the design problem is cleared up. In place of this part, a 563 D/A Converter was added to the slash sheet. This part is identical with the 562 D/A Converter except that the 563 has an internal reference voltage. Since the internal reference voltage source contributes to the error measurements, several of the test parameter limits had to be relaxed. Table I of the slash sheet is shown in Table 7-8.

Definitions were included in the slash sheet and at the time of this writing were still being discussed.

7.7 Conclusions and Recommendations

The test circuits were developed for use on an automatic test set. The test adapter was designed to test all of the parameters listed in Table 7-8, except for settling time, noise and reference input impedance. In retrospect, it would be much better to devote one test adapter circuit to the standard type test parameters and to develop a separate test adapter test circuit for the unique test parameters such as bit linearity error.

The abbreviated test for the measurement of bit linearity error is adequate for the measurement of 562 D/A Converters from both Analog Devices and Harris. Should a new vendor request qualification for the production of these devices, a full characterization of the new vendors parts should be made to determine if the abbreviated test method is adequate.

Definitions of the D/A Converter terms used in MIL-M-38510/121 are still being discussed by the vendors. GEOS recommends that these definitions be issued by DESC for distribution and comment and that a Data Converter Sub-committee should resolve the comments received by DESC. Also, the definitions should reflect the specific devices on the slash sheet and should not be written as general data converter definitions.

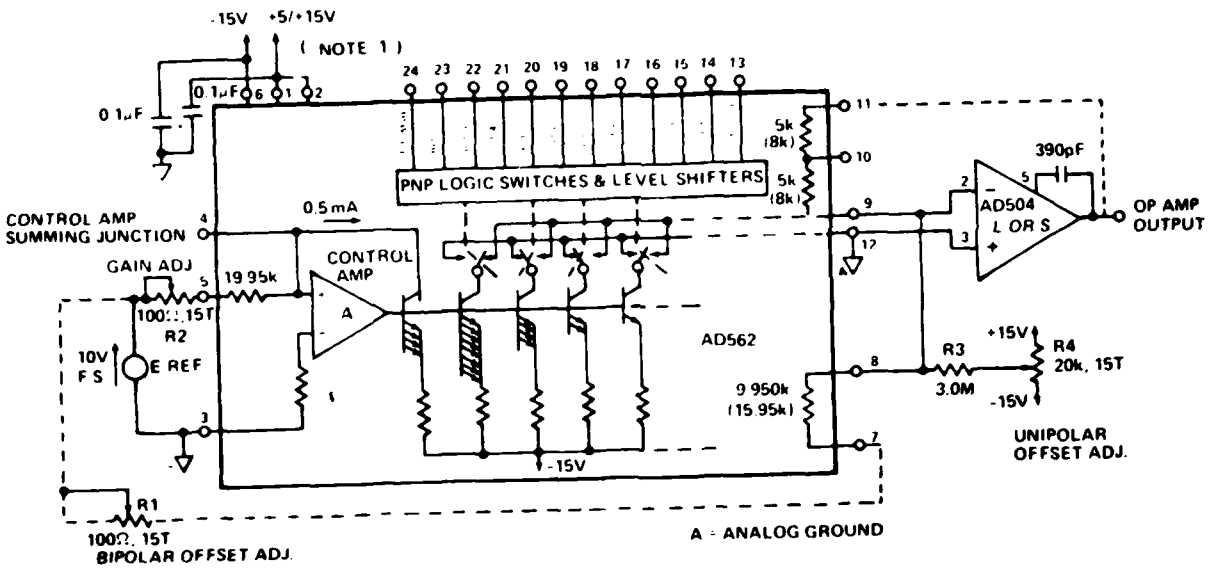


Figure 7-1. Block Diagram of AD562 D/A Converter.

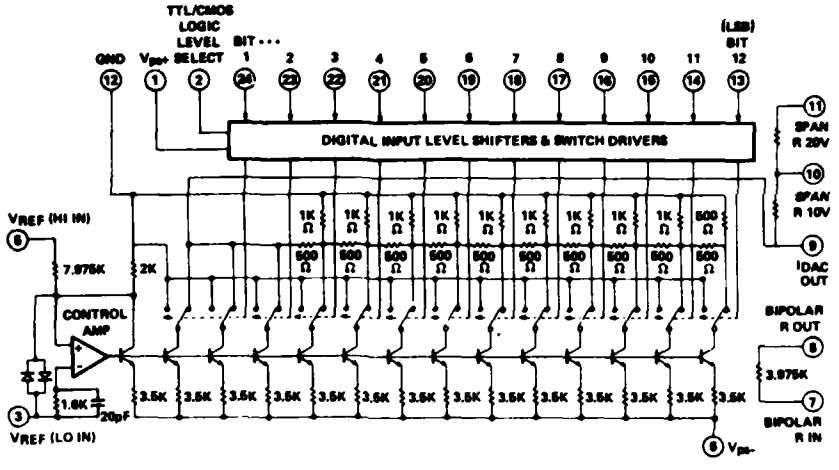


Figure 7-2. Block Diagram of HI-562.

HI-562 Connection Chart

ANALOG OUTPUT MODE	OUTPUT RANGE	ACTUAL FULL SCALE	CONNECTIONS PIN 8 TO	PIN 10 TO	PIN 11 TO	RB BIAS RESISTORS
UNIPOLAR						
BIPOLAR						

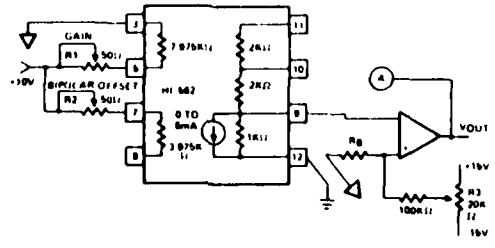


Figure 7-3. Operational Diagram of HI-562.

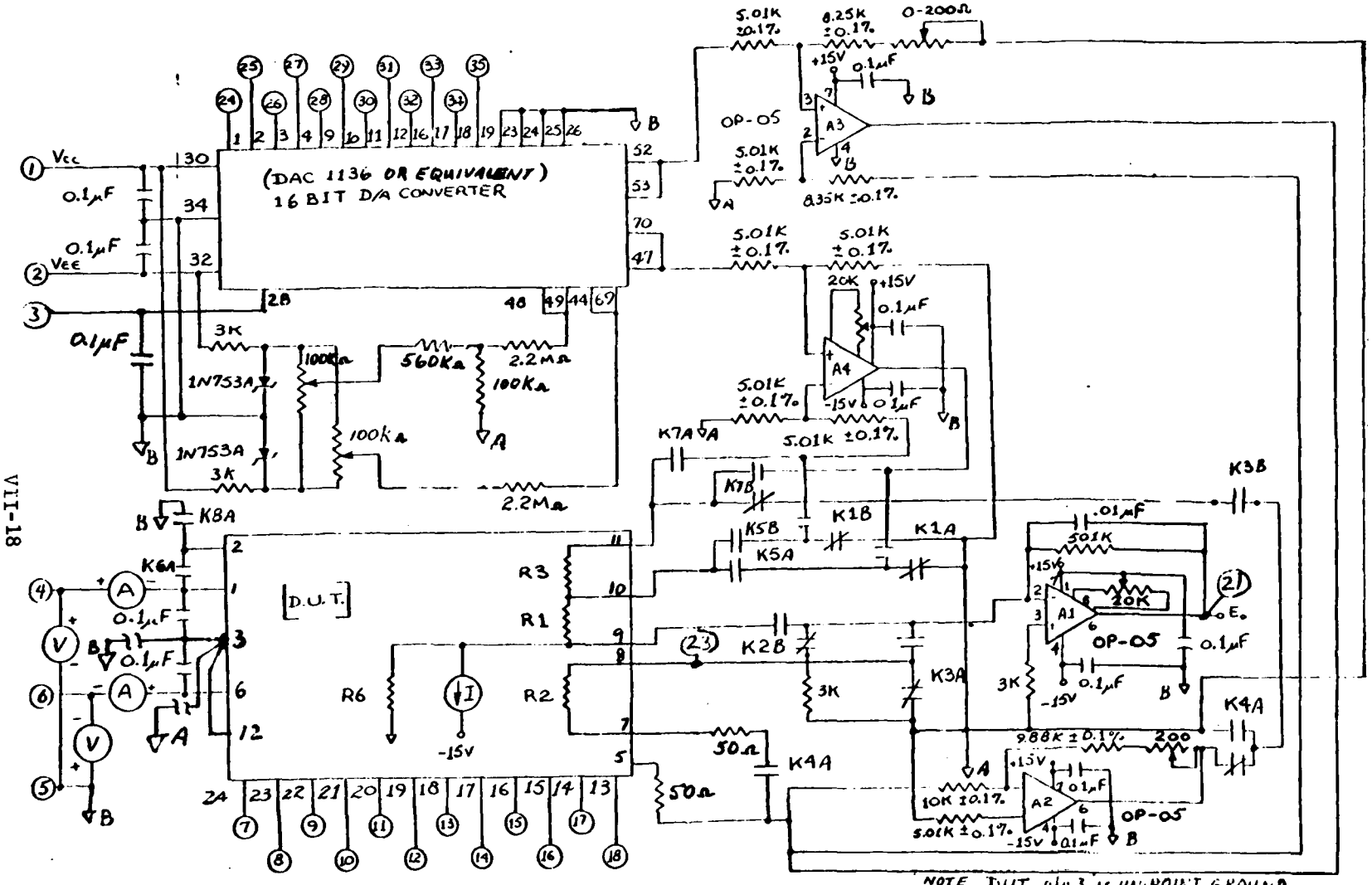


Figure 7-4. Test Adapter Test Circuit for Static Test Measurement.

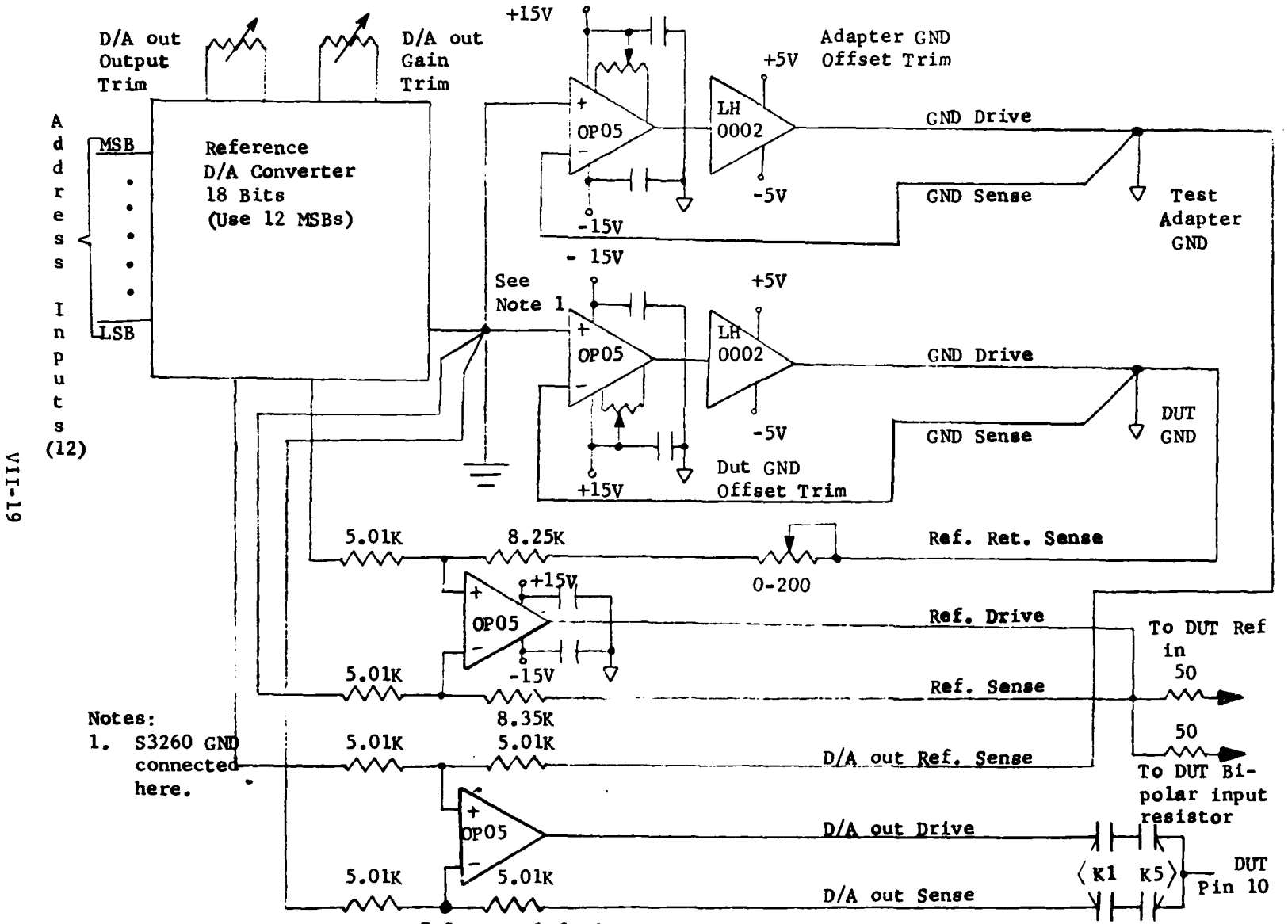


Figure 7.5. Simplified Interconnect Schematic.

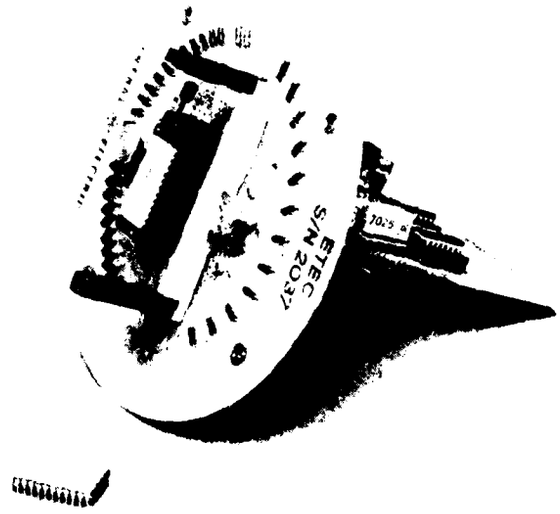


Figure 7-6. S3260 test adapter for the 562, D/A Converter.

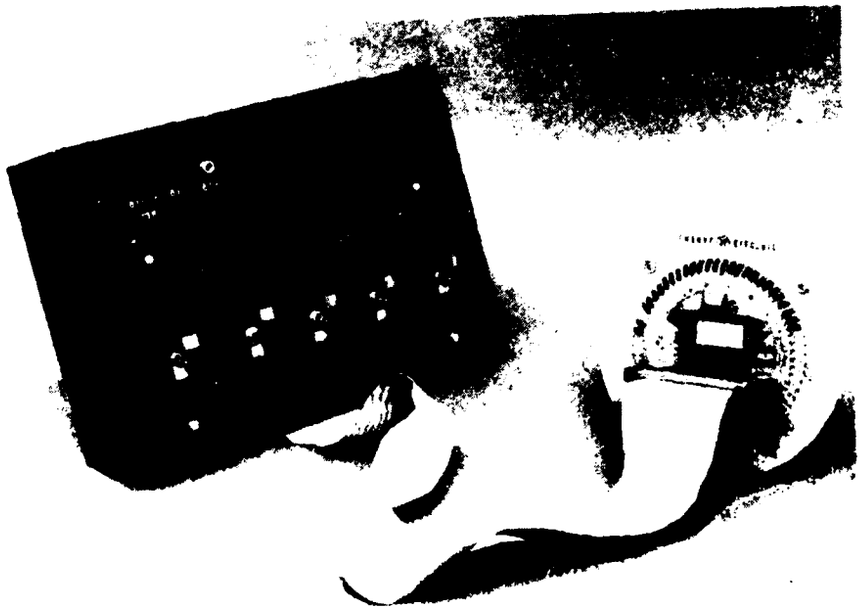
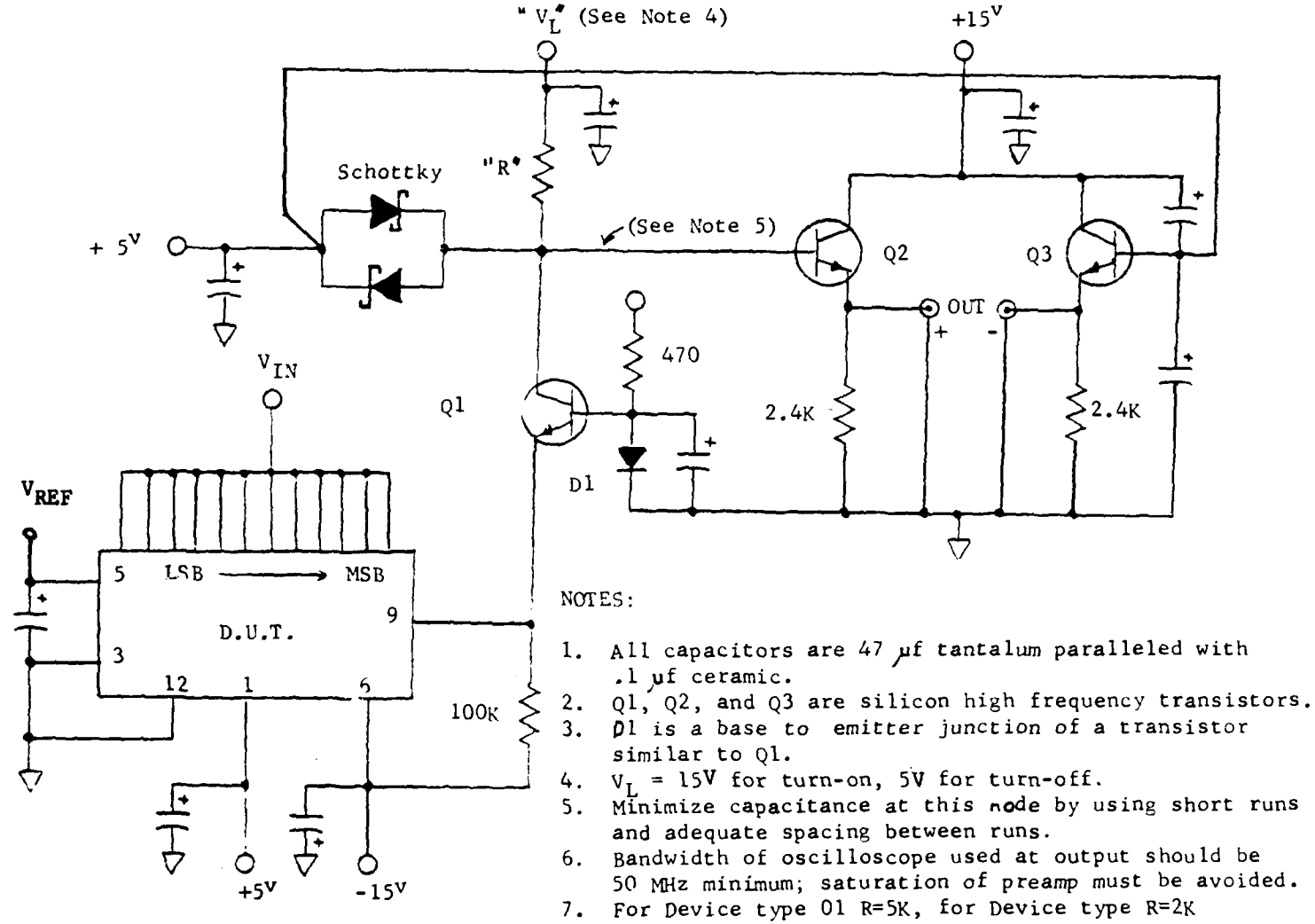


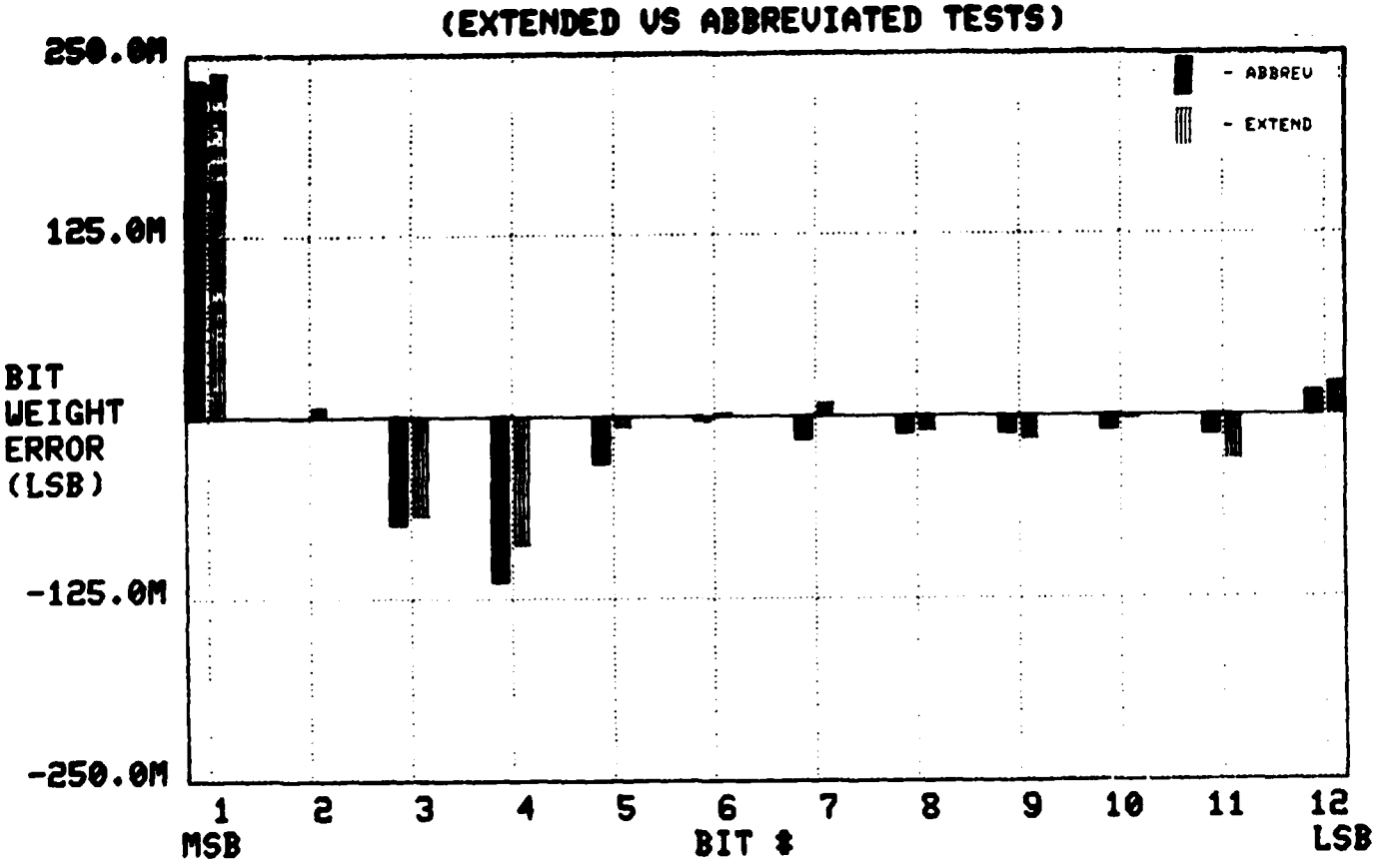
Figure 7-7. Reference module connected to the S3260 test adapter.



NOTES:

1. All capacitors are 47 μf tantalum paralleled with .1 μf ceramic.
2. Q1, Q2, and Q3 are silicon high frequency transistors.
3. D1 is a base to emitter junction of a transistor similar to Q1.
4. V_L = 15V for turn-on, 5V for turn-off.
5. Minimize capacitance at this node by using short runs and adequate spacing between runs.
6. Bandwidth of oscilloscope used at output should be 50 MHz minimum; saturation of preamp must be avoided.
7. For Device type 01 R=5K, for Device type R=2K

Figure 7-8. Test Circuit for Settling Time Device Types 01 and 02.



ABBREVIATED TEST

WORST CASE BIT ERROR (+)= 800.0MLSB @ 100000000011

WORST CASE BIT ERROR (-)= -868.0MLSB @ 011111111100

SUM-WORST CASE BIT ERRORS= -68.01MLSB

EXTENDED TEST

WORST CASE BIT ERROR (+)= 263.7MLSB @ 100001100011

WORST CASE BIT ERROR (-)= -257.2MLSB @ 011111011100

SUM-WORST CASE BIT ERRORS= 6.540MLSB

Figure 7-9. Bit Weight Error Display (25°C).

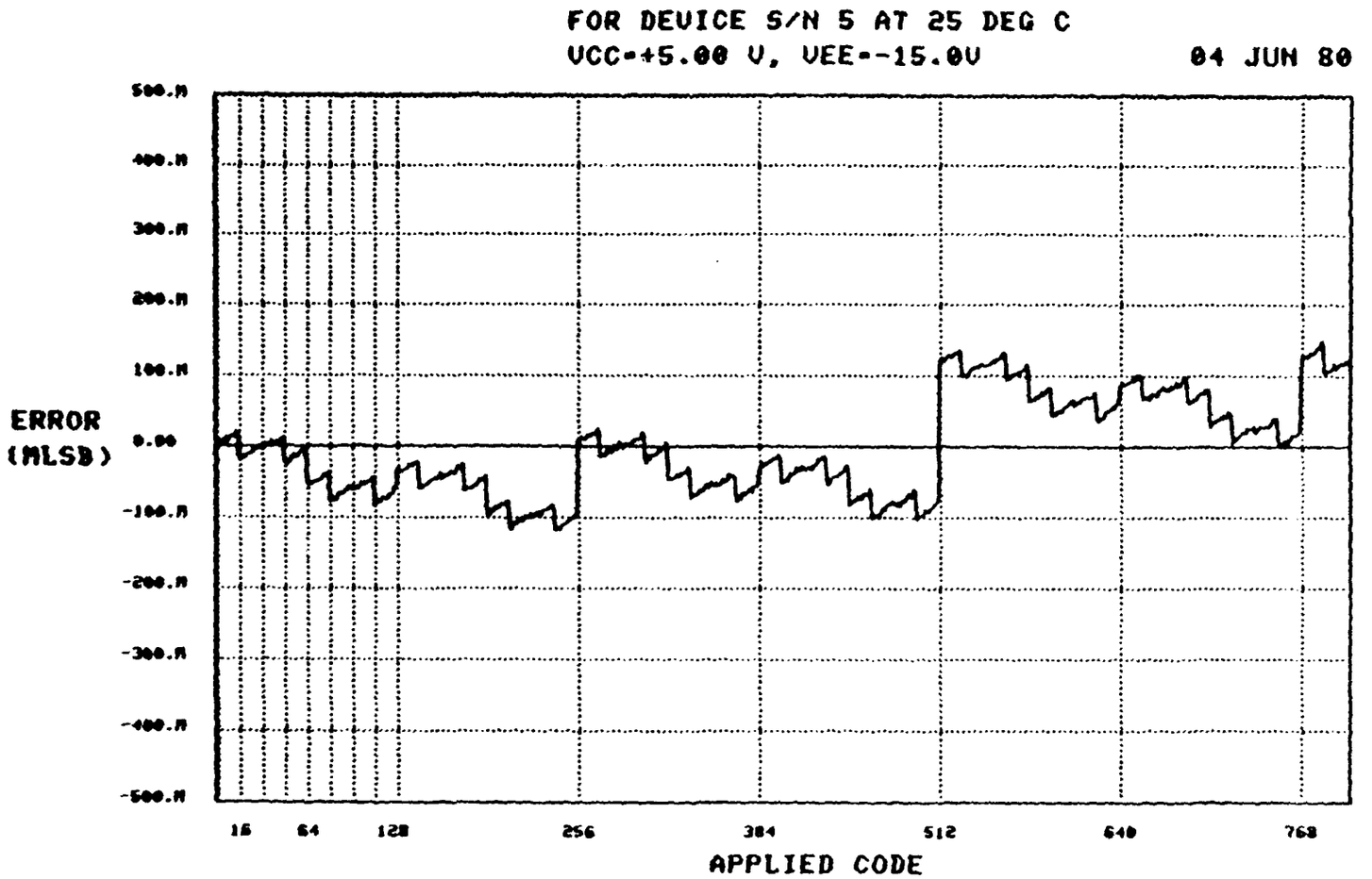


Figure 7-10. Bit Linearity Error (all codes).

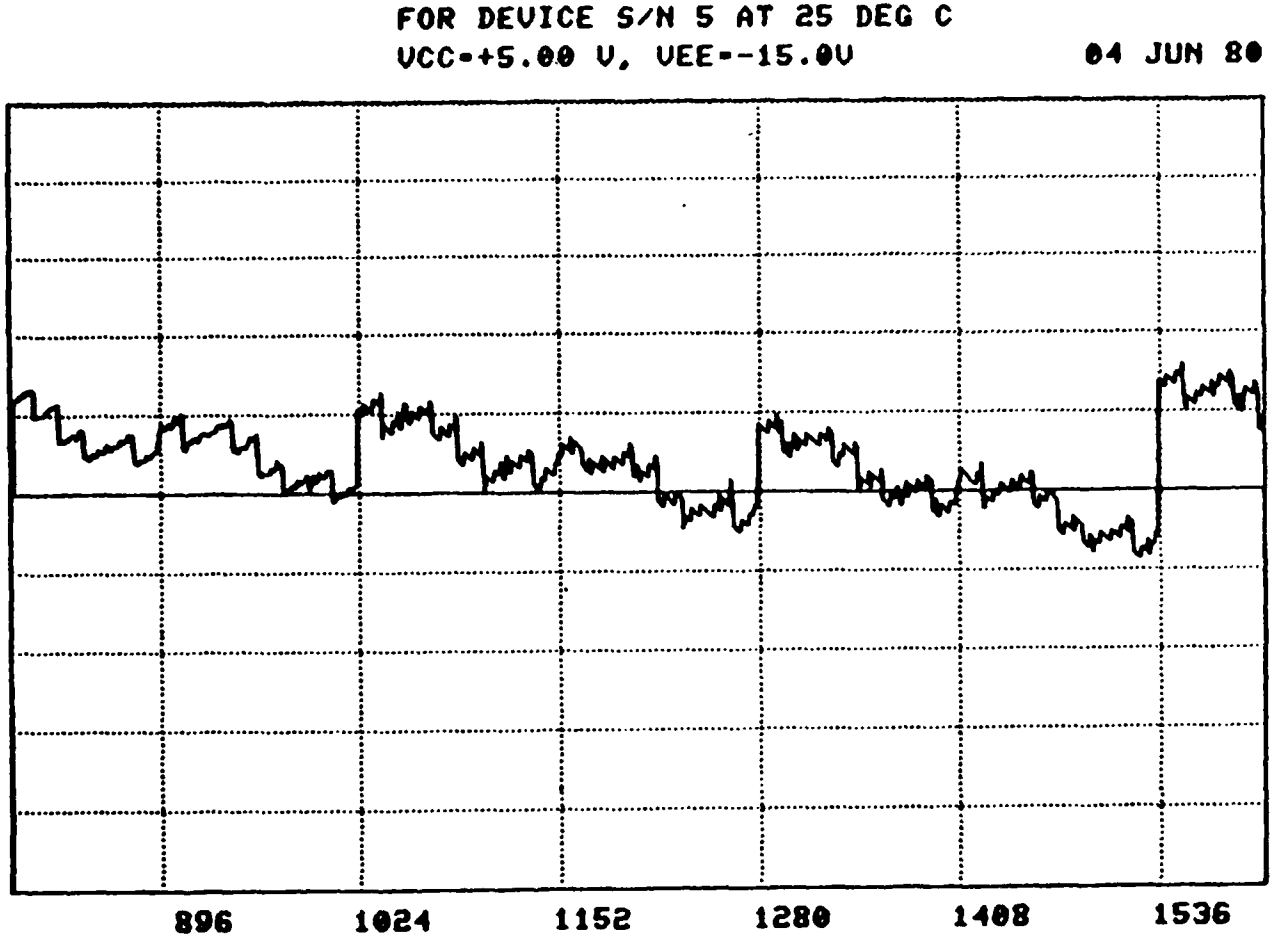


Figure 7-10. Bit Linearity Error (all codes). (cont'd)

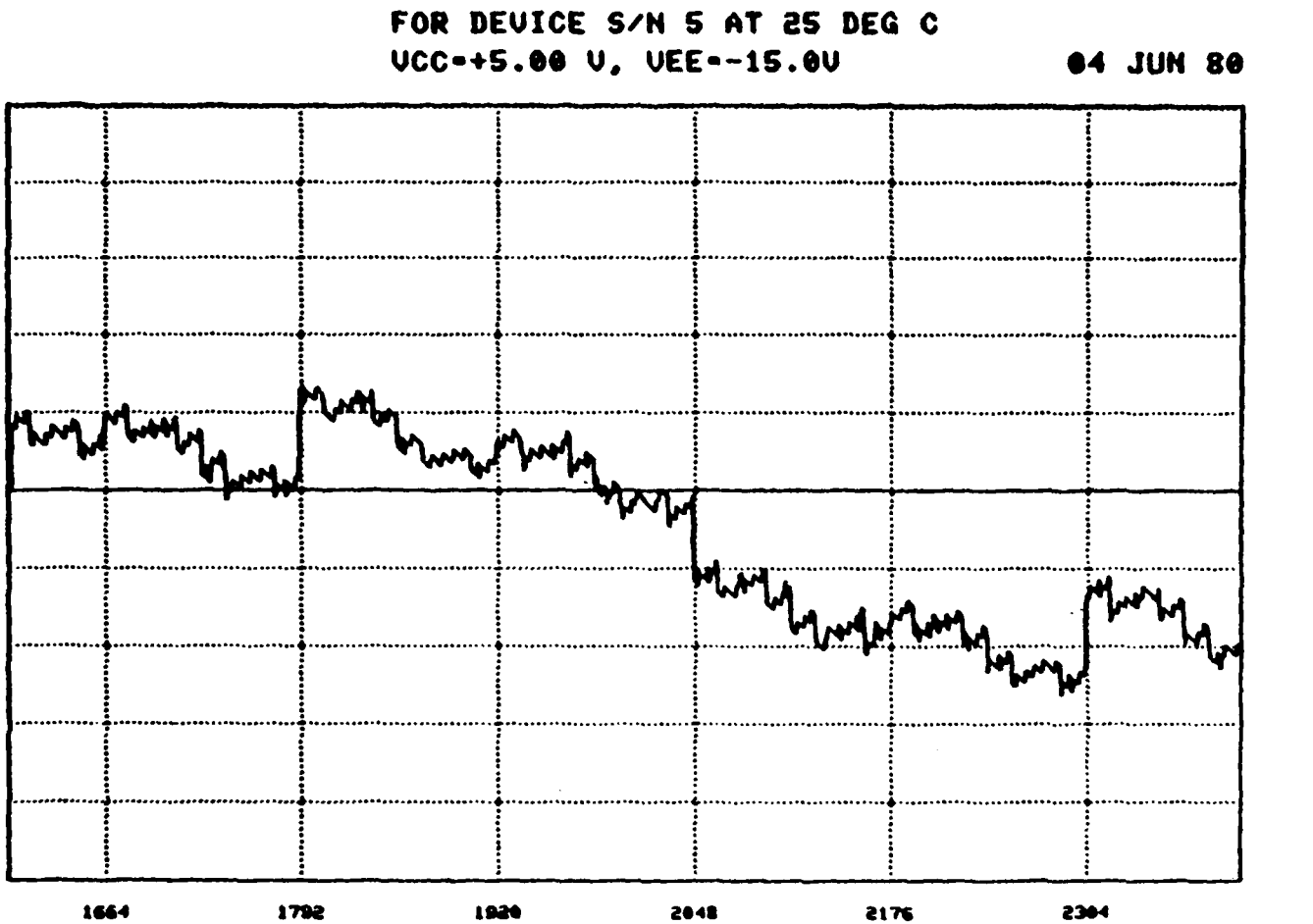


Figure 7-10. Bit Linearity Error (all codes). (Cont'd)

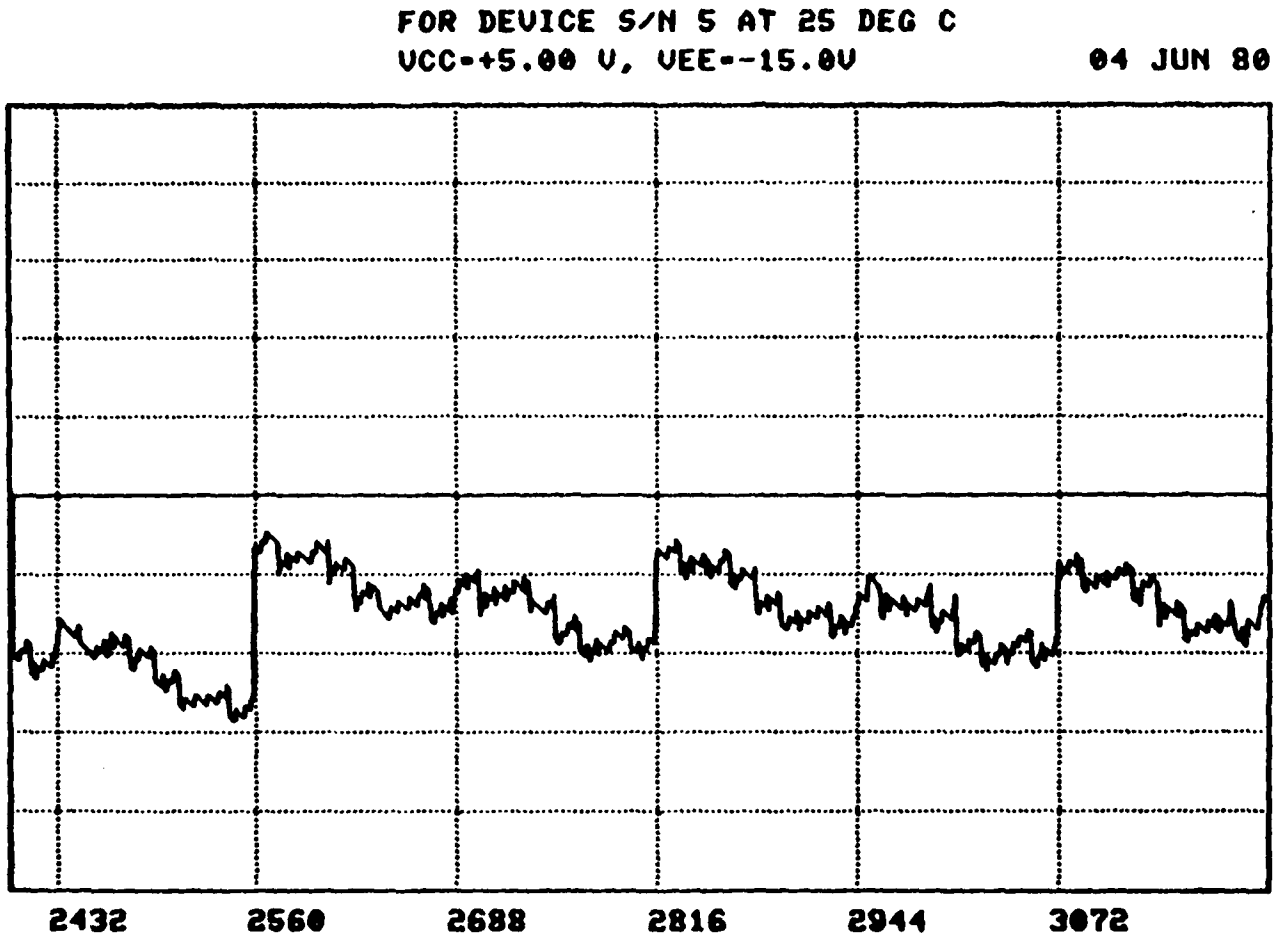


Figure 7-10. Bit Linearity Error (all codes). (cont'd)

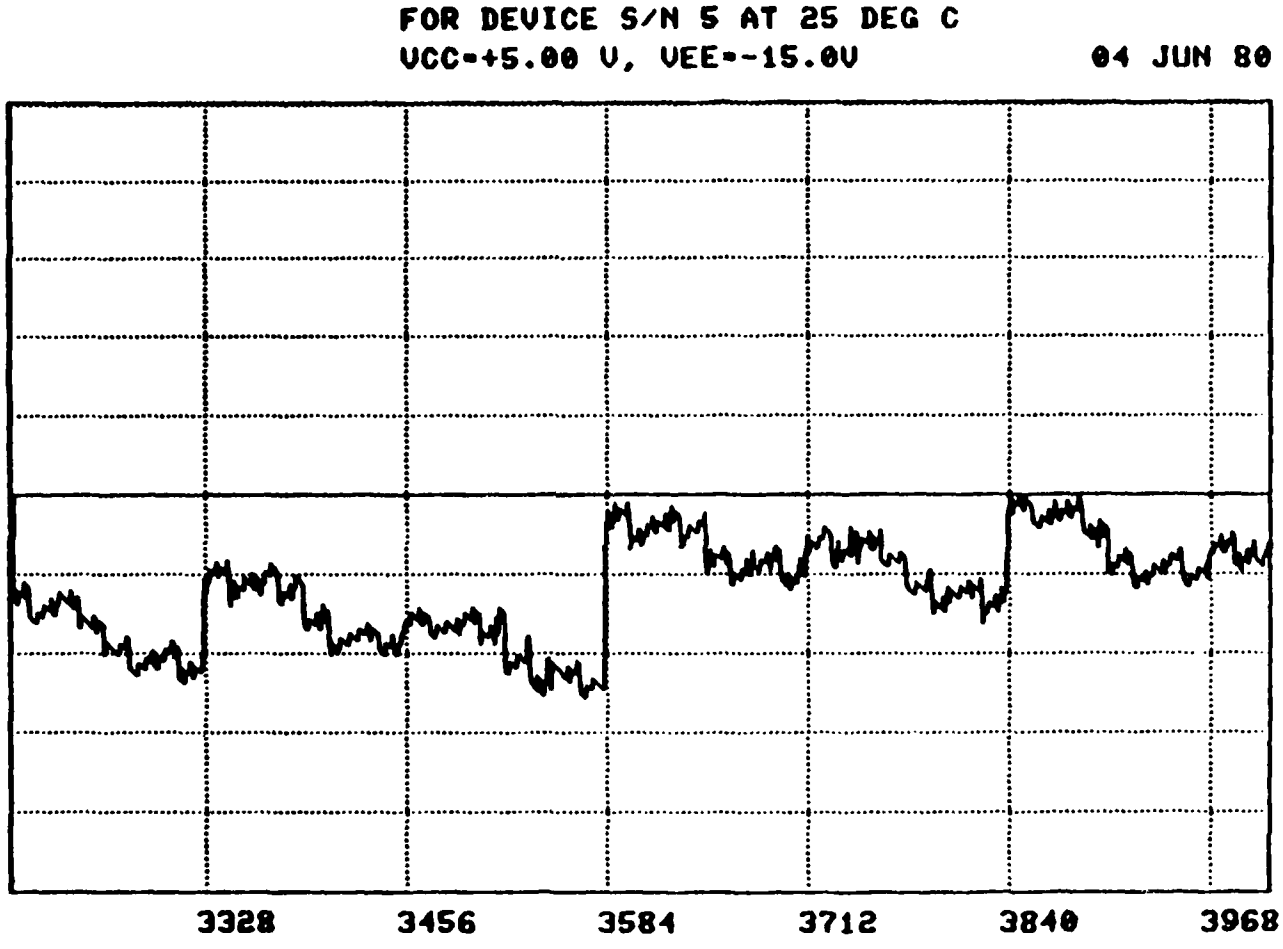


Figure 7-10. Bit Linearity Error (all codes). (cont'd)

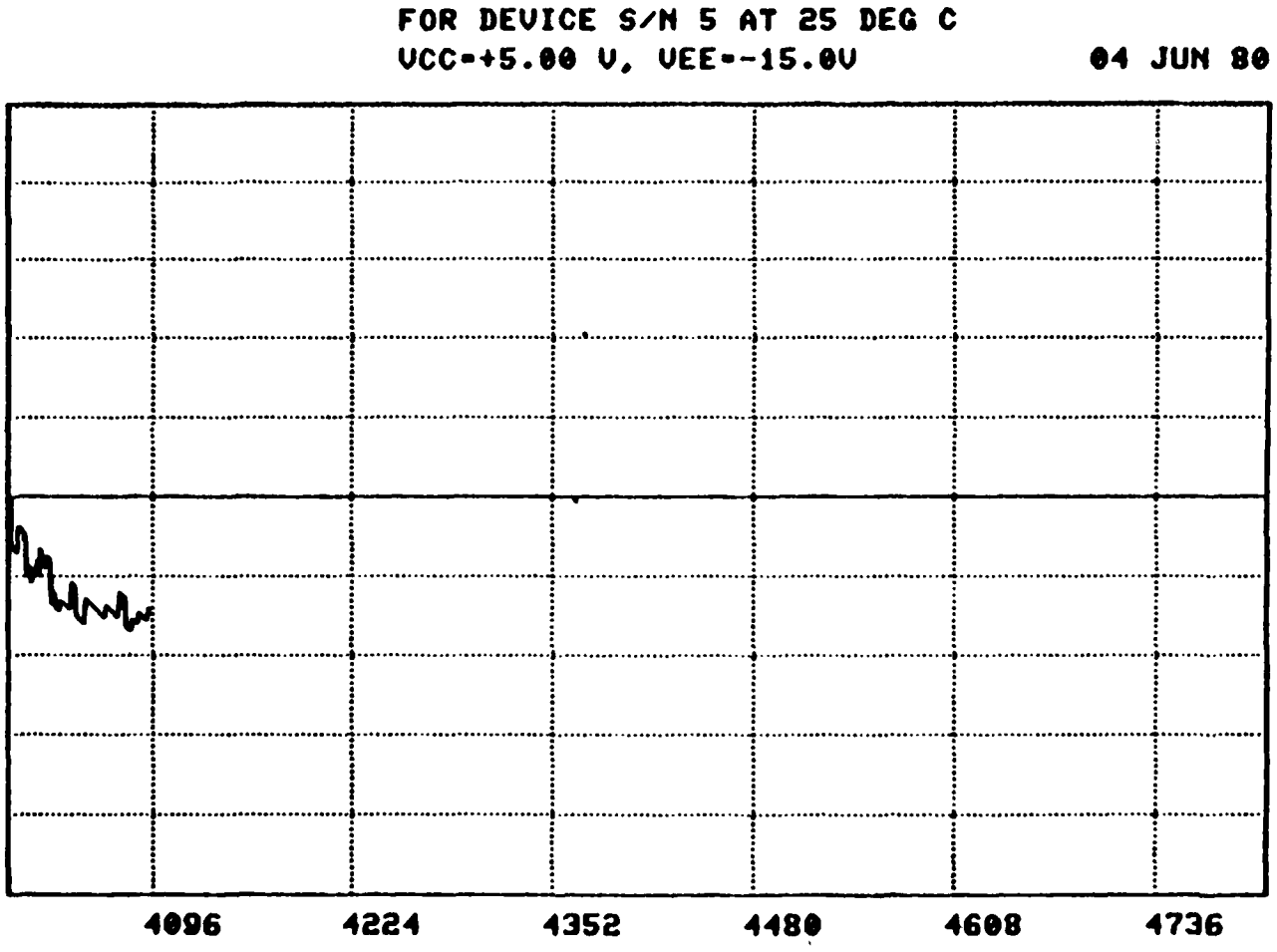


Figure 7-10. Bit Linearity Error (all codes). (cont'd)

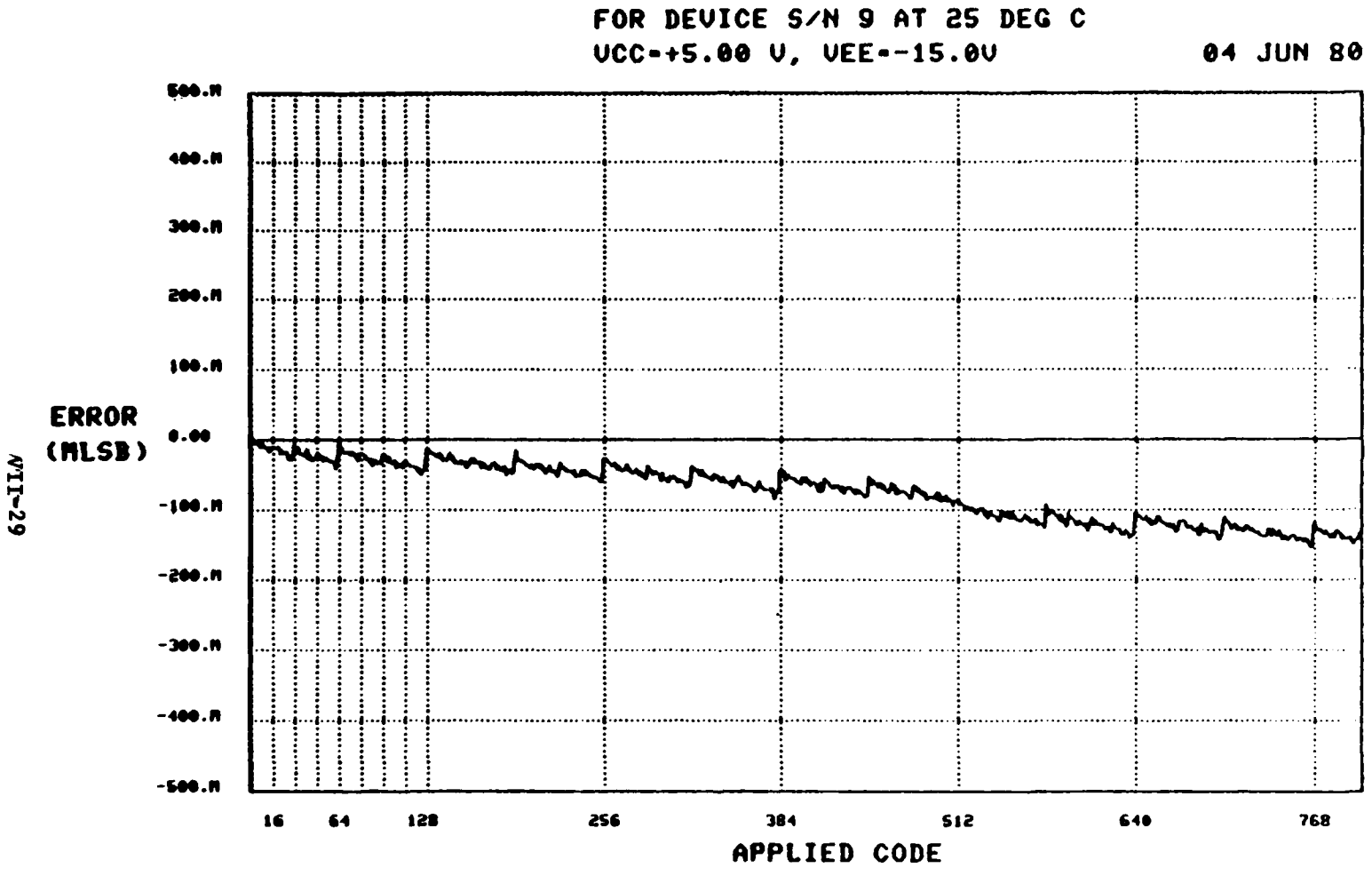


Figure 7-11. Bit Linearity Error (all codes).

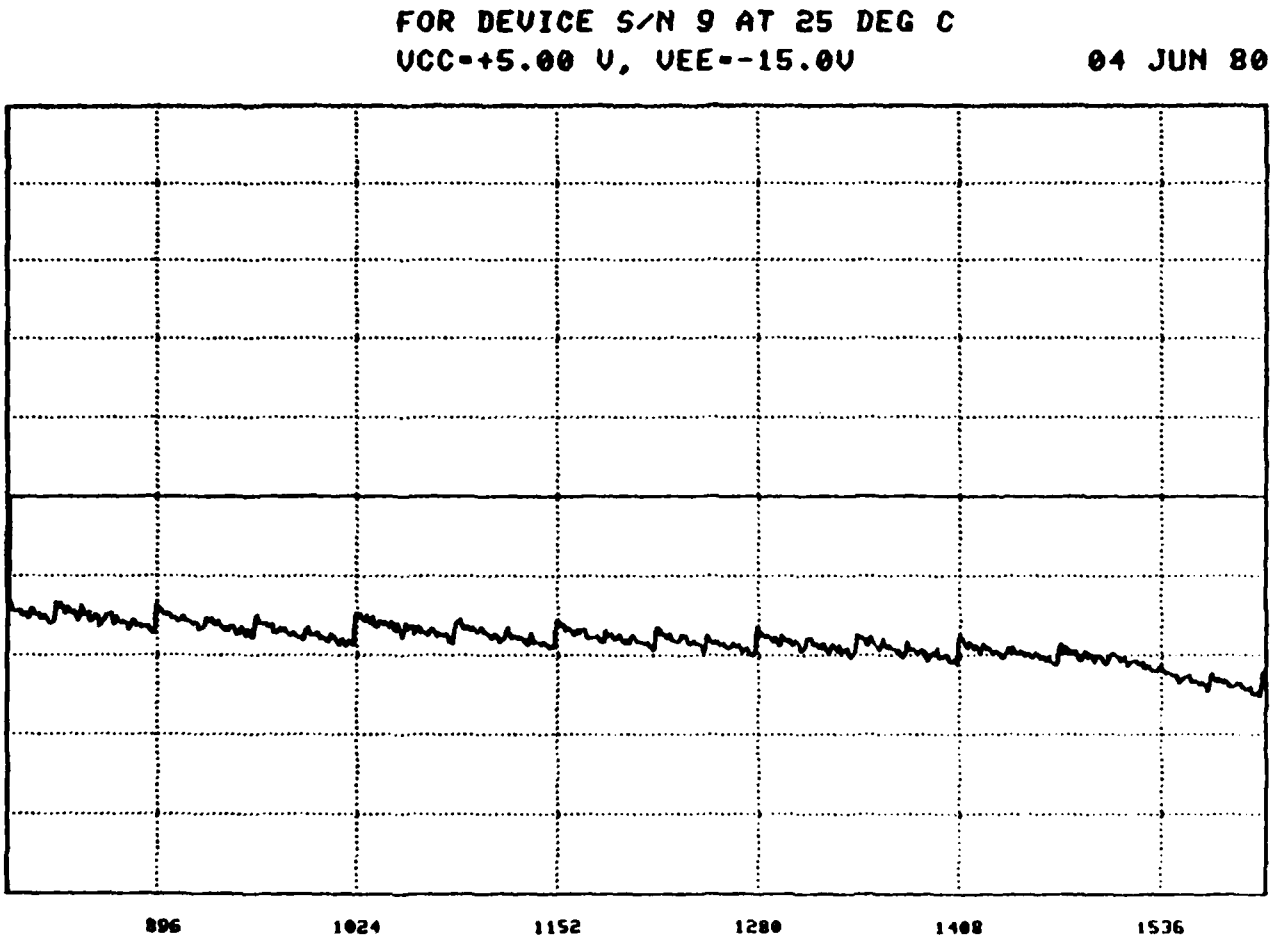


Figure 7-11. Bit Linearity Error (all codes). (cont'd)

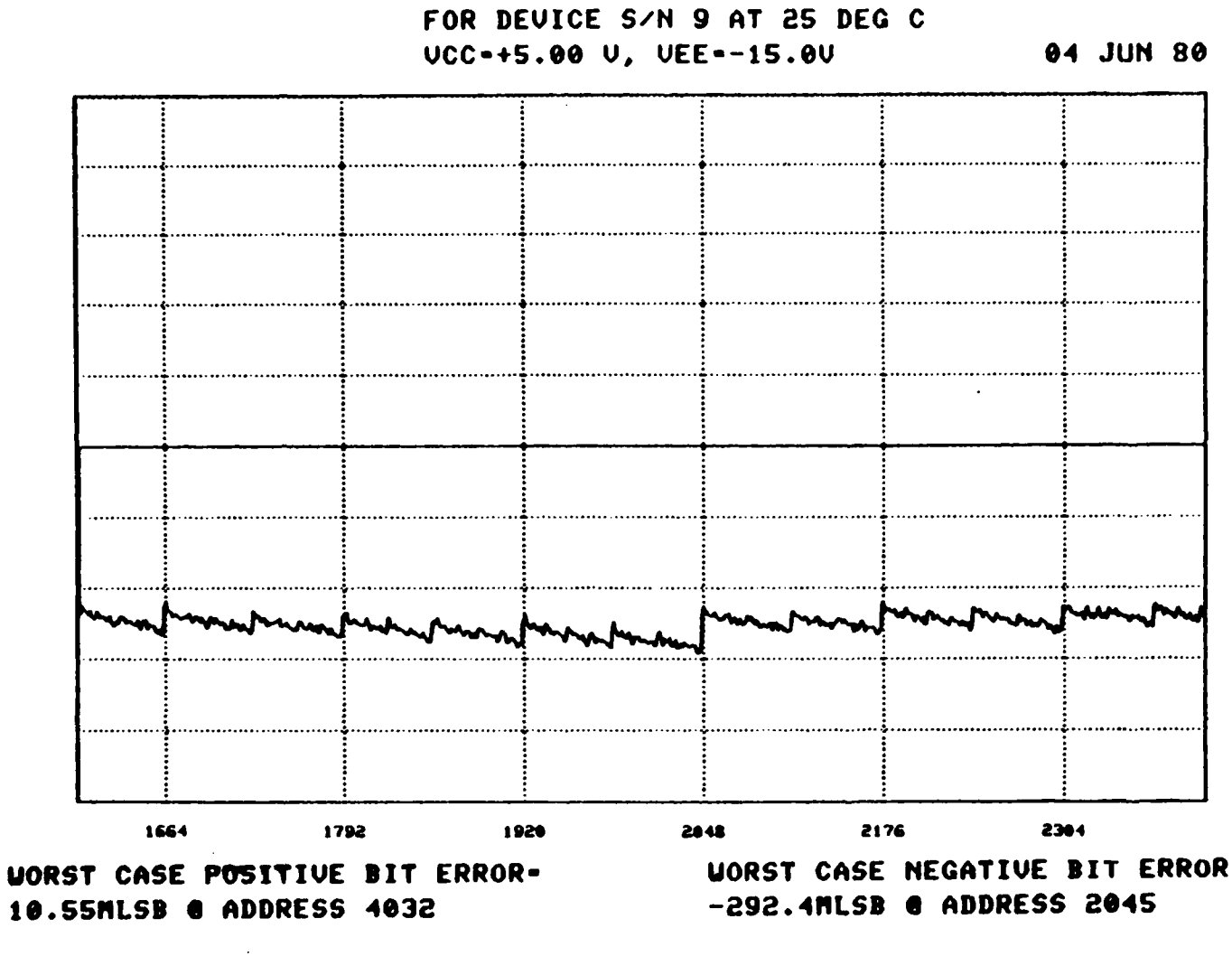


Figure 7-11. Bit Linearity Error (all codes). (cont'd)

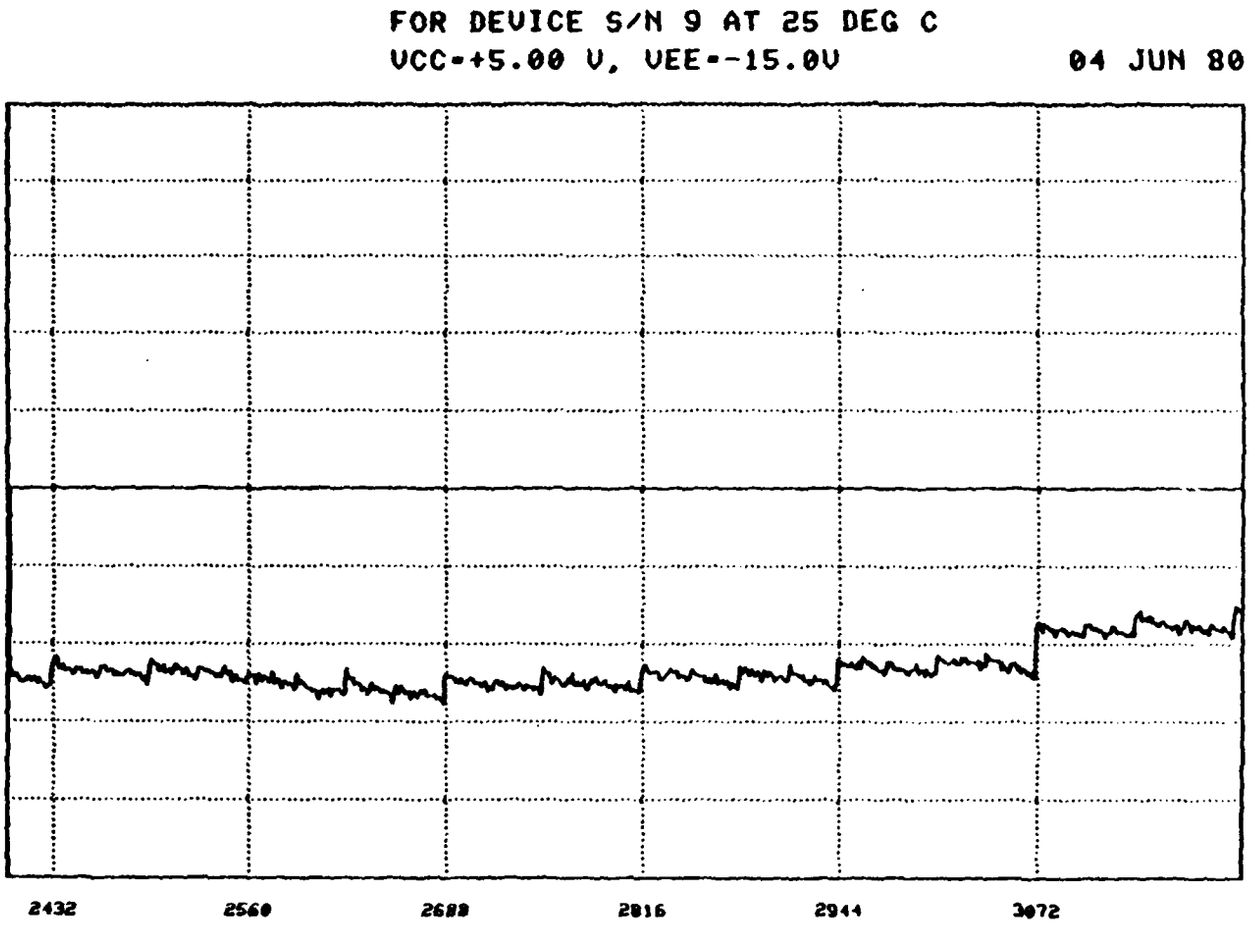


Figure 7-11. Bit Linearity Error (all codes). (cont'd)

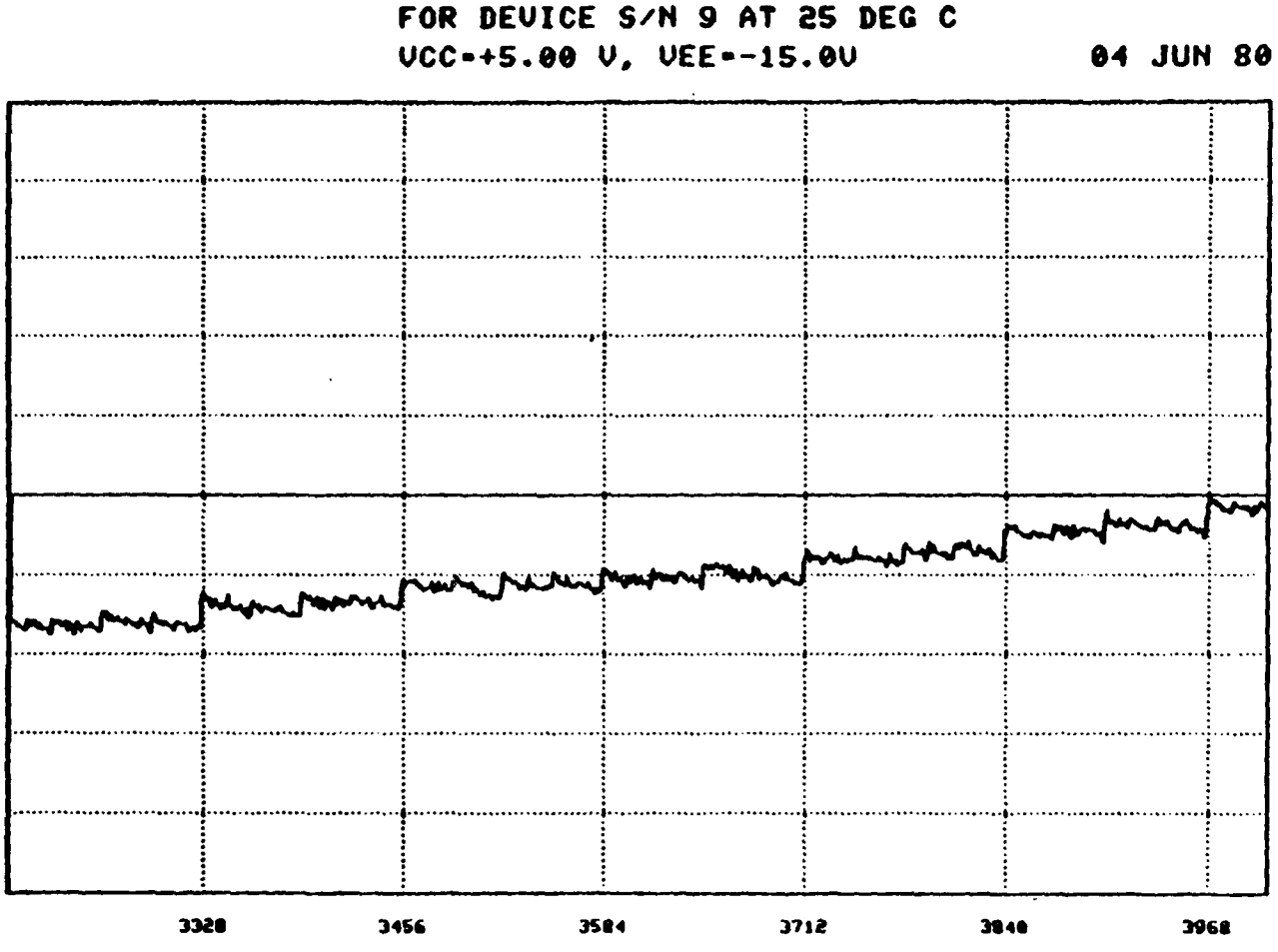


Figure 7-11. Bit Linearity Error (all codes). (cont'd)

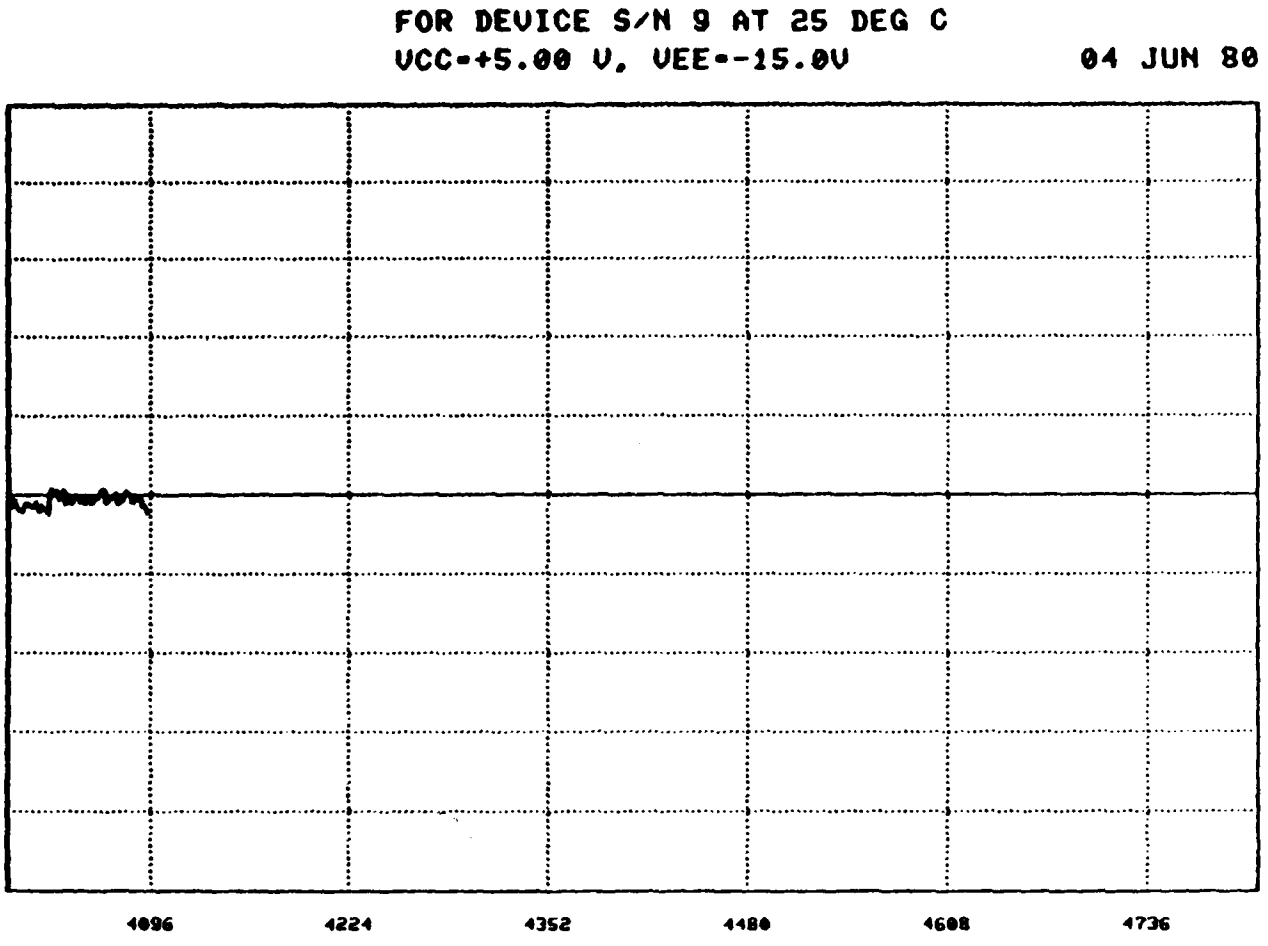


Figure 7-11. Bit Linearity Error (all codes). (cont'd)

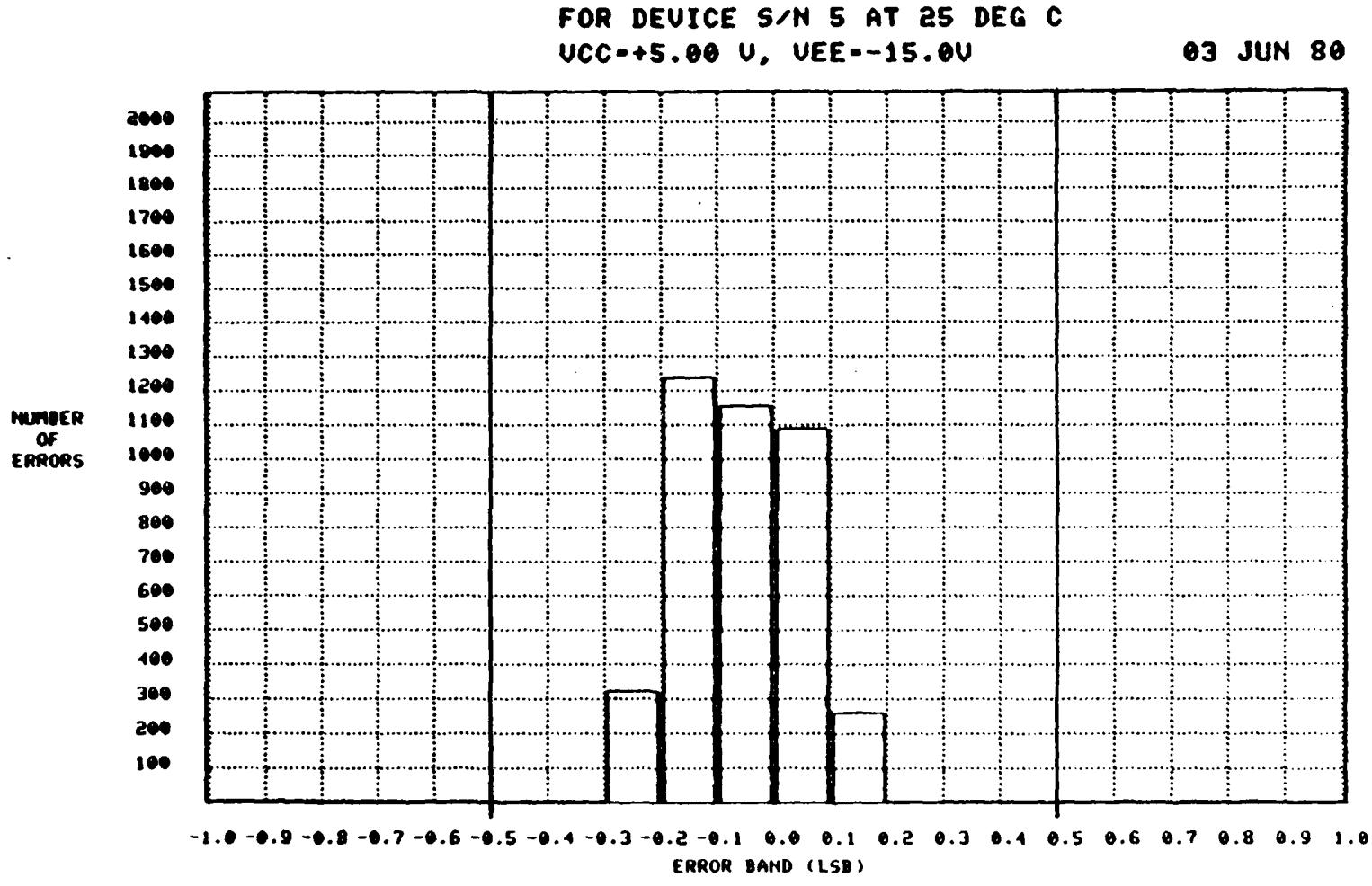


Figure 7-12. Bit Linearity Error Distribution.

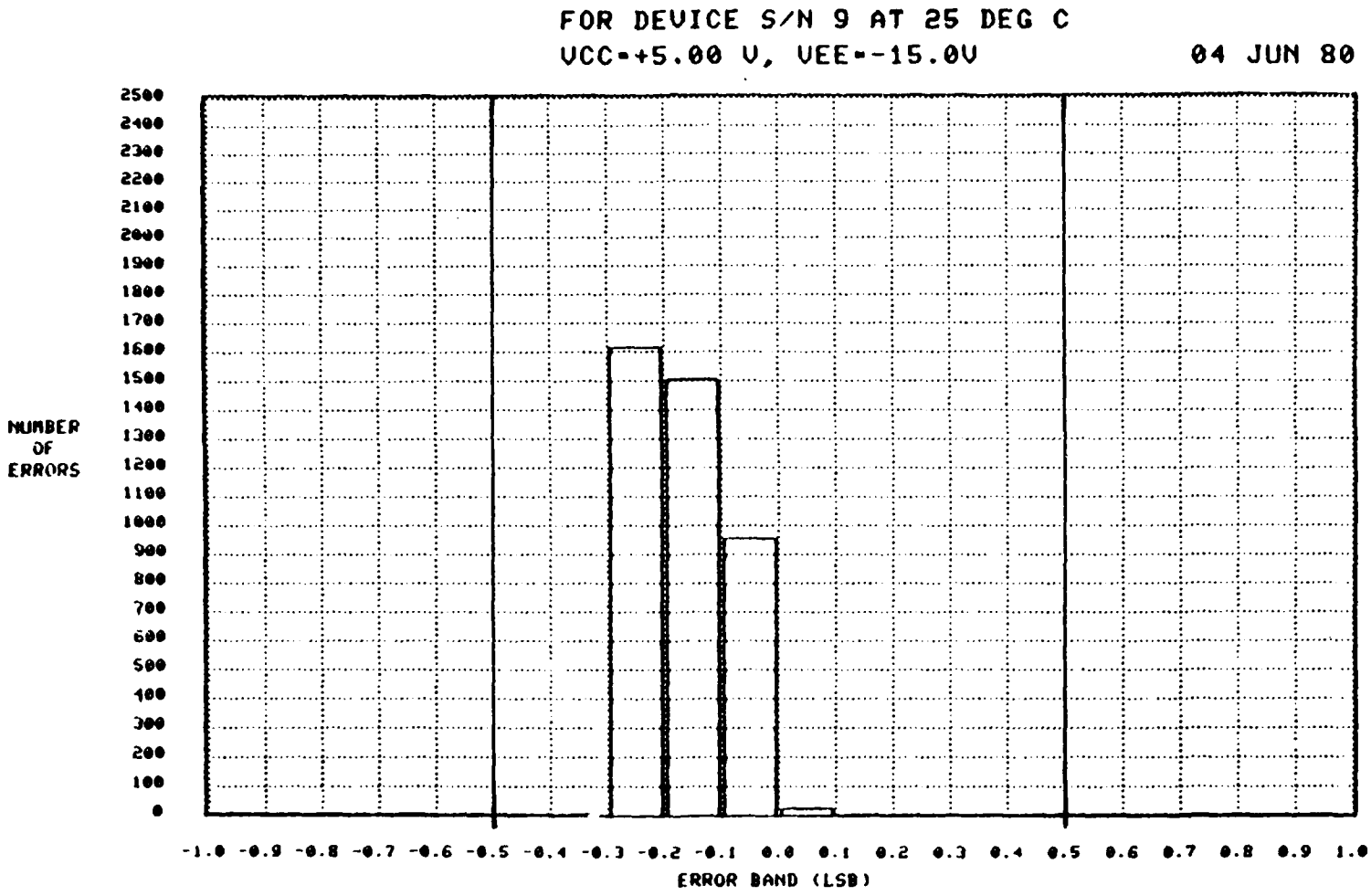
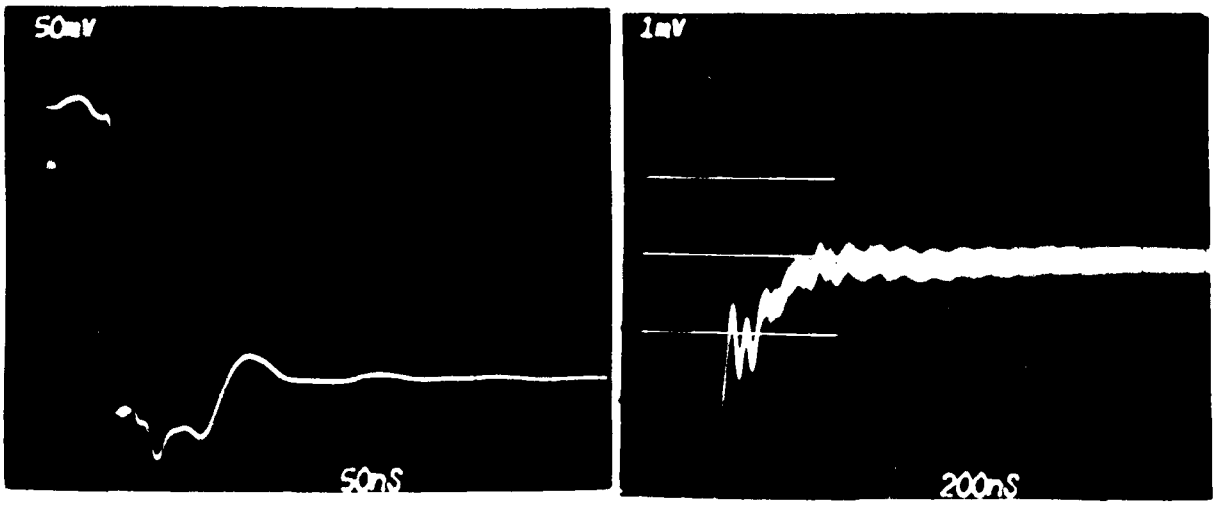
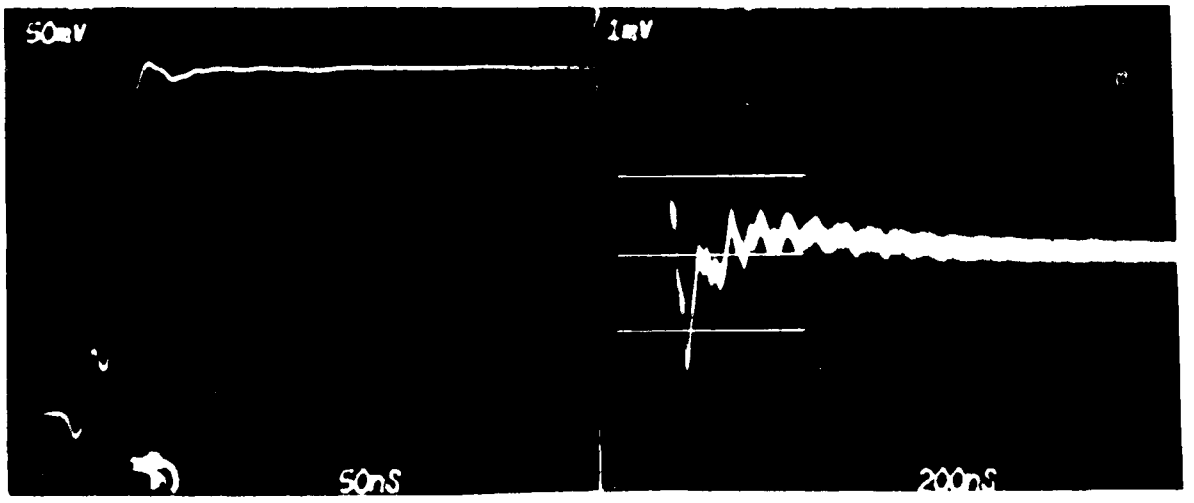


Figure 7-13. Bit Linearity Error Distribution.



0-1 Transition Overall
(a)

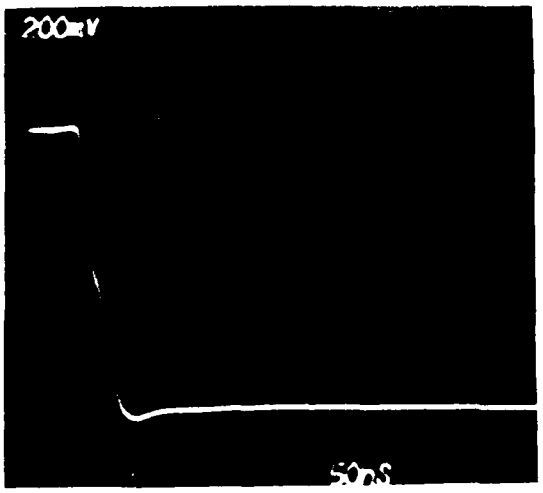
0-1 Transition Expanded
(b)



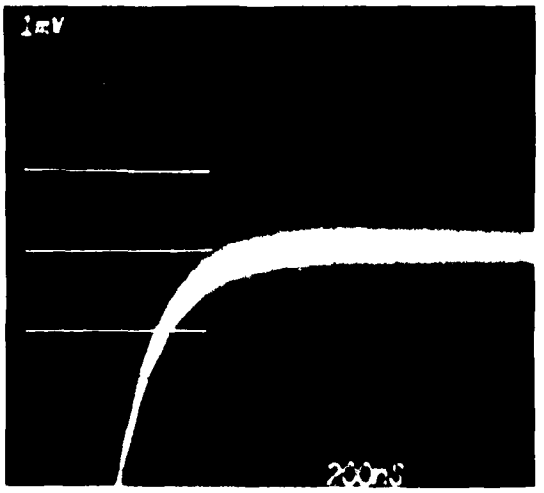
1-0 Transition Overall
(c)

1-0 Transition Expanded
(d)

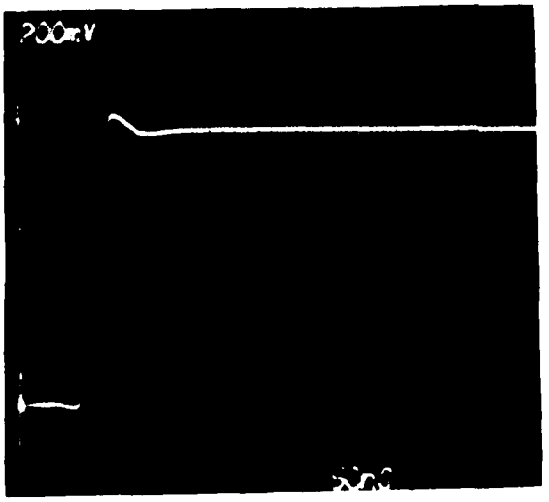
Figure 7-14. Settling time waveforms S/N 4312.



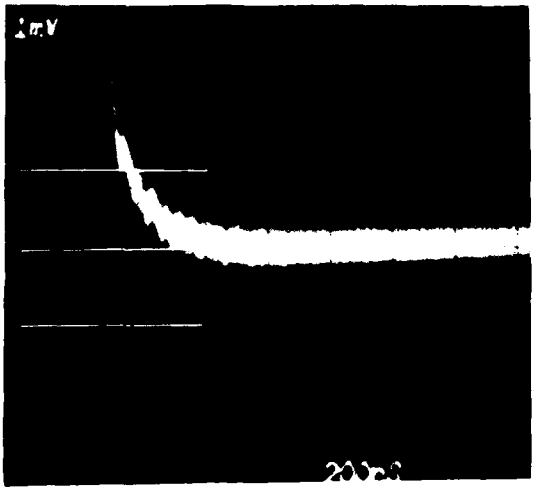
0-1 Transition Overall
(a)



0-1 Transition Expanded
(b)

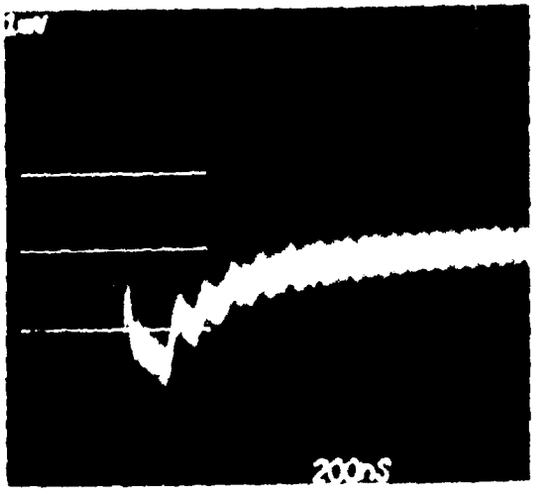


1-0 Transition Overall
(c)

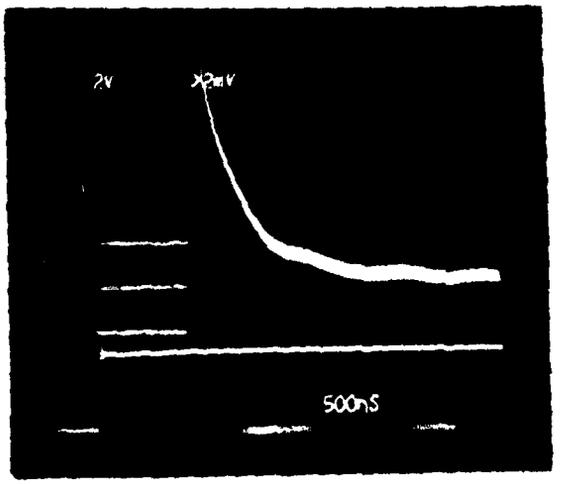


1-0 Transition Expanded
(d)

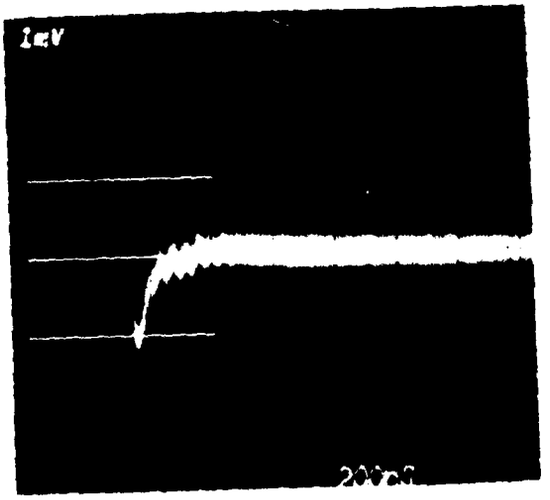
Figure 7-15. Settling time waveforms S/N 07.



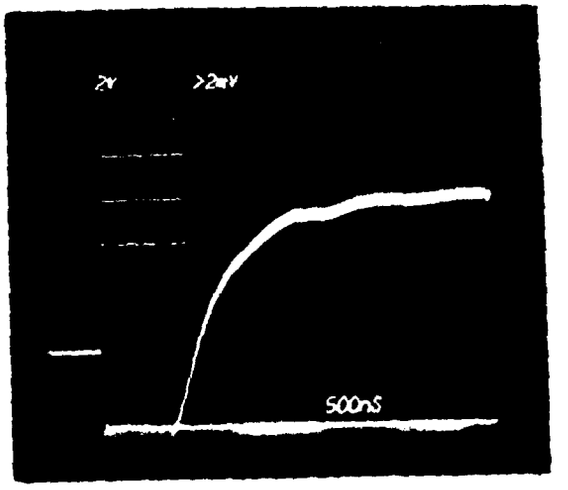
0-1 Transition with
GEOS Test Circuit



0-1 Transition with
Vendor Test Circuit

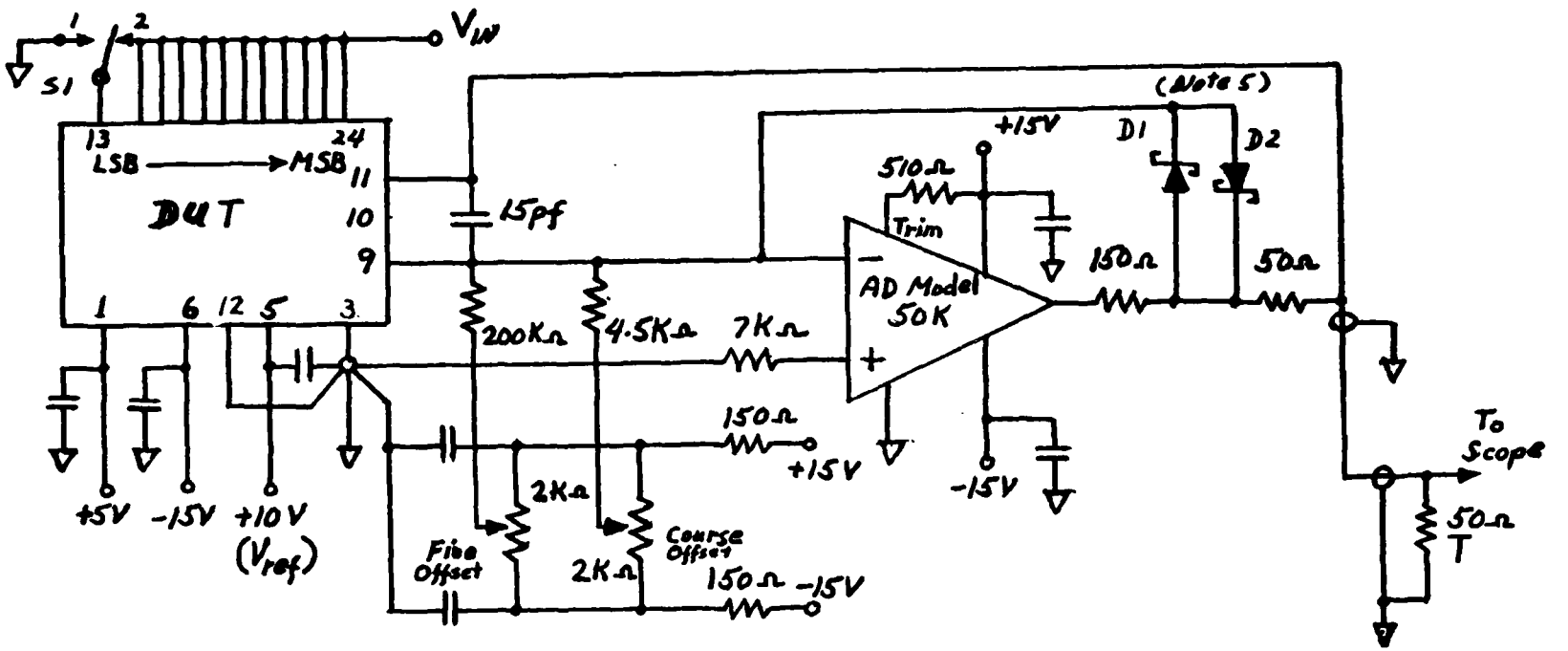


1-0 Transition with
GEOS Test Circuit



1-0 Transition with
Vendor Test Circuit

Figure 7-16. Settling time waveforms S/N 35.



VII-40

Notes: 1. Unless otherwise defined, all capacitors are 47 uF tantalum paralleled with 0.1 uF ceramic.

2. Bandwidth of the oscilloscope shall be 50 MHz minimum; saturation of the preamp must be avoided. Use a voltage comparator preamp.

3. Adjust the course and fine offset control to position the waveform final value on the oscilloscope center horizontal graticule.

4. While operating switch S-1, adjust the oscilloscope vertical gain for 1/2 LSB per cm.

5. D1 = D2 = HP 5082-2835 or equivalent.

Figure 7-17. Test circuit for settling time, device type 01.

TABLE 7-4. Device Type 01 Data at + 25°C.

MANUFACTURER CODE: ; DEVICE TYPE: 868; TEMPERATURE: 25 DEG C ; 25 OCT 78 10:58:08

PARAMETER	LO-LIM	4310	4312	4313	4314	4315	5	10	20	21	25	HI-LIM	UNITS
ICC-SUPPLY CURRENT	3.00	11.8	18.3	18.0	11.8	11.8	18.3	18.3	13.0	13.1	13.7	18.0	MA
IEE-SUPPLY CURRENT	-25.0	-16.5	-16.3	-15.8	-16.6	-16.7	-17.3	-16.0	-17.8	-17.3	-18.3	-5.00	MA
IIH FOR BIT# 1	-1.00	2.00	1.95	2.40	1.95	1.90	1.90	2.05	2.10	1.95	1.85	100.	UA
IIH FOR BIT# 2	-1.00	1.85	1.80	1.95	2.10	1.75	1.70	1.85	1.75	1.80	1.80	100.	UA
IIH FOR BIT# 3	-1.00	1.85	2.20	1.80	1.85	1.90	1.95	2.00	1.85	1.85	1.85	100.	UA
IIH FOR BIT# 4	-1.00	1.90	2.05	1.95	1.85	1.80	1.95	1.80	2.05	1.70	1.90	100.	UA
IIH FOR BIT# 5	-1.00	1.95	2.25	2.10	2.05	1.75	1.90	1.85	2.20	2.05	1.85	100.	UA
IIH FOR BIT# 6	-1.00	1.80	2.20	1.85	2.05	2.05	1.95	1.85	1.85	1.80	1.85	100.	UA
IIH FOR BIT# 7	-1.00	2.05	2.40	1.90	1.80	2.20	2.20	1.95	1.95	1.95	1.95	100.	UA
IIH FOR BIT# 8	-1.00	1.95	2.15	2.25	1.90	1.90	2.20	1.80	2.10	1.90	2.00	100.	UA
IIH FOR BIT# 9	-1.00	2.35	2.45	2.35	2.30	2.15	2.20	2.30	2.20	2.35	2.20	100.	UA
IIH FOR BIT# 10	-1.00	2.35	2.40	2.30	2.35	2.45	2.40	1.95	2.20	1.90	2.40	100.	UA
IIH FOR BIT# 11	-1.00	2.55	2.40	2.55	2.60	2.55	2.55	2.50	2.35	2.35	2.75	100.	UA
IIH FOR BIT# 12	-1.00	3.80	4.00	3.70	3.55	3.40	3.55	3.60	3.75	3.50	3.80	100.	UA
IIL FOR BIT# 1	-200.	-8.40	-9.10	-8.65	-8.85	-8.55	-9.35	-8.45	-8.70	-10.8	-10.6	1.00	UA
IIL FOR BIT# 2	-200.	-8.60	-8.95	-8.80	-9.80	-8.80	-9.55	-9.05	-7.30	-9.70	-10.2	1.00	UA
IIL FOR BIT# 3	-200.	-8.45	-8.85	-8.65	-8.75	-8.55	-11.3	-8.65	-7.20	-9.55	-10.2	1.00	UA
IIL FOR BIT# 4	-200.	-8.50	-8.75	-8.75	-8.70	-8.70	-8.75	-8.25	-7.15	-9.45	-10.3	1.00	UA
IIL FOR BIT# 5	-200.	-8.30	-8.80	-8.55	-8.60	-8.80	-11.4	-8.85	-7.10	-9.35	-10.0	1.00	UA
IIL FOR BIT# 6	-200.	-8.35	-8.80	-8.70	-8.50	-8.75	-10.1	-13.6	-7.05	-9.40	-9.95	1.00	UA
IIL FOR BIT# 7	-200.	-8.30	-8.75	-8.60	-8.55	-8.65	-8.70	-9.15	-6.95	-9.25	-9.70	1.00	UA
IIL FOR BIT# 8	-200.	-8.25	-8.55	-8.60	-8.50	-8.70	-14.0	-9.60	-7.20	-9.30	-9.70	1.00	UA
IIL FOR BIT# 9	-200.	-8.05	-8.75	-8.55	-8.55	-8.55	-9.55	-9.05	-7.05	-8.95	-9.50	1.00	UA
IIL FOR BIT# 10	-200.	-8.25	-9.50	-8.65	-8.45	-8.55	-8.60	-9.05	-6.75	-9.05	-9.35	1.00	UA
IIL FOR BIT# 11	-200.	-7.95	-9.65	-8.45	-8.45	-8.65	-8.55	-8.80	-6.65	-8.95	-14.5	1.00	UA
IIL FOR BIT# 12	-200.	-7.95	-8.65	-8.45	-8.50	-8.55	-9.10	-8.70	-6.75	-9.00	-15.1	1.00	UA
FULL SCALE CURR.-TTL	1.50	1.93	1.94	1.92	1.93	1.91	2.28	2.17	1.94	2.01	2.20	2.50	MA
FULL SCALE CURR.-CMOS	1.50	1.93	1.94	1.93	1.93	1.93	2.29	2.18	1.94	2.00	2.20	2.50	MA
ZERO SCALE CURR.-TTL	-1.00K	-58.0	-23.5	-38.0	-31.5	-41.0	-72.0	-108.	-97.5	-95.0	5.00	1.00K	MA
ZERO SCALE CURR.-CMOS	-1.00K	-72.0	-60.5	-68.5	-38.5	-85.0	-114.	-122.	-123.	-100.	-54.0	1.00K	MA
IOZ-DRIFT	-2.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	2.00	PPM/ C
BIPOLAR OFFSET CURR.	750.M	975.M	975.M	965.M	970.M	960.M	1.14	1.09	970.M	1.01	1.10	1.25	MA
+PSS2 (CMOS) [+10%]	-900.	-31.0	-66.6	0.00	-15.4	26.0	-78.6	-88.9	10.3	-89.7	-77.0	900.	UV
+PSS2 (CMOS) [-10%]	-900.	-87.8	-71.8	-31.2	-36.0	-67.5	52.4	-13.8	-61.7	-19.8	-4.63	900.	UV
-PSS1 (TTL) [+10%]	-1.00K	-82.7	-15.4	5.81	-10.3	-5.19	0.00	-27.5	-5.14	-84.8	-77.0	1.00K	UV
-PSS1 (TTL) [-10%]	-1.00K	62.0	36.9	20.8	20.8	15.6	-8.74	55.0	0.00	29.7	31.6	1.00K	UV
BIT WGHT ERR-BIT# 1	-500.M	-20.7M	-1.56M	4.30M	-48.6M	26.6M	-13.5M	-6.06M	805.M	858.M	-67.5M	500.M	LSB
BIT WGHT ERR-BIT# 2	-500.M	37.0M	11.5M	49.7M	43.4M	45.5M	73.9M	49.5M	-27.5M	40.9M	64.6M	500.M	LSB
BIT WGHT ERR-BIT# 3	-500.M	-56.7M	-49.8M	-40.8M	-28.3M	-68.7M	108.M	48.6M	-68.8M	97.6U	77.6M	500.M	LSB
BIT WGHT ERR-BIT# 4	-500.M	6.84M	1.34M	21.6M	1.61M	-31.4M	-84.6M	-43.4M	-63.6M	-37.8M	-6.71M	500.M	LSB
BIT WGHT ERR-BIT# 5	-500.M	37.3M	-49.7M	26.4M	96.6M	10.4M	-63.6M	87.1M	-7.76M	-86.7M	41.7M	500.M	LSB
BIT WGHT ERR-BIT# 6	-500.M	-6.68M	-37.8M	-63.3M	-16.8M	-8.37M	-90.3M	-7.11M	-16.6M	-44.8M	-14.4M	500.M	LSB
BIT WGHT ERR-BIT# 7	-500.M	-8.13M	10.7M	-18.1M	48.3M	16.6M	-38.8M	-5.42M	8.66M	-8.19M	18.3M	500.M	LSB
BIT WGHT ERR-BIT# 8	-500.M	-13.6M	8.48M	-41.1M	29.1M	-8.09M	-83.5M	80.7M	-981.U	-6.86M	7.08M	500.M	LSB
BIT WGHT ERR-BIT# 9	-500.M	-38.8M	19.7M	-84.8M	85.8M	-6.36M	-6.47M	-8.38M	6.88M	81.6M	-81.6M	500.M	LSB
BIT WGHT ERR-BIT# 10	-500.M	1.88M	17.3M	8.84M	80.3M	-1.68M	86.8M	-1.38M	-86.6M	10.5M	-4.03M	500.M	LSB
BIT WGHT ERR-BIT# 11	-500.M	-7.88M	4.47M	-14.7M	-10.8M	-87.4M	7.87M	-18.8M	-19.9M	-6.86M	-1.05M	500.M	LSB
BIT WGHT ERR-BIT# 12	-500.M	4.71M	4.34M	4.39M	81.4M	-1.98M	17.8M	86.8M	-466.U	40.8M	87.3M	500.M	LSB

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

TABLE 7-4 Device Type 01 Data at + 25°C. (cont'd)

MANUFACTURER CODE: ; DEVICE TYPE: 888; TEMPERATURE: 85 DEG C ; 85 OCT 78 10:88:84

PARAMETER	LO-LIM	35	40	HI-LIM	UNITS
ICC-SUPPLY CURRENT	3.00	13.8	13.3	18.8	MA
IEE-SUPPLY CURRENT	-88.8	-17.8	-17.1	-6.00	MA
IIH FOR BIT8 1	-1.88	1.88	1.78	188.	MA
IIH FOR BIT8 2	-1.88	1.88	8.18	188.	MA
IIH FOR BIT8 3	-1.88	1.88	1.38	188.	MA
IIH FOR BIT8 4	-1.88	1.88	1.88	188.	MA
IIH FOR BIT8 5	-1.88	1.88	1.88	188.	MA
IIH FOR BIT8 6	-1.88	8.18	8.18	188.	MA
IIH FOR BIT8 7	-1.88	1.88	1.88	188.	MA
IIH FOR BIT8 8	-1.88	8.18	1.88	188.	MA
IIH FOR BIT8 9	-1.88	1.88	8.88	188.	MA
IIH FOR BIT8 18	-1.88	8.38	8.38	188.	MA
IIH FOR BIT8 11	-1.88	8.38	8.38	188.	MA
IIH FOR BIT8 12	-1.88	3.88	3.38	188.	MA
IIL FOR BIT8 1	-288.	-11.1	-7.88	1.88	MA
IIL FOR BIT8 2	-288.	-11.8	-8.38	1.88	MA
IIL FOR BIT8 3	-288.	-11.1	-7.88	1.88	MA
IIL FOR BIT8 4	-288.	-11.8	-7.98	1.88	MA
IIL FOR BIT8 5	-288.	-18.8	-7.88	1.88	MA
IIL FOR BIT8 6	-288.	-18.8	-7.95	1.88	MA
IIL FOR BIT8 7	-288.	-18.7	-7.95	1.88	MA
IIL FOR BIT8 8	-288.	-18.7	-7.85	1.88	MA
IIL FOR BIT8 9	-288.	-18.6	-7.65	1.88	MA
IIL FOR BIT8 18	-288.	-18.7	-7.75	1.88	MA
IIL FOR BIT8 11	-288.	-18.1	-7.68	1.88	MA
IIL FOR BIT8 12	-288.	-18.1	-7.68	1.88	MA
FULL SCALE CURR.-TTL	1.58	2.89	1.99	2.58	MA
FULL SCALE CURR.-CMOS	1.58	2.89	1.99	2.58	MA
ZERO SCALE CURR.-TTL	-1.88K	-94.5	-134.	1.88K	MA
ZERO SCALE CURR.-CMOS	-1.88K	-124.	-119.	1.88K	MA
IOZ-DRIFT	-2.88	8.88	8.88	2.88	PPM/C
BIPOLAR OFFSET CURR.	758.M	1.85	995.M	1.25	MA
+PSS2 (CMOS) [+18%]	-888.	-81.2	-15.1	888.	UU
+PSS2 (CMOS) [-18%]	-888.	-33.4	-45.2	888.	UU
-PS81 (TTL) [+18%]	-1.88K	-85.5	-88.3	1.88K	UU
-PS81 (TTL) [-18%]	-1.88K	33.4	18.8	1.88K	UU
BIT WGHT ERR-BIT8 1	-888.M	48.8M	831.M	888.M	LSB
BIT WGHT ERR-BIT8 2	-888.M	-88.8M	883.U	888.M	LSB
BIT WGHT ERR-BIT8 3	-888.M	-73.5M	-73.8M	888.M	LSB
BIT WGHT ERR-BIT8 4	-888.M	-87.3M	-113.M	888.M	LSB
BIT WGHT ERR-BIT8 5	-888.M	87.8M	-21.8M	888.M	LSB
BIT WGHT ERR-BIT8 6	-888.M	17.9M	-8.84M	888.M	LSB
BIT WGHT ERR-BIT8 7	-888.M	88.7M	-18.7M	888.M	LSB
BIT WGHT ERR-BIT8 8	-888.M	874.U	-11.8M	888.M	LSB
BIT WGHT ERR-BIT8 9	-888.M	-888.U	-18.1M	888.M	LSB
BIT WGHT ERR-BIT8 18	-888.M	-13.1M	-18.8M	888.M	LSB
BIT WGHT ERR-BIT8 11	-888.M	-48.8M	-13.3M	888.M	LSB
BIT WGHT ERR-BIT8 12	-888.M	-8.88M	18.8M	888.M	LSB

NOTES:1.ZERO (8) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

TABLE 7-4. Device Type 01 Data at + 25°C.

MANUFACTURER CODE: ; DEVICE TYPE: 868; TEMPERATURE: 25 DEG C ; 25 OCT 78 10:08:45

PARAMETER	LO-LIM	4310	4312	4313	4314	4315	5	19	20	21	26	HI-LIM	UNITS
SUM BIT ERROR(+)	-900.M	30.7M	49.7M	78.1M	138.M	90.7M	104.M	104.M	188.M	222.M	140.M	900.M	LSB
SUM BIT ERROR(-)	-900.M	-78.8M	-30.7M	-100.M	-188.M	-93.8M	-154.M	-117.M	-801.M	-815.M	-111.M	900.M	LSB
SUM-ERROR(+)+ERROR(-)	-100.M	-38.8M	18.0M	-30.8M	11.3M	-18.8M	11.0M	-13.1M	-16.4M	17.8M	28.4M	100.M	LSB
GAIN ERROR (TTL)	-25.0	-4.48	-1.18	-861.M	-3.84	-1.18	6.83	8.36	4.00	4.18	5.63	25.0	MV
GAIN ERROR (CMOS)	-25.0	-4.78	-1.60	-1.00	-3.36	-1.36	6.81	8.14	4.40	4.15	5.40	25.0	MV
GAIN ERROR DRIFT (TTL)	-5.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	5.00	PPM/ C
BIPOLAR OFFSET ERROR	-20.0	-2.70	-3.40	-731.M	-4.16	-3.43	-3.57	-4.58	-788.M	-3.80	-3.80	20.0	MV
BPOE DRIFT	-4.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	4.00	PPM/ C
+PSS1 (TTL) [+10%]	-800.	-165.	-97.4	-78.1	-30.8	-31.2	-78.6	-68.8	-113.	-104.	-96.2	800.	UV
+PSS1 (TTL) [-10%]	-800.	87.8	0.00	-10.4	30.8	0.00	30.6	0.00	0.00	49.6	36.3	800.	UV
MJR CARRY ERR-BITS 1	-900.M	-3.63M	45.1M	18.9M	-113.M	64.0M	-13.4M	-30.9M	389.M	456.M	-162.M	900.M	LSB
MJR CARRY ERR-BITS 2	-900.M	95.5M	117.M	128.M	-935.U	126.M	151.M	76.1M	151.M	261.M	60.7M	900.M	LSB
MJR CARRY ERR-BITS 3	-900.M	-54.4M	48.4M	2.20M	-101.M	-31.8M	250.M	101.M	85.8M	198.M	135.M	900.M	LSB
MJR CARRY ERR-BITS 4	-900.M	21.7M	94.6M	89.7M	-50.2M	-6.26M	121.M	-815.U	1.64M	113.M	42.1M	900.M	LSB
MJR CARRY ERR-BITS 5	-900.M	76.7M	-6.16M	120.M	129.M	70.4M	45.8M	112.M	56.4M	1.62M	114.M	900.M	LSB
MJR CARRY ERR-BITS 6	-900.M	21.7M	-31.4M	-2.03M	-27.0M	23.5M	-61.5M	55.5M	5.86M	13.8M	-19.1M	900.M	LSB
MJR CARRY ERR-BITS 7	-900.M	36.5M	21.1M	23.6M	42.5M	51.2M	-2.47M	44.2M	5.86M	19.9M	34.7M	900.M	LSB
MJR CARRY ERR-BITS 8	-900.M	21.6M	14.8M	-4.17M	6.65M	-6.25M	-20.4M	38.6M	5.86M	-416.U	23.6M	900.M	LSB
MJR CARRY ERR-BITS 9	-900.M	6.83M	14.8M	27.8M	8.76M	-1.99M	-15.0M	-6.44M	10.1M	17.9M	-6.11M	900.M	LSB
MJR CARRY ERR-BITS 10	-900.M	38.6M	21.1M	25.7M	19.3M	19.3M	31.5M	2.94M	-13.1M	-22.7M	21.7M	900.M	LSB
MJR CARRY ERR-BITS 11	-900.M	-12.2M	136.U	-19.1M	-37.6M	-25.4M	-9.63M	-42.1M	-19.4M	-47.1M	-28.4M	900.M	LSB

TABLE 7-4. Device Type 01 Data at + 25°C.

MANUFACTURER CODE: ; DEVICE TYPE: 568; TEMPERATURE: 25 DEG C ; 25 OCT 78 10:58:59

PARAMETER		LO-LIM	36	48	HI-LIM	UNITS
SUM BIT ERROR(+)		-500.M	151.M	200.M	500.M	LSB
SUM BIT ERROR(-)		-500.M	-180.M	-252.M	500.M	LSB
SUM-ERROR(+)+ERROR(-)		-100.M	-30.3M	-52.0M	100.M	LSB
GAIN ERROR (TTL)		-25.0	3.63	5.05	25.0	MV
GAIN ERROR (CMOS)		-25.0	3.17	4.88	25.0	MV
GAIN ERROR DRIFT (TTL)		-5.00	0.00	0.00	5.00	PPM/C
BIPOLAR OFFSET ERROR		-20.0	-2.11	-3.12	20.0	MV
BPOE DRIFT		-4.00	0.00	0.00	4.00	PPM/C
+PSS1 (TTL) [+10%]		-800.	-43.0	-20.1	800.	UV
+PSS1 (TTL) [-10%]		-800.	-23.9	-15.1	800.	UV
MJR CARRY ERR-BITS	1	-900.M	111.M	464.M	900.M	LSB
MJR CARRY ERR-BITS	2	-900.M	-80.6M	242.M	900.M	LSB
MJR CARRY ERR-BITS	3	-900.M	-112.M	98.1M	900.M	LSB
MJR CARRY ERR-BITS	4	-900.M	-133.M	-36.4M	900.M	LSB
MJR CARRY ERR-BITS	5	-900.M	52.5M	48.8M	900.M	LSB
MJR CARRY ERR-BITS	6	-900.M	23.1M	50.9M	900.M	LSB
MJR CARRY ERR-BITS	7	-900.M	19.2M	20.1M	900.M	LSB
MJR CARRY ERR-BITS	8	-900.M	-6.20M	7.73M	900.M	LSB
MJR CARRY ERR-BITS	9	-900.M	13.4M	-25.2M	900.M	LSB
MJR CARRY ERR-BITS	10	-900.M	-6.20M	-12.8M	900.M	LSB
MJR CARRY ERR-BITS	11	-900.M	-39.4M	-29.3M	900.M	LSB

Table 4-5. Device Type 62 Data at + 25°

MANUFACTURER CODE: 8; DEVICE TYPE: 62; TEMPERATURE: 25 DEG C , 12 MAR 80 21:30:03

PARAMETER	LO-LIM	6	7	9	13	15	22	60	87	88	HI-LIM	UNITS
ICC-SUPPLY CURRENT	3.00	3.0	12.3	11.2	10.8	10.4	10.7	11.3	9.25	11.8	18.0	MA
IEE-SUPPLY CURRENT	-40.2	-4.0	-3.3	-3.8	-25.8	-20.5	-28.0	-20.6	-21.8	-20.8	-5.00	MA
IIH FOR BIT# 1	-1.00	4.0	4.2	3.9	5.05	1.65	2.35	1.70	1.25	1.90	100.	MA
IIH FOR BIT# 2	-1.00	2.15	2.05	1.80	3.80	1.90	2.05	1.45	1.80	1.05	100.	MA
IIH FOR BIT# 3	-1.00	2.05	2.2	1.85	3.55	1.30	2.00	1.60	1.35	1.60	100.	MA
IIH FOR BIT# 4	-1.00	2.15	1.95	1.90	3.70	1.70	2.10	1.70	1.45	1.80	100.	MA
IIH FOR BIT# 5	-1.00	1.95	1.95	1.60	3.70	1.35	1.70	1.60	1.65	1.75	100.	MA
IIH FOR BIT# 6	-1.00	2.15	2.10	1.95	4.00	1.80	2.20	1.65	1.80	1.35	100.	MA
IIH FOR BIT# 7	-1.00	2.35	2.40	1.85	3.85	1.70	2.15	1.65	1.65	1.60	100.	MA
IIH FOR BIT# 8	-1.00	2.60	2.10	1.85	4.00	1.80	2.15	1.85	1.75	1.95	100.	MA
IIH FOR BIT# 9	-1.00	2.40	2.35	1.85	4.00	1.90	2.25	1.80	1.90	1.95	100.	MA
IIH FOR BIT# 10	-1.00	2.60	2.45	2.40	5.10	2.20	2.45	2.05	1.95	1.95	100.	MA
IIH FOR BIT# 11	-1.00	2.70	2.75	2.25	4.15	2.10	2.40	2.15	1.95	2.25	100.	MA
IIH FOR BIT# 12	-1.00	3.95	3.45	3.05	5.55	3.25	3.80	3.20	3.30	3.35	100.	MA
IIL FOR BIT# 1	-200.	-9.65	-5.65	-6.10	-14.4	-6.30	-11.0	-4.45	-7.20	-6.05	1.00	UA
IIL FOR BIT# 2	-200.	-5.05	-2.85	-3.00	-7.25	-3.25	-5.35	-2.25	-3.60	-3.00	1.00	UA
IIL FOR BIT# 3	-200.	-5.15	-2.85	-3.05	-7.40	-3.15	-5.65	-2.25	-3.60	-3.10	1.00	UA
IIL FOR BIT# 4	-200.	-4.80	-2.95	-3.15	-7.55	-3.15	-5.20	-2.25	-3.70	-3.15	1.00	UA
IIL FOR BIT# 5	-200.	-5.50	-3.00	-3.05	-7.45	-3.20	-5.45	-2.25	-3.60	-3.20	1.00	UA
IIL FOR BIT# 6	-200.	-5.05	-2.95	-3.05	-7.50	-3.20	-5.60	-2.25	-3.70	-3.15	1.00	UA
IIL FOR BIT# 7	-200.	-5.00	-2.90	-3.00	-7.35	-3.25	-5.60	-2.15	-3.75	-3.15	1.00	UA
IIL FOR BIT# 8	-200.	-5.00	-2.95	-3.05	-7.25	-3.25	-5.80	-2.20	-3.55	-3.10	1.00	UA
IIL FOR BIT# 9	-200.	-4.90	-2.90	-3.00	-7.30	-3.15	-5.65	-2.20	-3.55	-3.15	1.00	UA
IIL FOR BIT# 10	-200.	-5.05	-2.95	-3.05	-7.55	-3.15	-5.75	-2.35	-3.65	-3.05	1.00	UA
IIL FOR BIT# 11	-200.	-4.95	-3.00	-3.00	-7.35	-3.20	-5.95	-2.15	-3.55	-3.05	1.00	UA
IIL FOR BIT# 12	-200.	-5.05	-3.00	-3.00	-7.50	-3.15	-5.50	-2.35	-3.60	-3.10	1.00	UA
FULL SCALE CURR.-TTL	4.00	4.80	4.58	5.18	4.57	4.58	5.21	4.48	5.12	4.52	6.00	MA
FULL SCALE CURR.-CMOS	4.00	4.80	4.59	5.18	4.58	4.59	5.22	4.48	5.12	4.51	6.00	MA
ZERO SCALE CURR.-TTL	-2.50K	-690.	-705.	-860.	-850.	-925.	-850.	-865.	-990.	-905.	2.50K	NA
ZERO SCALE CURR.-CMOS	-2.50K	-695.	-720.	-855.	-835.	-930.	-835.	-880.	-995.	-920.	2.50K	NA
IOZ-DRIFT	-2.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	2.00	PPM/C
BIPOLAR OFFSET CURR.	2.00	2.42	2.31	2.61	2.31	2.30	2.63	2.25	2.50	2.27	3.00	MA
+PSS2 (CMOS) [+10%]	-800.	-6.23	-37.0	-23.2	-26.2	-28.3	-1.92	-15.6	-1.95	-33.1	800.	UV
+PSS2 (CMOS) [-10%]	-800.	-39.5	0.00	-23.2	-17.5	13.1	-7.68	-13.4	-3.91	17.7	800.	UV
-PSS1 (TTL) [+10%]	-1.60K	-20.8	-13.1	-42.5	-10.9	-26.2	0.00	-17.8	3.91	-13.3	1.60K	UV
-PSS1 (TTL) [-10%]	-1.60K	6.23	17.4	32.8	0.00	17.4	-26.9	-8.91	1.95	6.63	1.60K	UV
BIT WGHT ERR-BIT# 1	-500.M	-288.M	-259.M	-315.M	-297.M	-256.M	-364.M	-261.M	-328.M	-252.M	500.M	LSB
BIT WGHT ERR-BIT# 2	-500.M	-132.M	-91.4M	-150.M	-105.M	-63.0M	-215.M	-84.5M	-161.M	-85.6M	500.M	LSB
BIT WGHT ERR-BIT# 3	-500.M	-96.2M	-39.8M	-64.8M	-66.9M	-15.0M	-149.M	-51.4M	-47.9M	-13.4M	500.M	LSB
BIT WGHT ERR-BIT# 4	-500.M	37.0M	86.1M	-391.U	32.0M	83.8M	19.0M	19.9M	-87.6M	9.16M	500.M	LSB
BIT WGHT ERR-BIT# 5	-500.M	8.78M	47.3M	4.84M	81.3M	10.6M	-3.11M	1.31M	-20.6M	-4.47M	500.M	LSB
BIT WGHT ERR-BIT# 6	-500.M	-84.1M	-13.8M	-293.U	-13.6M	8.16M	-84.7M	-11.2M	-4.89M	482.U	500.M	LSB
BIT WGHT ERR-BIT# 7	-500.M	-58.0M	80.0M	-11.2M	8.81M	-3.61M	80.1M	-12.0M	8.88M	-16.5M	500.M	LSB
BIT WGHT ERR-BIT# 8	-500.M	-38.4M	18.1M	8.30M	-17.0M	-8.08M	43.0M	-18.8M	-17.9M	-14.6M	500.M	LSB
BIT WGHT ERR-BIT# 9	-500.M	18.8M	8.84M	-7.85M	84.6M	-8.88M	-8.01M	-81.9M	-7.34M	-6.03M	500.M	LSB
BIT WGHT ERR-BIT# 10	-500.M	4.44M	-37.1M	-8.33M	-8.48M	-468.U	10.8M	-88.4M	-88.1M	-17.9M	500.M	LSB
BIT WGHT ERR-BIT# 11	-500.M	34.1M	-85.8M	-803.U	781.U	14.6M	-3.88M	-8.90M	9.37M	99.6U	500.M	LSB
BIT WGHT ERR-BIT# 12	-500.M	37.8M	-88.1M	-1.49M	14.3M	-8.88M	110.U	883.U	956.U	500.M	500.M	LSB

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 7-5. Device Type 02 Data at + 25 C. (Cont'd)

MANUFACTURER CODE: X; DEVICE TYPE: 668; TEMPERATURE: 25 DEG C ; 18 MAR 80 21:30:58

PARAMETER	LO-LIM	6	7	8	13	15	22	69	87	88	HI-LIM	UNITS
SUM BIT ERROR(+)	-600.M	132.M	216.M	-14.9M	87.6M	38.8M	180.M	18.2M	306.U	5.88M	600.M	LSB
SUM BIT ERROR(-)	-600.M	-258.M	-285.M	-71.1M	-198.M	-139.M	-267.M	-133.M	-19.1M	-88.3M	600.M	LSB
SUM-ERROR(+)+ERROR(-)	-100.M	-127.M x	-48.9M	-86.0M	-105.M x	-101.M x	-147.M x	-121.M x	-18.8M	-83.1M	100.M	LSB
GAIN ERROR (TTL)	-25.0	8.04	5.89	-1.11	9.40	-1.37	6.48	-1.24	-2.95	-706.M	25.0	MV
GAIN ERROR (CMOS)	-25.0	8.00	5.92	-970.M	9.56	-1.14	6.45	-1.11	-2.86	-519.M	25.0	MV
GAIN ERROR DRIFT (TTL)	-5.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	5.00	PPM/C
BIPOLAR OFFSET ERROR	-20.0	19.8	20.4 x	-5.62	20.9 x	-7.88	23.5 x	-5.56	-6.46	-5.00	20.0	MV
BPOE DRIFT	-4.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	4.00	PPM/C
+PSS1 (TTL) [+10%]	-800.	0.00	6.53	5.80	8.75	-17.4	-1.92	-22.3	-13.7	30.9	800.	UV
+PSS1 (TTL) [-10%]	-800.	2.16K	2.12K	1.94K	2.07K	1.88K	2.07K	1.96K	1.90K	1.95K	800.	UV
MJR CARRY ERR-BITS 1	-900.M	-137.M	-259.M	-130.M	-207.M	-193.M	-158.M	-142.M	30.6M	-137.M	900.M	LSB
MJR CARRY ERR-BITS 2	-900.M	-83.3M	-158.M	-55.4M	-103.M	-31.1M	-189.M	-10.8M	-25.3M	-24.5M	900.M	LSB
MJR CARRY ERR-BITS 3	-900.M	-147.M	-163.M	-48.2M	-138.M	-31.1M	-277.M	-41.9M	41.1M	27.2M	900.M	LSB
MJR CARRY ERR-BITS 4	-900.M	16.2M	-12.2M	20.7M	-23.3M	35.8M	-88.7M	62.1M	25.9M	39.0M	900.M	LSB
MJR CARRY ERR-BITS 5	-900.M	-18.7M	15.5M	40.4M	-5.43M	28.7M	-99.7M	46.6M	24.3M	29.0M	900.M	LSB
MJR CARRY ERR-BITS 6	-900.M	-57.8M	-56.7M	23.8M	-53.8M	29.6M	-127.M	33.9M	33.9M	32.6M	900.M	LSB
MJR CARRY ERR-BITS 7	-900.M	-134.M	123.M	8.01M	-21.5M	33.1M	-645.U	49.4M	29.9M	9.10M	900.M	LSB
MJR CARRY ERR-BITS 8	-900.M	-137.M	89.5M	19.1M	-49.3M	18.0M	36.3M	29.3M	-6.12M	10.0M	900.M	LSB
MJR CARRY ERR-BITS 9	-900.M	-58.6M	85.9M	-3.07M	18.7M	1.00M	-9.29M	12.9M	-6.12M	4.58M	900.M	LSB
MJR CARRY ERR-BITS 10	-900.M	-73.1M	18.1M	-1.49M	-21.5M	9.93M	11.1M	-4.45M	-38.9M	-22.6M	900.M	LSB
MJR CARRY ERR-BITS 11	-900.M	-3.35M	3.87M	885.U	-13.5M	19.8M	-1.43M	-9.01M	9.09M	-855.U	900.M	LSB

TABLE 7-6. Output Settling Time Data.

Device Types 01 & 02

Serial Number of Device	All Bits Off to All Bits On	All Bits On to All Bits Off
00005	500 ns	260 ns
00019	480 ns	300 ns
00020	500 ns	260 ns
00021	480 ns	260 ns
00025	480 ns	220 ns
00035	480 ns	360 ns
00048	480 ns	245 ns
04310	400 ns	290 ns
04311	370 ns	240 ns
04312	360 ns	240 ns
04313	370 ns	245 ns
04314	380 ns	245 ns
04315	400 ns	240 ns
6	480 ns	360 ns
7	450 ns	380 ns
13	480 ns	380 ns
22	500 ns	360 ns

Table 7-7 . Comparison of Bit Linearity Error Test Methods
(V_{cc} = + 5 V V_{ee} = - 15 V)

Serial Number	Temp (°C)	A. Superposition Method W/C Pos. Code	A. Superposition Method W/C Pos. Value (LSB)	A. Superposition Method W/C Neg. Code	A. Superposition Method W/C Neg. Value (LSB)	B. 16-Segment Method W/C Pos. Code	B. 16-Segment Method W/C Pos. Value (LSB)	B. 16-Segment Method W/C Neg. Code	B. 16-Segment Method W/C Neg. Value (LSB)	C. All-codes Method W/C Pos. Code	C. All-codes Method W/C Pos. Value (LSB)	C. All-codes Method W/C Neg. Code	C. All-codes Method W/C Neg. Value (LSB)
5	125	1836	.360	2259	-.270	1836	.360	2259	-.270	1838	.360	2258	-.270
	25	1549	.160	2546	-.286	1549	.160	2547	-.286	1550	.160	2546	-.287
	-55	2566	.820	1529	-.700	2566	.820	1529	-.745	2570	.826	496	-.747
9	125	31	.072	4046	-.151	31	.072	2687	-.330	62	.082	2559	-.334
	25	0	-0-	4095	-.054	0	-0-	2816	-.265	4032	.016	2045	-.292
	-55	1920	.850	2175	-1.02	1920	.850	2175	-1.10	1959	.874	2117	-1.13
87	125	255	.105	3840	-.140	255	.105	3072	-.280	126	.121	3103	-.285
	25	99	.017	3996	+.096	3939	.098	1948	-.290	4089	.113	2038	-.302
	-55	0	-0-	4095	+.085	3840	.185	2559	-.325	4031	.202	2460	-.338
88	125	247	.138	3838	-.299	503	.185	3080	-.320	510	.196	3071	-.343
	25	91	-.042	4004	-.080	8	.008	2484	-.300	8	.008	2725	-.303
	-55	3072	.315	1023	-.420	3584	.442	1023	-.420	3584	.442	1014	-.443
4310	125	1289	.117	2806	-.135	89	.117	2806	-.135	1280	.124	2805	-.140
	25	1409	.080	2686	-.096	1409	.080	2687	-.090	1440	.088	2653	-.105
	-55	3297	.140	798	-.140	3297	.140	798	-.140	3304	.146	782	-.156
4312	125	3841	.147	254	-.082	3841	.147	2302	.147	3840	.147	2293	-.177
	25	3113	.120	982	-.124	3369	.122	982	-.124	3328	.123	965	-.125
	-55	3113	.148	982	-.093	3113	.148	726	-.068	3258	.159	837	-.079

Table 7-8. Electrical Performance Characteristics.

Characteristics	Symbol	Conditions	Device Type	Limits Min	Limits Max	Unit
Monotonicity	-	Guaranteed by the Bit Linearity and Major Carry Error Tests	All	-	12	Bits
Supply current from Vcc	Icc	Vcc = + 15V All input bits = +10.5V	01,02 03	3 3	18 20	mA mA
Supply current from Vee	Iee	Vcc = + 15V All input bits = +4.5V	01,02 02	-25 -40	-5 -5	mA mA
Logic "1" input current	IIH	Vcc = + 15V, Vin (logic "1") = +10.5V, Each input measured separately	01,03 02	- 1 - 1	+100 +100	uA nA
Logic "0" input current	IIL	Vcc = + 15V Vin (logic "0") = 0 V, Each input measured separately	01,03 02	-200 -100	+1 +1	uA uA
Full scale current	IFS	All inputs logic "1" Vo = 0 V	01,03 02	-2.7 -6	-1.6 -4	mA mA
Zero scale current (TTL)	IZS1	All inputs logic "0" Vo = 0 V, TA = 25oC	All	-.05	+.05	%IFS Current
Zero scale current (CMOS)	IZS2	All input bits = + 4.5V Vo = 0 V, Vcc = +15V, TA = 25oC	All	-.05	+.05	%IFS Current
Zero scale current drift	D-IZS /D-T	All inputs logic "0"	All	- 2	+ 2	PPM IFS /Co
Gain error (TTL)	VFSI1	All inputs logic "1" VFSI = Vo - 9.99756 TA = 25oC	01,02 03	-20 -16	+20 +16	mV mV
Gain error (CMOS)	VFSI2	All input bits = + 10.5V VFSI = Vo - 9.99756 Vcc = +15 V, TA = + 25oC	01,02 03	-20 -16	+20 +16	mV mV
Gain drift	D-VFS /D-T	All inputs logic "1"	01,02 03	- 5 -30	+ 5 +30	PPM VFS /Co

Table 7-8. Electrical Performance Characteristics.

Characteristics	Symbol	Conditions	Device Type	Limits Min	Limits Max	Unit
Bipolar offset error	BPOE	All inputs logic "0" TA = 25oC	01,02	-40	+40	mV
Bipolar offset drift	D-BPO /D-T	All inputs logic "0" Measure D-Vo 2/	01,02	- 4	4	PPM VFS /Co
Bipolar zero error (TTL)	BZE	Input bits = 4000 (octal) TA = 25oC	03	-32	+32	mV
Bipolar zero drift	D-BZ /D-t	Input bits = 4000 (octal)	03	-10	+10	PPM VFS /Co
Bipolar gain error	VFS13	All inputs logic "1" TA = 25oC	01,02 03	-40 -32	+40 +32	mV mV
Power supply sensitivity at full scale from Vcc (TTL)	+PSS1	Vcc = + 5V +/- 0.5 V TA = 25oC 1/ -55oC < TA < + 125oC	01,02 03 01,02 03	-0.8 -3.2 -1.6 -6.4	0.8 3.2 1.6 6.4	mV mV mV mV
Power supply sensitivity at full scale from Vcc (CMOS)	+PSS2	Vcc = + 15 V +/- 1.5 V TA = 25oC 1/ -55oC < TA < 125oC	01,02 03 01,02 03	-0.8 -3.2 -1.6 -6.4	0.8 3.2 1.6 6.4	mV mV mV mV
Power supply sensitivity at full scale from Vee	-PSS1	Vee = -15V +/- 1.5 V TA = 25oC 1/ -55oC < TA < + 125oC	01,02 03 01,02 03	-1.6 -6.4 -3.2 -12.8	1.6 6.4 3.2 12.8	mV mV mV mV

Table 7-8. Electrical Performance Characteristics.

Characteristics	Symbol	Conditions	Device Type	Limits Min	Limits Max	Unit
Bit linearity error	L1-L8	Turn on bits 5 to 12, 1 bit at a time, and measure relative to REF. DAC output. Bits 1 to 4 are turned off. Record the measured bit error signs. 1/	All	-1.22	+1.22	mV
	L9-L23	All combinations of bits 1 to 4, bits 5 to 12 are turned off. Measure Vo relative to REF. DAC output. Record the code words for the worse case positive bit error and for the worse case negative bit error.	All	-1.22	+1.22	mV
	L24	Bits 1 to 4 shall be the code word of the worse case positive bit error in L9-L23. Bits 5 to 12 shall be turned on for corresponding positive bit error measurements in L1 to L8.	All	-1.22	+1.22	mV
	L25	Bits 1 to 4 shall be the code word of the worse case negative bit error in L9-L23. Bits 5 to 12 shall be turned on for corresponding negative bit error measurements in L1 to L8.	All	-1.22	+1.22	mV
	L26-L4119	All combinations of bits 0 to 11. Measure Vo relative to REF DAC output.	All	-1.22	+1.22	mV
Major carry error	MC1-MC11	4000-3777 (octal) to 2-1 1/	All	-1.0	+1.0	LSB

Table 7-8. Electrical Performance Characteristics.

Characteristics	Symbol	Conditions	Device Type	Limits Min	Limits Max	Unit
Output current settling time 0 to FS	tSLH	All inputs switched simultaneously. Time to settle to within 1/2 LSB of final value. TA=25oC	01,03	-	3.0	usec
			02	-	1.0	usec
Output current settling time FS to 0	tSHL	All inputs switched simultaneously. Time to settle to within 1/2 LSB of final value. TA=25oC	01,03	-	3.0	usec
			02	-	1.0	usec
Reference input impedance	Zi	VREF = 10 V TA = 25oC	01	15	2.5	Kohms
			02	6.4	9.6	Kohms
Output noise voltage	No	Vcc = +15V. All inputs TA = 25oC	All	-	6.2	uVrms

Notes:

1. This test is performed in the unipolar mode over a 0 to 10 V range. One LSB is 2.44 mV.
2. VOFS is the full scale voltage range.
3. For device 02, the input voltage, Vin, shall be + 12 V(max).
4. The output compliance voltage range (See 6.4.1) may vary for each vendor. Devices with a finite output resistance will draw additional current that is equal to the output compliance voltage divided by the device output resistance.

SECTION VIII

CMOS MULTIPLYING D/A CONVERTERS

MIL-M-38510/127

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SECTION VIII

CMOS MULTIPLYING D/A CONVERTERS

MIL-M-38510/127

8.1 Introduction

CMOS multiplying digital to analog converters were initially introduced in late 1973 by Analog Devices. Since then these devices have been used in many applications and several other manufacturers have incorporated them into their product lines. Table 8-1 shows the CMOS multiplying D/A converters to be specified in MIL-M-38510/127.

Table 8-1. Table of Device Types Specified.

Device Type	Generic Type	Manufacturer Code *	Multiply D/A Converter Description
01	AD7523S	A,B	8-bit res., 8-bit lin.
02	AD7520U	A,B,C,D	10-bit res., 10-bit lin.
03	AD7521U	A,B,C,D	12-bit res., 10-bit lin.
04	AD7541T	A,C	12-bit res., 12-bit lin.
05	AD7541T	A,C	12-bit res., 12-bit lin.**
06	DAC1020LD	D	(AD7520 U equiv)
07	DAC1221LD	D	(AD7521 U equiv)
08	DAC1220LD	D	(AD7541 T equiv)
09	DAC1220LD	D	(AD7541 T equiv)**

*Manufacturer Code
A = Analog Devices
B = Micro Power
C = Intersil
D = National Semiconductor
**Best fit linearity. All others are specified with end-point linearity.

A recommendation for characterization and possible slash sheet action was made by the JC-41 Committee to RADC. Some device features which should sustain this recommendation are as follows:

1. First monolithic 10-bit D/A converter. (AD7520)

2. Many potential applications and user options.

3. Cost effective with other competing process technologies.

4. Device is sourced by several manufacturers.

5. Low power dissipation.

6. Usage in military systems is high.

8.2 Description of Device Types

This CMOS series of multiplying D/A converters are fabricated with a deposited thin film R-2R ladder over a CMOS integrated circuit. A functional schematic of a typical circuit is shown in Figure 8-1. The R-2R ladder resistors consists of 2 K ohms/square silicon-chromium material arranged to provide the network shown. These resistors have nominal values of 10 K ohms and 20 K ohms with an absolute temperature coefficient of approximately -350 ppm/^{o}C and a tracking temperature coefficient of better than 1 ppm/^{o}C.

When a voltage is applied to the reference terminal of the structure, the precision of the binary division of current is governed by the matching of these resistors and the drop across the associated switches. For proper operation the output terminals Ioutl and Iout2 should be as close to ground reference as possible. The CMOS switches of the integrated circuit structure are shown schematically in Figure 8-2. With the application of a DTL/TTL/CMOS compatible logic signal, two CMOS inverters assume the proper states to drive their respective output switches such that one is "ON" and the other "OFF". The end result is that the same ladder current is steered in either direction. A logic "high" input results in an Ioutl switch position and current flow.

Most applications of these R-2R ladder and switch networks involve an external operational amplifier configured as a current to voltage converter. The feedback resistor for this op amp is one of the deposited thin film resistors. Figure 8-3 shows how both devices are connected together to form a voltage output multiplying DAC. The digital input word determines the states of all of the bits from the MSB (Most Significant Bit) to the LSB (Least Significant Bit). All of the binary currents gated through logic "1" positioned switches flow through the feedback resistor to the op amp output. Therefore,

$$Eo = -Ioutl * Rfb$$

The current Ioutl is the product of the reference voltage and the digital binary fraction divided by the R-2R ladder input resistance.

$$Ioutl = D * Eref/Zin$$

where

$$D = B1*(1/2) + B2*(1/4) + B3*(1/8) + \ldots BN*(1/2\ expN)$$

B1 thru BN are 1 or 0.

8.3 Test Development

At the time that this report was being written the test development phase was in process, but not complete. Much of the techniques and equipment are the same as that used for the AD562 12-bit D/A Converter (MIL-M-38510/121), reported in Section VII.

One major difference between the multiplying D/A converters and the AD562 is that the former can have a variable reference. Therefore new conditions have to be considered and specified.

A list of parameters which are planned for characterization are identified in Table 8-2.

Table 8-2. *Test Parameters for Characterization.*

Item No	Symbol	Test Parameter
1	Icc	Supply Current
2	Iref	Reference Input Current
3	IIL	Digital Input Leakage Current (logic 0)
4	IIH	Digital Input Leakage Current (logic 1)
5	IZS	Zero Scale Current (IOUT1 at logic 0 input)
6	IZS'	Zero Scale Current (IOUT2 at logic 1 input)
7	VFS	Gain Error (Full Scale)
8	dVFS/dT	Gain Error Drift
9	PSS	Power Supply Sensitivity
10	LE	Linearity Error (End Point)
11	LE(BF)	Linearity Error (Best Fit)
12	MCE	Major Carry Error
13	FTE	Feedthrough Error
14	tSLH	Output Current Settling Time
15	tSHL	Output Current Settling Time
16	Co	Output Capacitance
17	en	Noise (broadband)

Conclusions and Recommendations

Characterization of the CMOS multiplying D/A converters is incomplete at the time that this report is being written. Completion of the characterization effort and the issuance of MIL-M-38510/127 is scheduled for December 1980 under a separate contract.

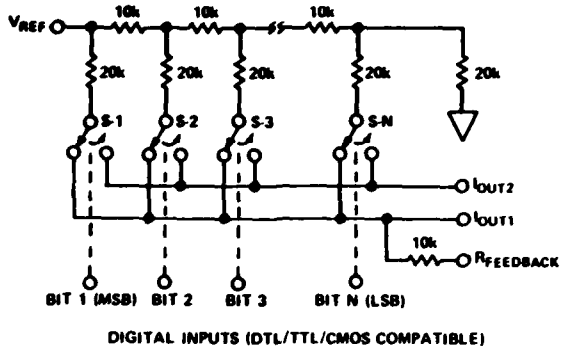

Figure 8-1. CMOS Multiplying DAC Schematic.

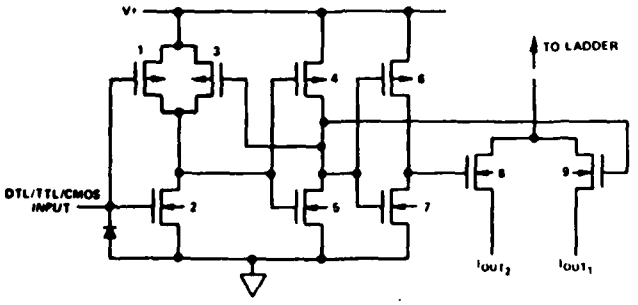

Figure 8-2. CMOS Switch Schematic.

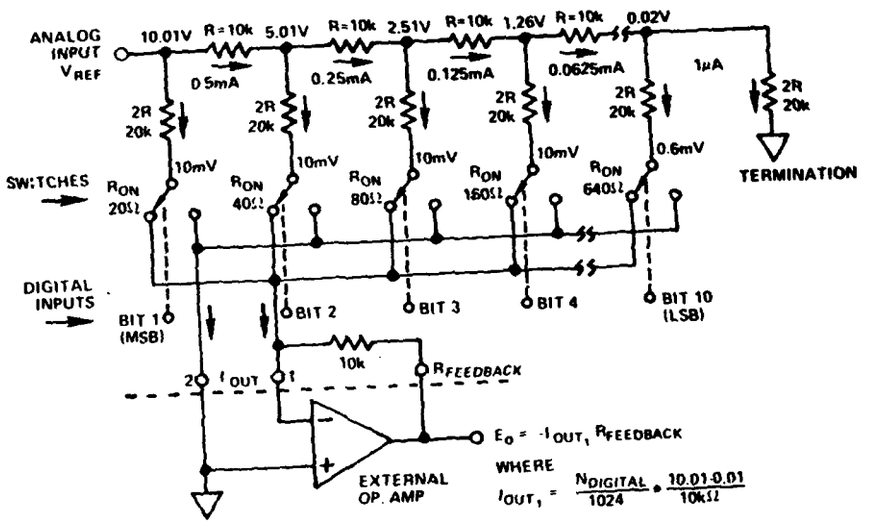

Figure 8-3. Typical Voltage Output Functional Schematic.

SECTION IX

12 BIT A/D CONVERTERS

MIL-M-38510/120

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SECTION IX

12-BIT A/D CONVERTERS

MIL-M-38510/120

9.1 Background and Introduction

This JAN 38510 specification development is the first slash sheet devoted to A/D converters, and the specified devices are the first linear hybrids to be designated for military usage in the JAN program. The need for data converters in military systems is well-established, not only for new microprocessors-based digital systems, but for retrofit into upgraded existing systems.

At this writing, high speed (e.g. 13 usec conversion time) 12-bit A/D converters do not exist as monolithic devices, although lower speed and/or lower resolution monolithics are available from some manufacturers. The hybrid devices selected for this slash sheet are already used in numerous military systems. They were developed by MicroNetworks Corporation, and at least some of the device types will also be available from other hybrid manufacturers . . . Analog Devices and Hybrid Systems. Generally, the devices offer choice of external or internal references, two conversion speed ranges, and four input voltage ranges.

Table 9-1 lists the device types specified for this characterization, along with a brief description.

The characterization effort focuses upon representative device types in each family.

Table 9-1. Device Types Specified.

Device type	Generic type	Input Voltage Range	Ref	Max Conv Time
120-01	MN5200	0 V to -10V	int	50 us
120-02	MN5203	"	ext	50
120-03	MN5201	-5 V to + 5V	int	50
120-04	MN5204	"	ext	50
120-05	MN5202	-10 V to +10V	int	50
120-06	MN5205	"	ext	50
120-07	MN5206	0 V to +10V	int	50
120-08	MN5207	"	ext	50
120-09	MN5210	0 V to -10V	int	13
120-10	MN5213	"	ext	13
120-11	MN5211	-5 V to + 5V	int	13
120-12	MN5214	"	ext	13
120-13	MN5212	-10 V to +10V	int	13
120-14	MN5215	"	ext	13
120-15	MN5216	0 V to +10V	int	13
120-16	MN5217	"	ext	13

9.2 Description of Device Types and Application Information

There are two series of device types included in /120, the Micro Networks MN5200 series and the MN5210 series. In each series there are eight device types, four pair having input voltage ranges of 0 to -10V, -5V to +5V, -10V to +10V, 0 to +10V, with each pair having either an internal or an external reference, as shown in Table 9-1. Both series are 12-bit successive-approximation converters having both serial and parallel digital outputs. They are packaged in miniature 24-pin glass/ceramic DIPs, are self-contained and internally laser-trimmed (no external adjustments). The two series differ only in maximum conversion time . . . the 5200 series (device types 01-08) requiring 50 usec for a complete conversion, and the 5210 series (device types 09-16) requiring 13 usec.

The hybrid devices have several chips; there are significant differences in the number of chips used by different manufacturers varying from about 6 to 35. Basically, the successive approximation converter con-

sists of a D/A converter (ladder network and switches), a successive approximation register and logic, and a comparator. An approximate diagram of the 5200 A/D converter is shown in Figure 9-1, which includes functional level information only, not detailed schematics of any sections. The 12-bit converter must make 12 successive approximations of the applied input voltage. While this is occurring, the input cannot change (unless it were to change so as not to affect previous trials, which is too restrictive), so a sample/hold circuit may be required to hold the input constant during the conversion time. The 12 comparisons are made between the input voltage and a feedback voltage obtained from the internal 12-bit parallel D/A converter, beginning first with the most significant bit (MSB) and ending with the least significant bit (LSB). The comparator output determines whether a "1" or a "0" should be entered in the register for each bit comparison. In the figure, this function is performed with a high-gain precision comparator.

The 25L04 successive approximation register (SAR) used in the Micro Networks device contains most of the digital control and storage necessary to operate the converter. It contains a set of master latches acting as control elements which change state when the external clock input is low, and a set of slave latches that hold the register data and change state on a low-high transition of the input clock. The SAR acts as a serial-to-parallel converter for information from the comparator, sending it to the appropriate slave latch to appear at the register output (serial output) when the clock transition goes from low-to-high. When that data enters the register, the next significant bit is set to a low, ready for the next iteration.

A timing diagram is shown in Figure 9-2. For parallel data outputs, the shaded areas shown denote states determined by data input immediately prior to the shaded area. Parallel data is valid for the entire time that the EOC signal is low, i.e., until the converter is reset. The converter is reset by holding the "start" signal low during a low-to-high transition of the clock, beginning at least 25 nsec prior to the clock transition. When the start is again set high, the conversion will begin on the next low-to-high clock transition. The start signal can be set low at any time during a conversion and it will reset the converter. A complete conversion takes place in 13 clock pulses. For continuous operation, the user has to connect "start convert" to EOC, pin 1 to pin 22. The ground terminals must be externally connected together as close as possible to the device.

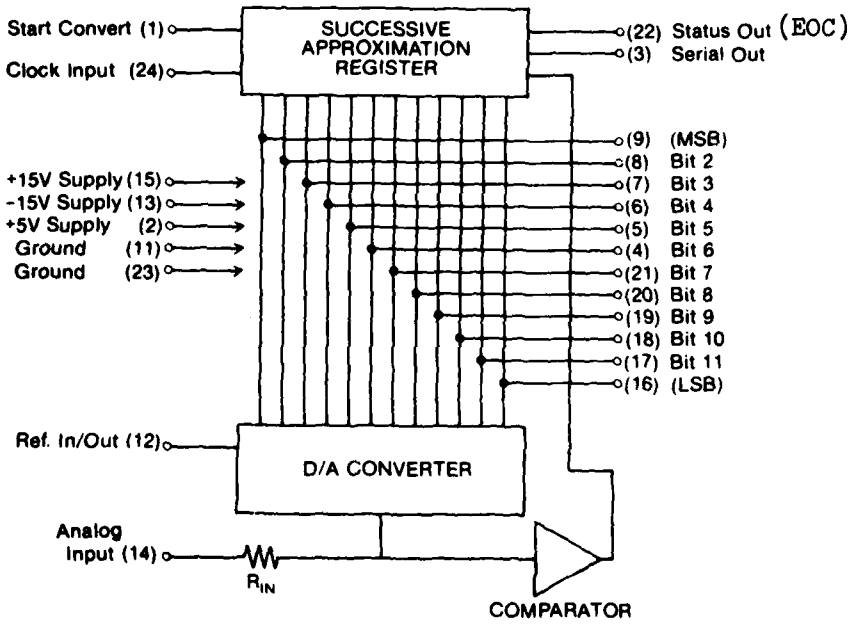
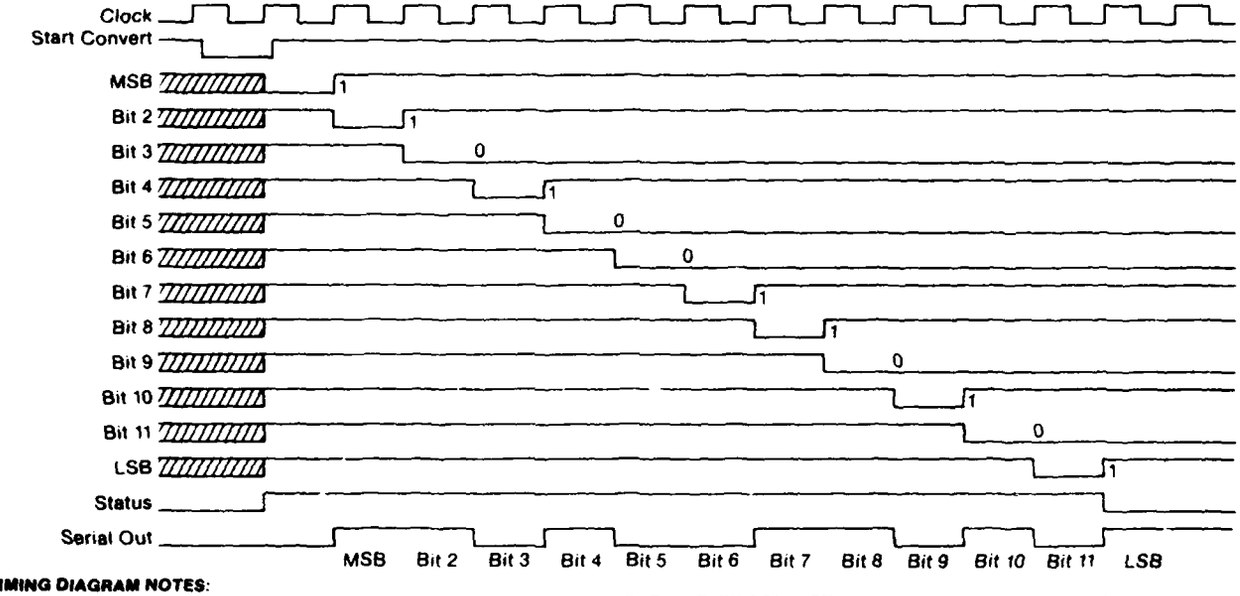


Figure 9-1 Block Diagram of 5200/5210 A/D Converter

TIMING DIAGRAM



TIMING DIAGRAM NOTES:

1. Operation shown is for the digital word 1101 0011 0101 which corresponds to 1.7432V on the 0 to +10V input range (MN5206). See Output Coding.
2. Conversion time is defined as the width of the STATUS (E.O.C.) pulse.
3. The converter is reset (MSB = "0", all other bits = "1", STATUS = "1") by holding the START CONVERT low during a low to high clock transition. The START CONVERT must be low for a minimum of 25 nSec prior to the clock transition. Holding the START low will hold the converter in the reset state. Actual conversion will begin on the next rising clock edge after the START has returned high.
4. The delay between the resetting clock edge and STATUS actually rising to a "1" is 120 nSec maximum.
5. The START CONVERT may be brought low at any time during a conversion to reset and begin converting again.
6. Both serial and parallel data bits become valid on the same rising clock edges. Serial data is valid on subsequent falling clock edges, and these edges can be used to clock serial data into receiving registers.
7. Output data will be valid 30 nSec (maximum) after the STATUS (E.O.C.) output has returned low. Parallel output data will remain valid and the STATUS output low until another conversion is initiated.
8. For continuous conversion, connect the STATUS output (Pin 22) to the START CONVERT input (Pin 1). See section on Continuous Conversion.
9. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

Figure 9-2 Timing Diagram for 5200/5210 Series A/D Converter

An op Amp (not shown) buffers the input reference voltage and provides the base line voltage to all switching transistors. sistors. The base line voltage varies to compensate for the variation in the switching transistor V_{BE}'s with temperature, thereby providing a constant voltage to the ladder resistors. Similar compensation exists for variations in the minus supply voltage, which would change ladder currents.

It should be noted that the 5210 series of devices manufactured by Micro Networks require a 2.2 uF solid tantalum capacitor connected between pins 15 and 10 for operation with conversion times of 24 usecs or less.

The user should be aware that there are differences in the supply currents among vendors, and also differences in power supply sensitivity. The specification tolerances have essentially been widened to accommodate both vendors. Proper system design considerations by the user will permit interchangeability by using the specified limits. Tighter performance may be obtained from a single vendor on power supply sensitivity, but this is not guaranteed or controlled within the spec, except as stated.

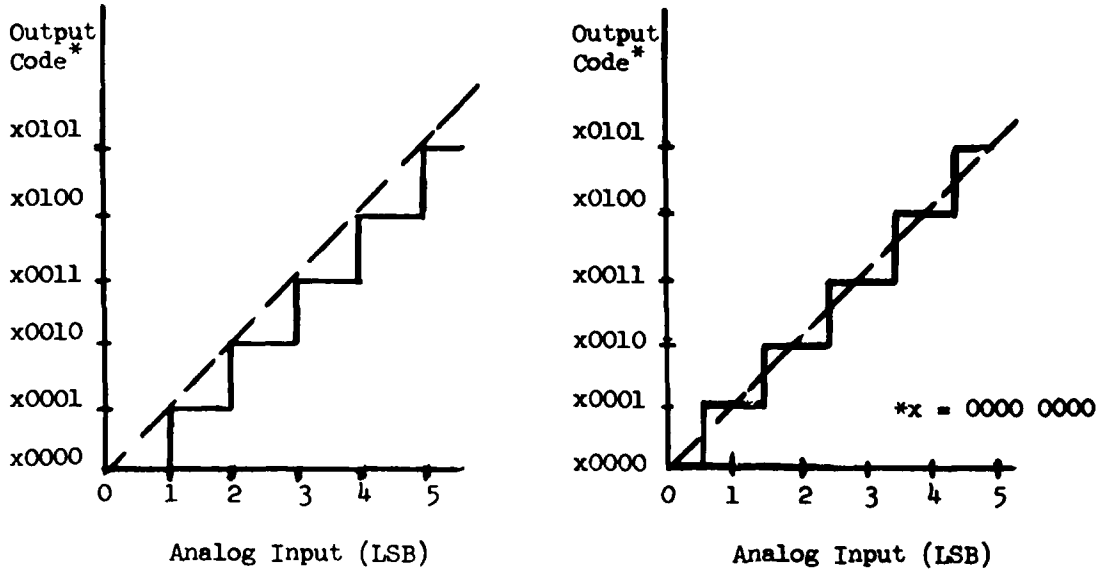
Two approaches to input quantization are illustrated in Figure 9-3, for a unipolar converter. The internal comparator can be offset by the manufacturer, such that the first transition occurs at either 1/2 LSB or at 1.0 LSB. Originally, there was not full agreement among the vendors regarding the preferred approach. It is now believed that all vendors will follow the Micro Networks approach, setting the first transition at 1.0 LSB.

9.3 Discussion of A/D Converter Parameters

A brief discussion of A/D converter parameters and characteristics is offered in this section as a preface to the discussions on test development which follows. The comments are not intended to be definitions.

Quantization Error

A 12-bit D/A converter could theoretically be super-accurate, since for a particular input code it could have a near-perfect output voltage or current. However, an A/D converter's accuracy is basically limited by its resolution and inherent quantization band. For a particular output code, there can be a host of values of analog input voltage which satisfy that particular output code. A study of figure 9-3 illustrates this point (either graph). Actually, a perfect A/D converter (ADC) has an inherent error of ± 1/2 LSB due to this quantization effect.

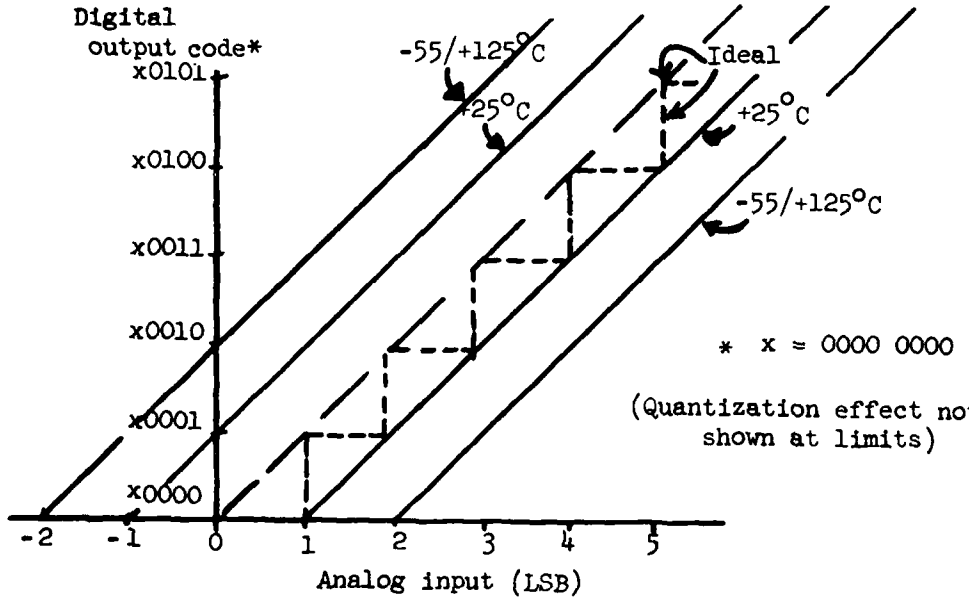


Note: Straight binary code assumed for illustration; MN 5200/5210 family has complementary binary coding.

Figure 9-3. Two Approaches to Ideal Quantization, Unipolar Mode.

Zero Error

Consider a 12 bit ADC operating in the unipolar mode (one polarity only of input voltage), e.g., a 0 to + 10V input range. The first output transition (from code 0000 0000 0000 to 0000 0000 0001) theoretically occurs at an input level of + 1/2 LSB or + 1.0LSB, depending on the manufacturer's design. (For 12 bits, 1 LSB = 2.44mV). The difference between the actual input voltage and the theoretical input voltage is the offset error. It will affect all other codes the same way, so that its effect can be subtracted out or otherwise corrected for. However, it will vary somewhat with temperature. For the MN5200, for example, the 25°C spec is ± 2.5mV, and at -55°C/+125°C the spec is ± 5.0mV. These concepts are illustrated in figure 9-4.



Note: Straight binary code assumed for illustration; MN 5200/5210 family has complementary binary coding.

Figure 9-4. Zero error tolerances.

For bipolar converters, or a range such as + 10V to 0, the concept of offset is not as clear, and most manufacturers therefore prefer to use the term "zero error". Depending upon the configuration and how the converter is trimmed, zero error can actually include one-half or all of the gain error tolerance. This complication need not be further pursued now if the discussion is confined to the 0 to + 10V unipolar converter originally assumed.

Gain Error

The gain of an ideal A/D converter is the slope of its transfer function, a straight line drawn from the origin to the full scale point (unipolar assumption again). In a real converter, having corrected for offset or zero error, the error occurring at full scale is a measure of the gain error, expressed in %F.S. usually. Thus the gain error at midpoint would be half the F.S. magnitude; other codes are similarly affected proportionately. One must realize that the full scale ideal input voltage for the assumed converter is not 10.0000V at full scale, but rather 10.0000V minus 0.00244V. In locating the transition for the final bit change to full scale, the ideal converter's transition would occur either 3/2LSB or 1 LSB away from full scale, depending upon the manufacturer trim (see Figure 9-3).

Gain error also changes with temperature, more so than offset does, so that a perfect converter which is very linear at one temperature, may appear quite non-linear during a temperature change.

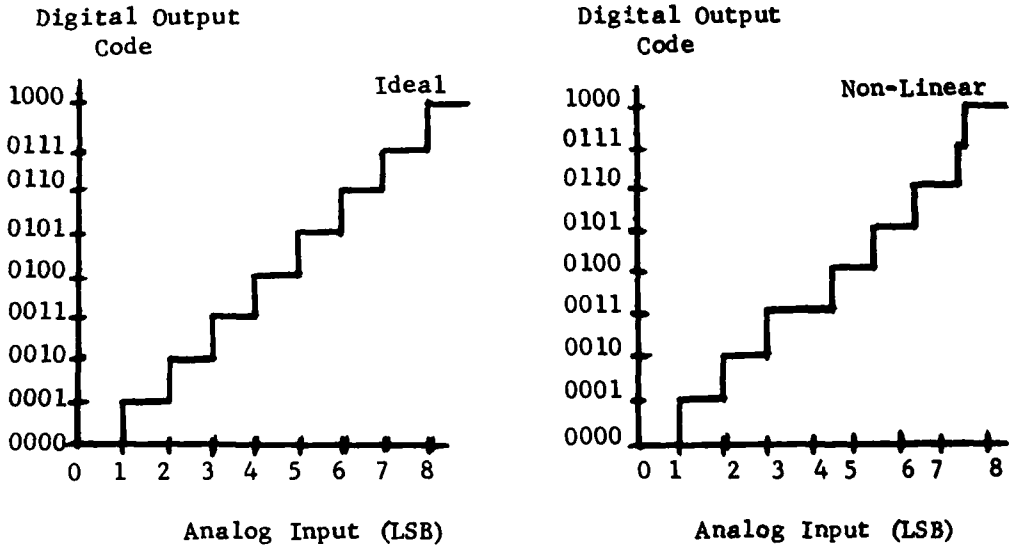
Gain error will change if the power supply voltages change, in accordance with the "Power Supply Rejection" specification. For example, some device types can vary as much as ± .05% for a 1% change in power supply level. (The maximum change usually occurs with that supply from which the internal reference is derived. The operating conditions in the slash sheet limit analog supply variations to ± 3%.)

Absolute Accuracy

Absolute accuracy defines the total error of the A/D converter at a stated digital code (often full scale) relative to an absolute standard. It includes quantization error, offset error, gain error, linearity error, and noise.

Linearity

For an A/D converter, the integral linearity (often called "linearity") is a measure of the deviation of a plot of the transition voltages from a given straight line. The given straight line is usually drawn between zero and actual full scale, but sometimes is drawn between zero and the best fit straight line to a plot of actual data points. The latter approach is difficult to communicate from vendor to user, so the end point definition is strongly preferred by GE. Figure 9-5 shows an example of a non-linear transfer function compared to an ideal transfer function. The ideal straight line could be drawn through the midpoints of a step, or through the transition points. Micro Networks chose to do the latter, consistent with their quantization approach, whereas Analog Devices chose the midpoint approach, also consistent with their quantization definition. Integral linearity is usually expressed as an error term, i.e., the deviation from a straight line, measured in LSBs, or in percent full scale. For the 5200/5210 A/D converters, the integral linearity error limit is ± 1/2 LSB over the military temperature range.



Note: Straight binary code assumed for illustration; MN 5200/5210 family has complementary binary coding.

Figure 9-5. Examples of Linear and Non-linear Performance.

Differential linearity

The differential linearity of an A/D converter is essentially a measure of the width of the input voltage steps in the linearity plot. The height of the steps is uniform since they are digital code transitions, but the range of analog input voltage for that code could be very narrow, or relatively wide, depending upon the degree of differential linearity.

Noise

Noise originating in the device under test, in the test circuit, or in the wiring, has the effect of creating a degree of uncertainty in the output code transitions. Figure 9-6 is an example of transition uncertainty due to noise.

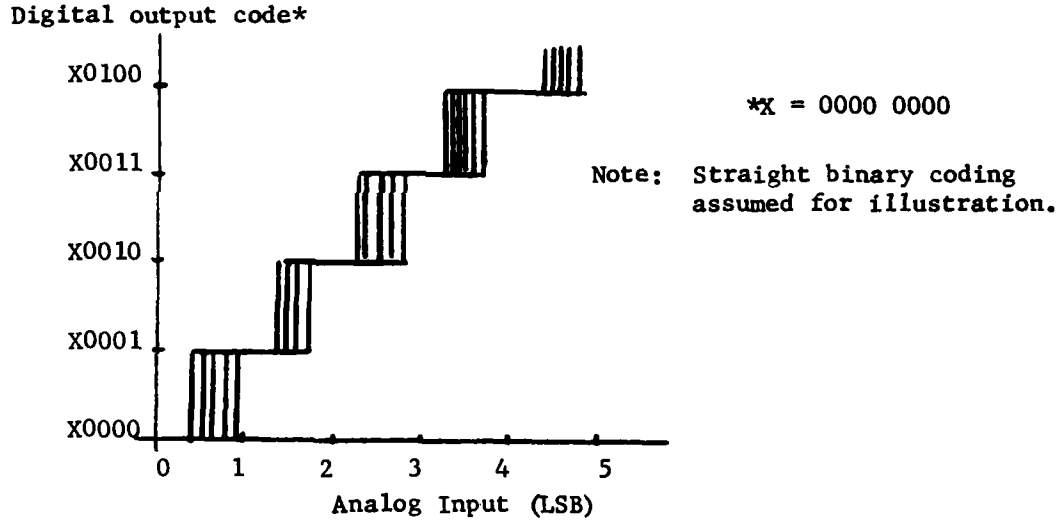


Figure 9-6. Transition uncertainty due to noise.

Monotonicity

The output of a monotonic A/D converter never decreases in response to an increasing input. A converter that is monotonic must have a differential linearity error less than ± 1 LSB. An A/D converter output might jump over a code, or might have the proper code only over such a narrow range of input as to be unusable. (Integrating converters are inherently monotonic, but successive approximation converters can be non-monotonic, especially over a wide temperature range such as -55°C to +125°C.) The 5200/5210 converter is not tested for monotonicity at all codes, nor for differential linearity at all codes, but it is tested for differential linearity at the major carries, the points where non-monotonicity is most likely to occur. Excessive noise can also cause non-monotonic behavior at any code.

Conversion Time

The time required for a converter to perform a single conversion is the conversion time. Depending upon how the END-OF-CONVERT or STATUS signal is handled, some additional delay may be required before valid data can be latched into a register. The relationship of the START signal relative to clock also requires care in its use.

Conversion time is a function of the settling time of the internal DAC; if the DAC does not fully settle within the required accuracy, transistion voltages will be affected, and non-monotonic behavior can result.

Test Parameters, MIL-M-38510/120 - Table I

The test parameters developed for MIL-M-38510/120 are discussed in the following. Table I of /120 is contained in this section as Table 9-2

Power Supply Currents

The power supply current limits were established to encompass all device manufacturers designs. The power requirements are:

	+15V	-15V	5V
Micro Networks	28mA	19*mA	42mA
Analog Devices	?(low)	35mA	?
Hybrid Systems	16	28	51

*6.3 mA for external reference devices only.

In order to allow all vendors to supply the devices, the maximum limits for each supply were adopted. However, a power dissipation spec of 1 watt maximum was added to limit total power. Power dissipation is calculated from the equation:

$$P_D = V_{cc}\ I_{cc} + V_{EE}\ I_{EE} + V_{LOG}\ I_{LOG} + V_{REF}\ I_{REF}*$$

*For external reference devices only.

Input Logic Voltage Levels

Logic "1" input voltage levels is + 2 V minimum and Logic "0" input voltage levels is +9.8 V maximum, typical digital logic levels. Inputs are: S.C. and Clock.

Output Logic Voltage Levels

Output logic "1" voltage is 2.4 V minimum when loaded with 320 uA (source). Output logic "0" voltage is 0.4 V maximum loaded with 3.2 mA (sink). Outputs are: 12 address outputs E.O.C., and SDO.

Output Short Circuit Current

All outputs are tested with a short circuit applied. Output current shall not exceed - 25mA.

Input Low Current

Input low current is the maximum sink current the device will sink with the input at 0 V.

Input High Current

Input high current is the maximum current the device will source with the input voltage at + 5 V.

Clock Input Pulse Width

Minimum clock input pulse width is specified as 200 ns. The positive (logic 1) portion of the clock pulse must be equal to or greater than 200 ns wide for all device types.

Conversion Time

The maximum value of conversion time represents the conversion speed which the device must be capable of at rated accuracy. There are two groups of converters in /120 which differ only in conversion time: device types 01-08 can convert in 50 us or less, and device types 09-16 can convert in 13 us or less.

Input Resistance

The input resistance of the analog input is different for each manufacturer, as shown in the following:

Device Type	Analog Devices	Micro Networks	Hybrid Systems	Units
01-04, 07-12, 15, 16	5.0±25%	6.7±5%	3.3±?	K Ω
05, 06, 13, 14	13±25%	10±5%		K Ω

Power Supply Sensitivity

A comparison of the power supply sensitivity specification is shown in the following tables:

External ref devices:

Power Supply	Micro Networks	Analog Devices	Hybrid Systems
+ 15V	± 0.05 %/%	± 0.02 %/%	-
- 15V	± 0.05	0.02	-

Internal ref devices:

Power Supply	Micro Networks	Analog Devices	Hybrid Systems
+ 15V	± 0.05 %/%	0.02 %/%	
- 15V	± 0.10	0.05	

Table 9-2 Device Specifications

Characterizations	Symbol	Conditions/Remarks	Device Types 01 - 13 Limits MIN	MAX	Units
Resolution		The device shall exhibit no missing codes		12	BITS
Power Supply Current from V_{CC}	I_{CC}		3	28	mA
Power Supply Current from V_{EE}	I_{EE}		-35	-1	mA
Power Supply Current from V_{LOG}	I_{LOG}		1	42	mA
Ref. Input	I_{REF}	Device Types with External Ref. Only - 02, 04, 06, 08, 10, 12, 14, 16	0.1	2	mA
Power Dissipation	P_D	Device Types - 02, 04, 06, 08, 10, 12, 16 Device Types - 01, 03, 05, 07, 09, 11, 13, 15		0.8 1	w w
Input Logic Voltage Levels Logic "1" Logic "0"	 V_{IH} V_{IL}		 2	 0.8	 V V
Output Logic Voltage Levels Logic "1" Logic "0"	 V_{OH} V_{OL}	 I_L = 320 uA I_L = 3.2 mA	 2.4	 0.4	 V V
Input Low Current	I_{IL}	V_{IN} = 0 V (digital inputs)		-.6	mA

Table 9-2 Device Specifications (Cont.)

Characterizations	Symbol	Conditions/Remarks	Device Types 01 - 13 Limits MIN	MAX	Units
Input High Current	I_{IH}	V_{IN} = + 5 V (digital inputs)		40	uA
Output Short Circuit Current	I_{OSC}	T_A = +25°C, V_{IN} = + 10.5 V	-25	0	mA
Input Impedance	Z_I	Device Types - 01 to 04, 07 to 12, 15, 16 Device Types - 05, 06, 13, 14	3.5 7.0	10 20	kΩ kΩ
Conversion Time	t_{CT}	Device Types - 01-08 Device Types - 09-16		50 13	us us
Propagation Delay	t_{PHL}	Clock to Status Out Clock to Serial Out			
	t_{PLH}	Clock to Status Out Clock to Serial Out			
Clock Input Pulse Width	CPW		200		ns
Power Supply Sensitivity V_{CC}	PSS1	Device Types - 01,03,05,07,09,11,13,15 Device Types - 02,04,06,08,10,12,14,16		±.02 ±.02	%FSR/ %P.S. %FSR/ %P.S.
Power Supply Sensitivity V_{EE}	PSS2	Device Types - 01,03,05,07,09,11,13,15 Device Types - 02,04,06,08,10,12,14,16		±.05 ±.02	%FSR/ %P.S. %FSR/ %P.S.
Power Supply Sensitivity V_{LOG}	PSS3	Device Types - 01,03,05,07,09,11,13,15 Device Types - 02,04,06,08,10,12,14,16		±.02 ±.02	%FSR/ %P.S. %FSR/ %P.S.

Table 9-2 Device Specifications (Cont.)

Characterizations	Symbol	Conditions/Remarks	Device Types 01 - 13 Limits MIN	Device Types 01 - 13 Limits MAX	Units
Zero Error	V_{IO}	V_{CC} = + 15 V ± .015 V V_{EE} = -15 V ± .015 V		2	LSB
Bipolar Offset Error	BPOE	V_{CC} = + 15 V ± .015V V_{EE} = -15 V ± .015V			
Absolute Accuracy " "	V_{FSE}	V_{CC} = + 15 V ± .015 V Ext. Ref. V_{EE} = - 15 V ± .015 V Int. Ref.		±.1 ±.4	%FSVR
Bit Transition Linearity Error	LE	V_{CC} = + 15 V ± .015 V V_{EE} = - 15 V ± .015 V		±1/2	LSB
Major Carry Errors	MCE	$Bit(2^n-2) - Bit(2^n-3)$ for n=12 $Bit(2^n-1) - Bit(2^n-2)$ for n=1 to 11 $Bit(2^n) - Bit(2n-1)$ for n=0 to 11		±1	LSB
Noise	No			1/4	LSB

9.4 Test Development

Automatic testing of high resolution data converters (12 bits or more) is a new technology, implemented by very few users and manufacturers at this time. In particular, characterization testing of 12-bit A/D converters is complex, for several reasons:

- o The quantity of data required to absolutely verify performance is staggering (approximately 100,000 data points are needed to verify linearity and differential linearity at all codes, at two conversion frequencies, at two supply voltages, and at three temperatures, for one device).

- o Unlike many D/A converters, A/D converters are not particularly well-behaved, and superposition errors tend to negate the validity of abbrevated testing (for characterization, at least).

- o Noise, from the test system, the test circuit, and the test device itself, interferes with the required precise measurement of the analog input at output code transitions. Filtering or statistical averaging is usually required to minimize the effects of noise. Wiring and grounding noise is difficult to eliminate in circuits which employ both digital and analog signals.

- o Measurement of precise analog signals (0.1 LSB = 0.0024% for a 12-bit converter) requires sophisticated instruments and relatively long settling times to obtain valid data.

Several phases of testing MN5200 A/D Converters have been pursued at Ordnance Systems. These include:

1. Automatic test of static parameters and logic signals using S3260/70 static test adapter.

2. Bench test of linearity and associated parameters using test box simulating original automatic test techniques.

3. Bench test of linearity using cross-plot method.

4. 53260/70 automatic test of linearity using open loop direct approach.

5. 53260/70 automatic test of linearity using closed loop dither approach.

Each of these test approaches are discussed in this section but the focus is on automatic test of linearity, method 5.

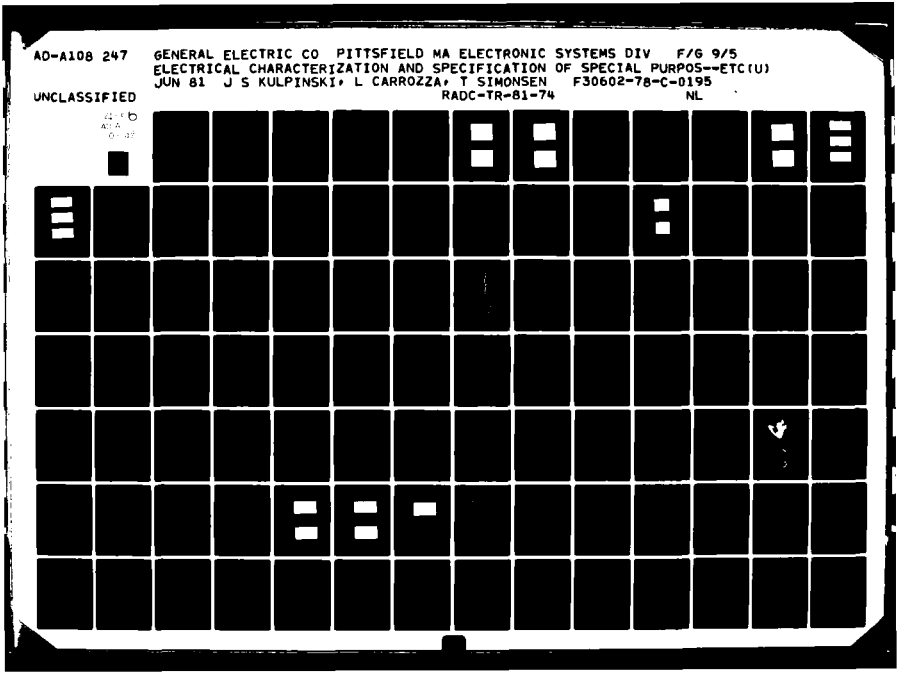
Method #1 - Automatic test of static parameters

Many of the A/D converter parameters are not particularly difficult to test. For example, parameters such as gain, offset, supply drain, supply sensitivity, and standard logic tests, are in this category. Since linearity testing requires complex test circuitry, it is desirable to devote one test circuit to linearity exclusively, and another test circuit to all other parameters. This approach minimizes the complexity of the linearity test circuit with the accompanying benefits to layout, wiring, and grounding.

A test adapter was developed for S3260/70 test of the A/D digital inputs and outputs, as well as other static parameters; Table 9-3 lists the parameters tested. Measurements of all voltage and current parameters was straightforward - force current/measure voltage or force voltage/measure current. The transition and propagation time measurements were performed while the outputs were loaded with the circuit illustrated in Figure 9-7.

Two functional tests were also performed - "start convert" pulse width check and serial output to parallel output check. The first verified that the device converted properly with worst case timing on the "start convert" input. The second test stored the serial output as the device converted and compared it to the parallel output when the conversion was completed.

AD-A108 247 GENERAL ELECTRIC CO PITTSFIELD MA ELECTRONIC SYSTEMS DIV F/G 9/5
ELECTRICAL CHARACTERIZATION AND SPECIFICATION OF SPECIAL PURPOS--ETC(U)
JUN 81 J S KULPINSKI, L CARROZZA, T SIMONSEN F30602-78-C-0195
UNCLASSIFIED RADC-TR-81-74 NL



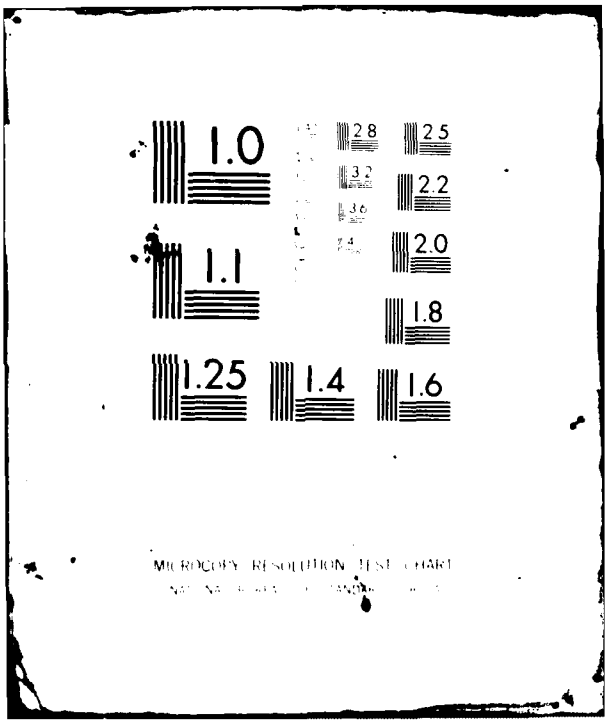

1.0
1.1
1.25
1.4
1.6
2.0
1.8
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART

Table 9-3. Static test parameters for characterization.

Symbol	Parameter	Notes
I_{OS}	Output short circuit current	Test each of 12 bits plus "E.O.C.", "SO"
I_{ICL}	Input clamp current	Test "start convert" and clock
V_{OH}, V_{OL}	Output logic voltage levels	Test each of 12 bits plus "EOC", "SO"
I_{IH}, I_{IL}	Input logic current	Test "start convert" and clock
I_{cc}	Supply current drain	Test 3 supplies
t_{TLH}, t_{THL}	Large transition times	Test each of 12 bits plus "EOC", "SO"
t_{PLH}, t_{PHL}	Logic propagation delays	Clock to each bit, to EOC, to SO.
	Start convert pulse check	Verify conversion with min pulse width
	Serial to parallel check	Verify SO = D1-----D12.

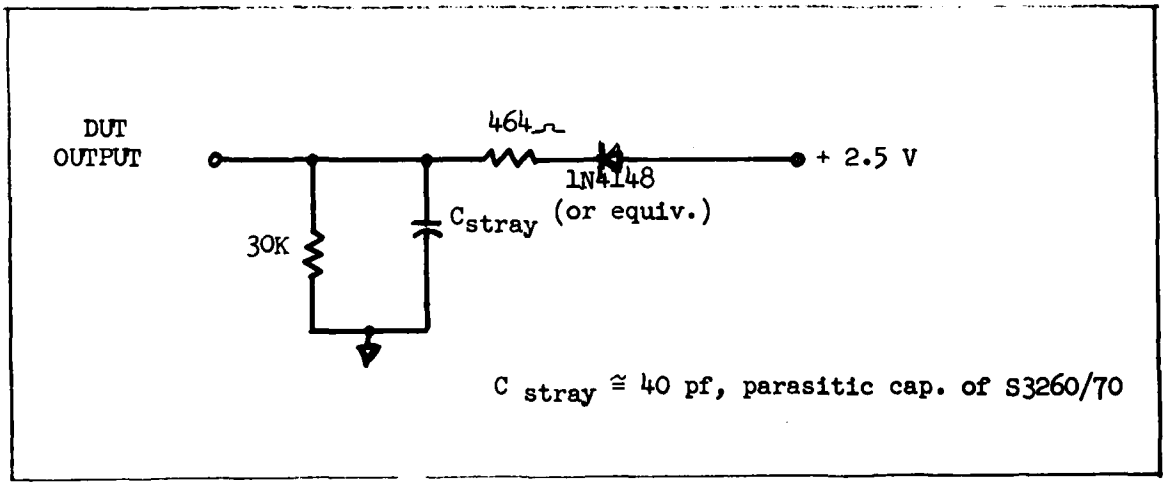


Figure 9-7 A/D Converter Load Circuit

Method #2 - Bench Test of Linearity

In the early phase of this A/D test development program, a bench test box setup was developed to proof out an analog comparison/dither technique for measuring A/D linearity errors. Other dither methods were later refined to those described in Method #5, and the bench test box proofing of the now-obsolete approach was abandoned. It is summarized here for completness in presenting the total test development effort.

Figure 9-8 shows a simplified block diagram of the test circuit developed for linearity testing. The transition to be tested minus 1 LSB is entered into the A_n register, where it is applied to the reference DAC and a digital comparator. The digital comparator's other input comes from the device under test, the 12 bit A/D converter. The latch inserted between the DUT and the digital comparator ensures that only valid data is applied to the comparators, i.e. it is strobed when an end-of-convert signal is received from the ADC.

The digital comparator has 3 possible outputs, $A < B$, $A = B$, or $A > B$ depending on the relative magnitude of the transition to be tested and the present state of the A/D converter. If $A < B$, the input to an integrator is connected to + 5 volts through an analog switch. This causes the integrator to ramp downwards. The output of the integrator is summed with the analog output of the reference DAC. Since the DAC output is a constant DC level and the integrator's output is decreasing, their inverted sum is rising, which forms the analog input to the DUT. The DUT input voltage will continue to increase and its digital output word will continue to decrease until the digital comparator decides that $A = B$ or $A > B$. When this happens, the analog switch changes state, connecting -5 volts to the input of the integrator. This causes the output of the integrator to ramp upwards. When summed with the DAC output, this forces the DUT input voltage to decrease, which increases its digital output word.

In this way it can be seen that the DUT digital output word locks onto the word present in the A_n register, and cycles between $A < B$ and $A \geq B$, at the DUT input transition voltage.

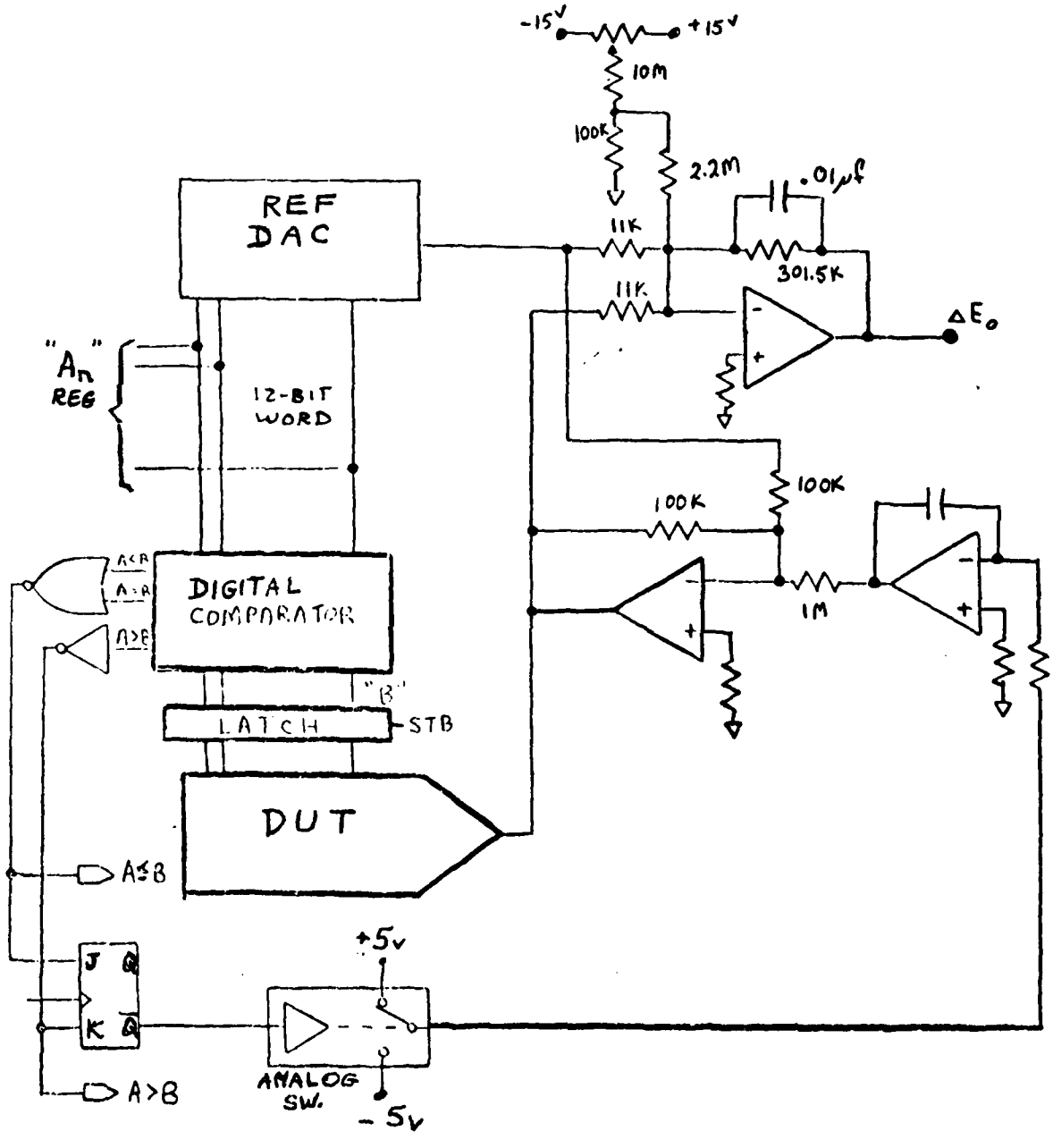


Figure 9-8 Block Diagram of Test Circuit, Method # 2

Method #3 - Cross-plot Test Method

One of the first test circuits developed in industry for testing bit accuracy of A/D converters is the cross-plot test method. A functional block diagram of this circuit is shown in Figure 9-9.

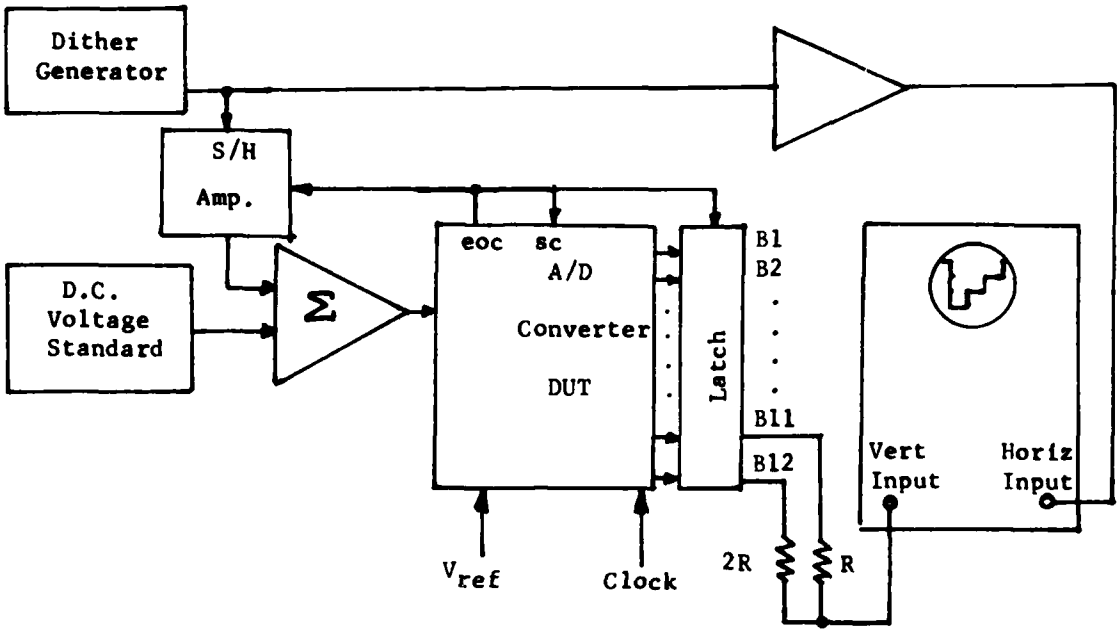


Figure 9-9 Block Diagram for Crossplot Test Circuit

All cross-plot test methods use a voltage dither on the input signal and an oscilloscope to display the converter output. In the test circuit shown in Figure 9-9, the input voltage to the DUT is the summation of the voltages obtained from a d.c. voltage standard and from a dither voltage generator. The dither voltage serves two important functions. First, the dither, when summed with the D.C. voltage standard output, causes the input voltage to vary about the fixed d.c. level. Secondly, the dither is amplified, applied to the horizontal input to the oscilloscope and controls the horizontal sweep so that the sweep is in exact time, phase and amplitude synchronism with the varying input signal to the DUT. Thus, as long as the average value of the dither is zero and the peak amplitudes remain constant, and as long as the slope of the dither is less than 0.1 LSB/conversion, the display seen on the oscilloscope will remain unchanged irrespective of the shape of the dither - the dither signal may be sinusoidal, triangular or sawtooth.

Sawtooth dithers used by GEOS for cross-plot testing are shown in Figures 9-10 and 9-11. The sample/hold circuit between the dither generator and the summing amplifier maintains a stable voltage at the DUT input during conversion. The voltage amplitude of the dither is sampled when the status signal is low.

The output to the oscilloscope from the DUT is derived from output bits B11 and B12 - the two least significant bits. Either or both of these outputs may be a logic "0" or a logic "1"; therefore the vertical input to the oscilloscope can have four possible voltage levels - 0 V, 1/3 V, 2/3 V and 1V when the DUT outputs are 00, 01, 10 and 11, respectively. When the dither signal has the equivalent peak-to-peak voltage of 8 LSB, two four-level staircases are displayed on the oscilloscope. When the oscilloscope is properly adjusted the vertical centerline represents the average value of the signal at the DUT input. The vertical voltage at the centerline defines the state of the DUT's 2 LSB's when the dither voltage is zero. Figure 9-12 shows the oscilloscope display obtained with a well behaved A/D converter. The staircases can be moved left or right by varying the d.c. voltage standard output. In this way precise measurements can be made of the input and output signal.

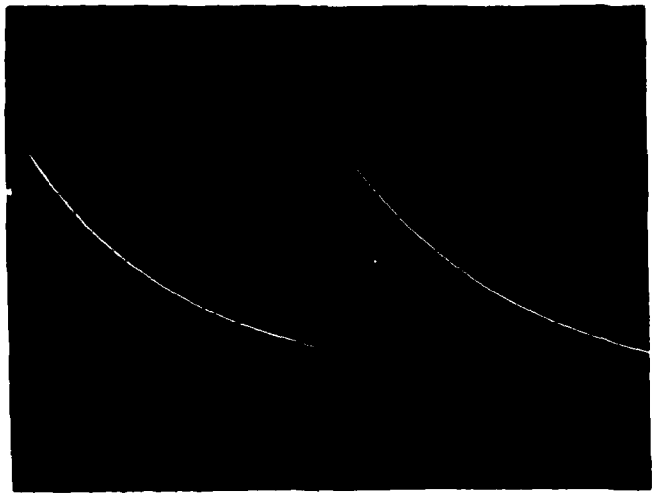
Incorporation of a positive slope and a negative slope dither voltage demonstrates hystersis operation of the A/D Converter. The oscillographs in Figure 9-12 and 9-13, respectively, demonstrate the behavior of the A/D Converter with a negative slope dither and with a positive slope dither.

The differences shown in Figures 9-12 and 9-13 can be explained as follows and by referring to Figure 9-1. In the 5200 and 5210 series converters, the current that flows through the DAC switches comes from the +15 Vdc supply. When a current switch is turned on, a positive current flows through the switch and a R-2R ladder network to a voltage comparator. A positive voltage applied to the input of the A/D Converter results in a current out of the DAC that drives the comparator input voltage to zero. Conversely, if the DAC output has a negative offset, the offset must be compensated for by a positive voltage at the converter input, resulting in an apparent positive input offset condition.

Figure 9-13 shows the operation of an A/D converter with a positive slope sawtooth dither. In this figure, the center line of the oscilloscope represents the mid-point of the converters range. The full output code-word from the converter is 1000 0000 0000. Also, the oscilloscope sweep moves from right to left. In Figure 9-12, the code-word, at this point, is 0111 1111 1111, and the oscilloscope

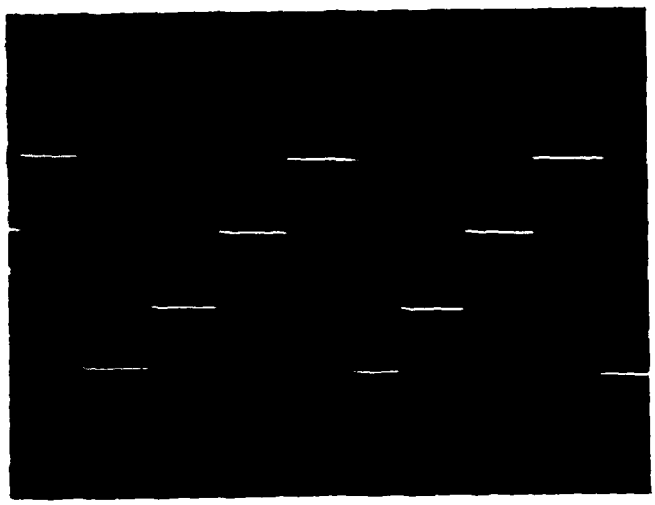
fo = 20 Hz

Figure 9-10 Sawtooth Dither With Positive Slope



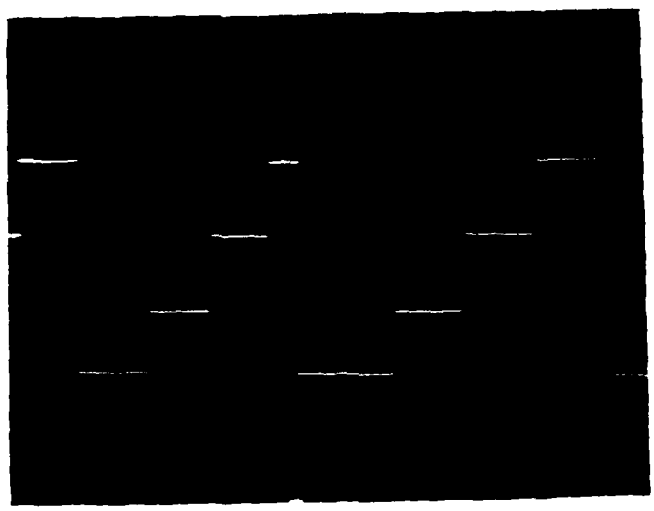
fo = 20Hz

Figure 9-11. Sawtooth Dither With Negative Slope



DUT = 5215 f_{CL} = 162 KHz

Figure 9-12. DUT Output at Mid-range With an Input Negative Slope Sawtooth Dither



DUT - 5215 f_{CL} = 162KHz

Figure 9-13. DUT Output At Mid-range With an Input Positive Slope Sawtooth Dither

sweep moves from left to right. Consider the operation, shown in Figure 9-13, of the converter as the sweep moves past the center line to the left. At this point, the converter output should have changed from 1000 0000 0000 to 0111 1111 1111, since the input voltage has changed polarity. As described previously, a negative offset from the DAC will result in a positive offset at the input.

Since this offset is not constant, it must be developed by some internal dynamic condition that changes as the polarity of the dither slope changes.

The current switches used in the DAC are bipolar transistors. Assume, that the turn off times of the transistors are faster than the turn on times. Also in the 5200 and 5210 series of converters, the transistors are turned off when the output bits are "1". Thus, as the output code-word changes from 1000 0000 0000 to 0111 1111 1111, the MSB transistor turns on after the other transistors turn off and an interim state exists where all switches are momentarily turned off. This will result in a large negative output "glitch" from the DAC, and until the glitch settles to zero, a positive voltage will be required at the input of the converter for a zero condition at the comparator input. Therefore, the transition between 1000 0000 0000 and 0111 1111 1111 moves to the left (+) because of the negative glitch. The following table shows the conditions that exist during a new conversion with a prior code-word of 1000 0000 0000.

Converter Operating Conditon	Switch Condition
Prior code-word condition ($\lessdot$ mid-range)	1000 0000 0000
Interim condition	1111 1111 1111 (major negative glitch)
Reset condition	0111 1111 1111
Interim condition	1111 1111 1111 (glitch not settled to zero)
MSB decision	- - - (decision based on negative input to comparator)
Interim condition	1011 1111 1111 (no glitch)

Converter Operating Condition	Switch Condition
Bit 2 decision	- - -
Bit 2 output condition	1001 1111 1111
---- Continued operation ----	
Bit 12 output condition	1001 0000 0000

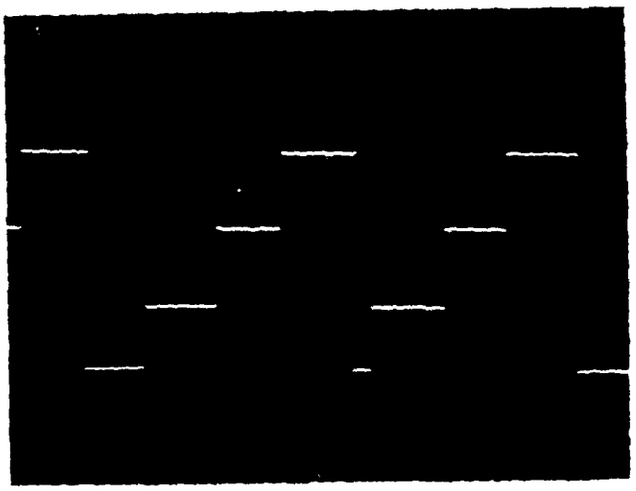
Note: Interim conditions do not actually appear at the output of the DUT.

When the sawtooth dither is negative, there is no glitch generated as the converter switches from the prior code-word 0111 1111 1111 to the reset code-word 0111 1111 1111. Since the switches are unchanged during this transition, the A/D converter is well behaved at the major transition as the input voltage crosses the mid-range voltage level from + to -.

The following table shows the conditions that exist during a new conversion with a prior code-word of 0111 1111 1111.

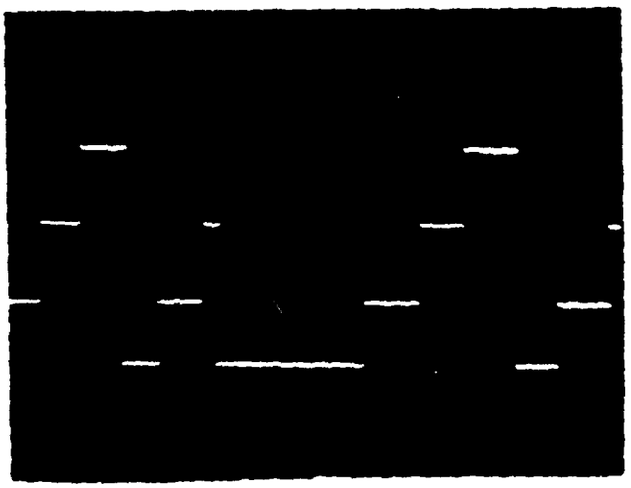
Converter Output Condition	Switch Conditions	
Prior code-word condition (> mid-range)	0111 1111 1111	
Interim condition	0111 1111 1111	(No glitch)
Reset condition	0111 1111 1111	
Interim condition	0111 1111 1111	(No glitch)
MSB decision	- - -	(Decision based on negative input to comparator)
MSB output condition	1011 1111 1111	
Interim condition	1011 1111 1111	(No glitch)
Bit 2 decision	- - -	
Bit 2 output conditon	1011 1111 1111	
---- Continued Operation ----		
Bit 12 output condition	1000 000 000	

The cross-plot technique can be used to measure a) bit accuracy, b) bit linearity error, c) differential non-linearity, d) zero error, e)absolute accuracy, f) transition noise, g) hysteresis, h) missing codes and i) monotonicity. Figures 9-14 through 9-17 show some of the displays obtained using the cross-plot measurement techniques. Although the cross-plot techniques provide excellent test capability, they are slow, require a skilled technician and the results are prone to subjective interpretation.



DUT - 5215 f_{CL} ≈ 162 KHz

Figure 9-14. DUT Output at Mid-range showing Narrow Step Width for Code-word 1000 0000 0000.



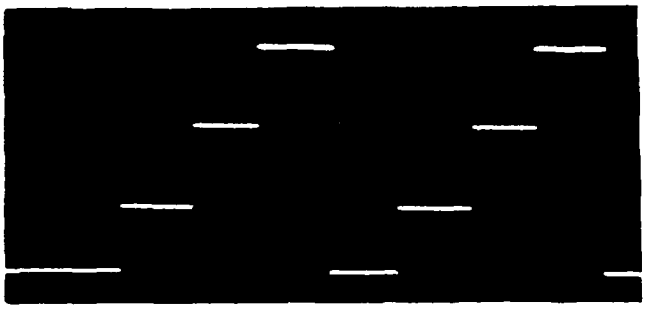
DUT - 5215 f_{CL} = 162 KHz

Figure 9-15. DUT output at Mid-range Showing Missing Code Word 0111 1111 1111.

(V_{CC} set to + 14.5 V)

a) V_{ee} = - 15.25 V

b) V_{ee} - -15.0 V



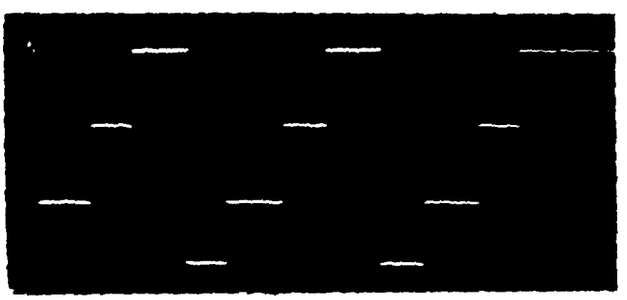
c) V_{ee} = -15.75 V

DUT = 5215 , f_{CL} - 162 KHz, V_{in} = + 10 V

Figure 9-16. DUT Output Showing The Affect of Negative Power Supply at Output Code-word 0000 0000 0000.

a) V_{ee} = -14.25 V

b) V_{ee} = -15.0 V



C) V_{ee} = -15.75 V

DUT - 5215 , f_{CL} - 162 KHz, V_{in} = -9.995 V

Figure 9-17. DUT Output Showing the Affect of Negative Power Supply at Output Code-word 1111 1111 1111.

Method #4 Automatic open loop linearity test method

Several of the techniques investigated by GEOS rely totally on the measurement or comparison of digital signals. These techniques assume that each digital code-word has an exact analog voltage equivalent (i.e. for measurement purposes in Method #4 a commanded 18-bit code-word to the reference DAC produces a predetermined analog output voltage).

Since the DUT full scale input voltage has a specified .4% maximum error, for a 0V to 10V DUT the required input voltage could be as high as 10.0375 V. This voltage is higher than the maximum output of the reference DAC, and additional analog signal processing is required. One solution to this problem is to insert a gain of two amplifier between the DAC and the DUT. The amplifier and its external resistors must be extremely precise, since 1 LSB is 0.0004% of full scale in an 18 bit converter. Offset drift, amplifier noise, and resistor noise all contribute to the measurement inaccuracy. Further, the settling time of the amplifier must be compatible with the dynamics of the test circuit.

The choice of a gain of 2, rather than 1.01, is for the convenience of handling the digital code in the REF DAC. Admittedly, this increases the parasitic effects of the amplifier in the test circuit. A compensating times two gain reduction is required in the DAC but this can easily be handled digitally by the automatic tester. Also the offset voltage to the DUT may be either positive or negative. Because of this the reference DAC will have to operate in a bipolar mode, even if the DUT is a unipolar device. Our original 18-bit reference DAC now has 16-bits of useful voltage magnitude.

A block diagram of this circuit is shown in FigureIX-18.The test circuit was not constructed by GEOS,although a similar technique was developed to the hardware stage in 1977. In this approach, the reference DAC is stepped through each of its input bits one bit at a time. After allowing time for analog voltage settling and for DUT conversion, the DAC input signal and the DUT output signal are measured and compared. Each time the DUT output changes, both the DUT output and the DAC input are recorded. The approach provides a direct measure of the transition voltage for each bit. From these measurements, linearity, differential non-linearity, absolute accuracy, zero error, missing codes, and monotonicity can all be determined. With this approach, the theoretical mechanization error is 1/16 of a DUT LSB. As with all approaches investigated, the analog type errors are expected to predominate.

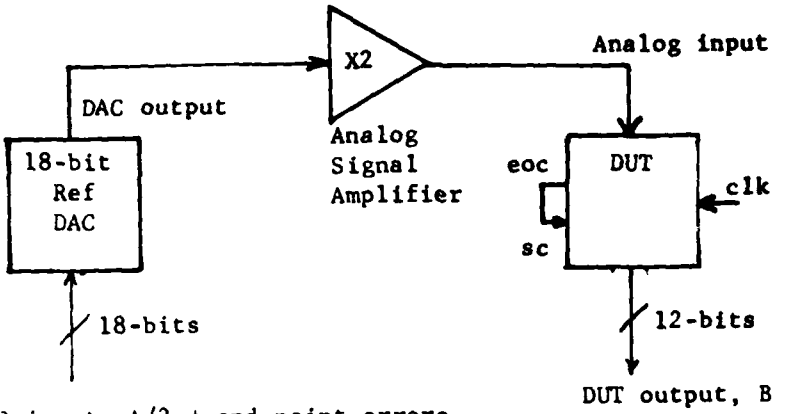


Figure 9-18. Simple Digital Measurement Technique

Method #5 Automatic Closed Loop Linearity Test Methods

Three closed loop methods were investigated by GEOS. All three methods use a dither that locks onto a threshold representing the point at which the DUT output code-word is equal to the commanded input code-word.

Any A/D test method must focus on the "transition points" (where the output code changes) since a transition point is the only point where the output code and the input voltage have unique values. (There are many input values for one output code.) A test circuit which varies the DUT analog input until a transition is detected is therefore the desired goal.

The dither signal used in Methods #2 and #3 previously described is an effective technique to vary the analog input about any desired voltage level within the analog input range. Whereas the dither signal in the crossplot method required a magnitude of several LSB, a closed-loop automatic test method can effectively employ a dither signal only a fraction of an LSB in amplitude.

The first of these three methods investigated by GEOS is a digital technique. The dither is developed digitally and all measurements are digital. The block diagram for this method is presented in Figure IX-19. The test circuit was not constructed by GEOS.

This technique is similar to the previously described approach in that it uses a highly accurate reference DAC and the measurements are all obtained from the digital code-words. However, instead of programming and measuring some 65536 digital code-words, this method programs only the 4094 code-words required by the DUT. A digital error signal is then either added to or subtracted from the original code-word. The resultant 12 bit code-word is then applied to the 18-bit reference DAC, and the analog signal to the DUT is adjusted to the level required to achieve the proper DUT output.

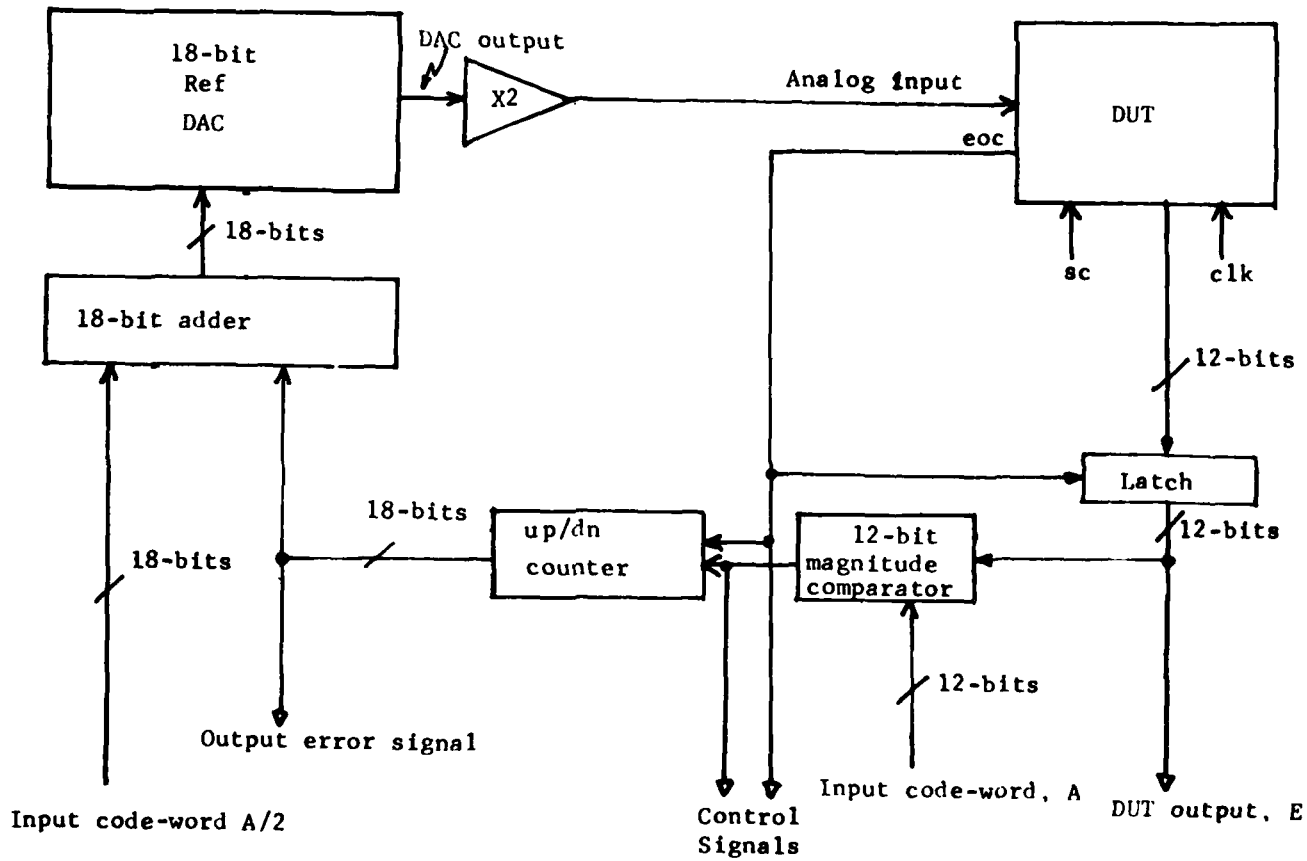


Figure 9-19. Digital Dither Measurement Technique

The digital error signal is generated by an up/down counter whose output, together with the commanded input code-word, is applied to a digital adder. Up/down control for the counter is supplied by a 12-bit digital magnitude comparator that compares the magnitudes of the DUT output and the commanded input code-word. The clock pulse for the counter is obtained from the DUT status (end-of-convert) output so that each status pulse steps the counter either forward or backward, in accordance with the state of the up/down control line.

The following is an example of the operation of the circuit of Figure 9-19:

1) Digital code-word, A, is applied to the 12-bit magnitude comparator and code word A/2 is applied to one input of the 18-bit adder.

2) If we assume that the output of the 18-bit up/down counter is zero momentarily, the adder output will be code-word A/2; it is applied to the reference DAC input.

3) Because of the gain-of-two analog amplifier, the voltage at the input to the DUT is the analog equivalent of code-word A.

4) A DUT code-word output, B, is obtained by converting this analog input. Assume, momentarily, that the magnitude of this output is less than the input code-word, A.

5) The magnitude comparator outputs will be high ("1") for output A $>$ B and low ("0") for outputs A $<$ B and A=B. Since output A $<$ B is tied to the up/down input to the counter, the counter will count up each time a status pulse causes a low-to-high transition. Therefore, as long as the up/down input is low the counter will step forward one count with each DUT conversion.

6) Since the code-word A/2 and the counter output are summed in the adder, the input to the reference DAC will change in such a way as to cause the DUT output, B, to increase.

7) When the reference DAC input is sufficiently advanced, the DUT output, B, will be equal to A. This will cause the magnitude comparator output A=B to go high, output A $>$ B to go low and the counter will step backward with the next DUT status pulse.

8) From this point on, the counter will step forward and backward with repetitive changes to the magnitude comparator output. The counter will dither between the conditions A $>$ B and A $\leq$ B. The voltage at the input to the DUT will be the value corresponding to the

transition between B-1 and B. If the magnitude comparator output A=B is ORed with the output A > B, the counter will dither about the condition $A \geq B$ and A < B. The average value of the DUT input voltage will represent the transition point between code-words B and B+1.

The second closed loop method is one of two methods mechanized by GEOS for this characterization. It is very similar to Method #2 previously described, except that it was implemented for automatic test. This method develops an analog signal error as opposed to a digital signal error. The error signal is added to the reference DAC output so as to develop a precise DUT analog input voltage, which corresponds to the transition between two adjacent digital output code-words B and B+1.

The functional block diagram for this approach is shown in Figure 9-8. As with the digital dither measurement technque, a digital code comparator is used to develop signal outputs of $A \leq B$ and A > B. Instead of controlling an up/down counter, these signals are used to control the polarity of a current applied to an analog integrator. The output of the integrator is a voltage that is summed with the reference DAC output and applied to the DUT analog input. Since the polarity of the integrator output voltage is controlled by the magnitude comparator, the DUT input voltage is forced to change in a direction that causes the output to approach the transition point between code words B and B+1. When the error is sufficiently small, the integrator output voltage will dither about a d.c. level that is proportional to the error of the DUT's bit transition accuracy.

Since the voltage at the DUT input is precisely that needed to establish the DUT output bit transition, we can conclude that if the reference DAC is precisely calibrated, the integrator output voltage is proportional to the error signal and will differ only by the gain of the summing amplifier. The peak-to-peak voltage of the dither defines a region wherein the amplitude of the error signal lies. Therefore, in order to minimize this ambiguity, the peal-to-peak voltage should have a maximum value of 0.1 LSB. This results in a varying voltage that has a slope such that dv/dt < 0.1 LSB conversion.

The slope of the dither is measured as a function of the value of the LSB and the time required to complete a conversion. Since an LSB can be either 2.44mV or 4.88 MV, and since the conversion test time can be either 13 usec or 50 usec, four different integrators/current source circuits are needed in order to maintain a constant $\frac{dv}{dt}$ = 0.1 LSB/conversion.

The problem with this approach is that the required DUT input voltage may be the equivalent of several (16 max.) LSBs away from the ideal output level of the reference DAC. The integrator will develop the error voltage at a rate of .1 LSBs per conversion and may require as many as 160 conversions just to reach the region of the error voltages final value. The number of conversions required in order to settle to the final error value can be reduced by increasing the value of dv/dt, however, this can be done only by sacrificing measurement accuracy, stability and repeatibility. Because of these problems and other layout problems, this test circuit was abandoned for the one shown in Figure 9-20.

Selected Automatic Test Approach

The selected approach for closed-loop automatic testing of the A/D converter is referred to as the "binary search and dither"method. The test circuit presented in Figure 9-20 uses an analog integrator to develop the error signal. As with the test circuit just described, the error signal is summed with the reference DAC output and applied to the DUT analog input. The DUT outputtest circuit is also similar in that it uses a magnitude comparator to compare the commanded digital code-word A with the DUT output code-word B. The output signals $A \geq B$ and $A < B$ are applied to a binary search and dither logic circuit which controls a DAC08 D/A converter. The DAC08 current output drives the analog integrator which develops the error signal to be summed with the reference DAC output. The average value of the DUT input voltage will represent the transition point between the DUT output code-words B and B+1.

A more detailed block diagram of the binary search and dither logic circuit is presented in Figure 9-21. An 8-bit D/A converter, operates in the bipolar mode and is used to source a current to the integrator or to sink a current from the integrator. With a 10 volt reference applied to the DAC08, the output current magnitude can be varied over a range from + 1 mA to - 1 mA in 7.8 uA steps. The polarity control to the DAC08 is determined by the output of the magnitude comparator. In the search mode, the magnitude of the DAC08 input is controlled both by a shift register output and by X-OR gates. The shift register established the absolute magnitude of the DAC08 input for negative output currents, and the X-OR gates are used to complement this input for positive output currents. Since the complementing function is ones-complement, a 1 LSB error exists between similar magnitude positive and negative output currents from the DAC08. This complementing function is used only in the search mode and, therefore, does not introduce errors in the dither mode.

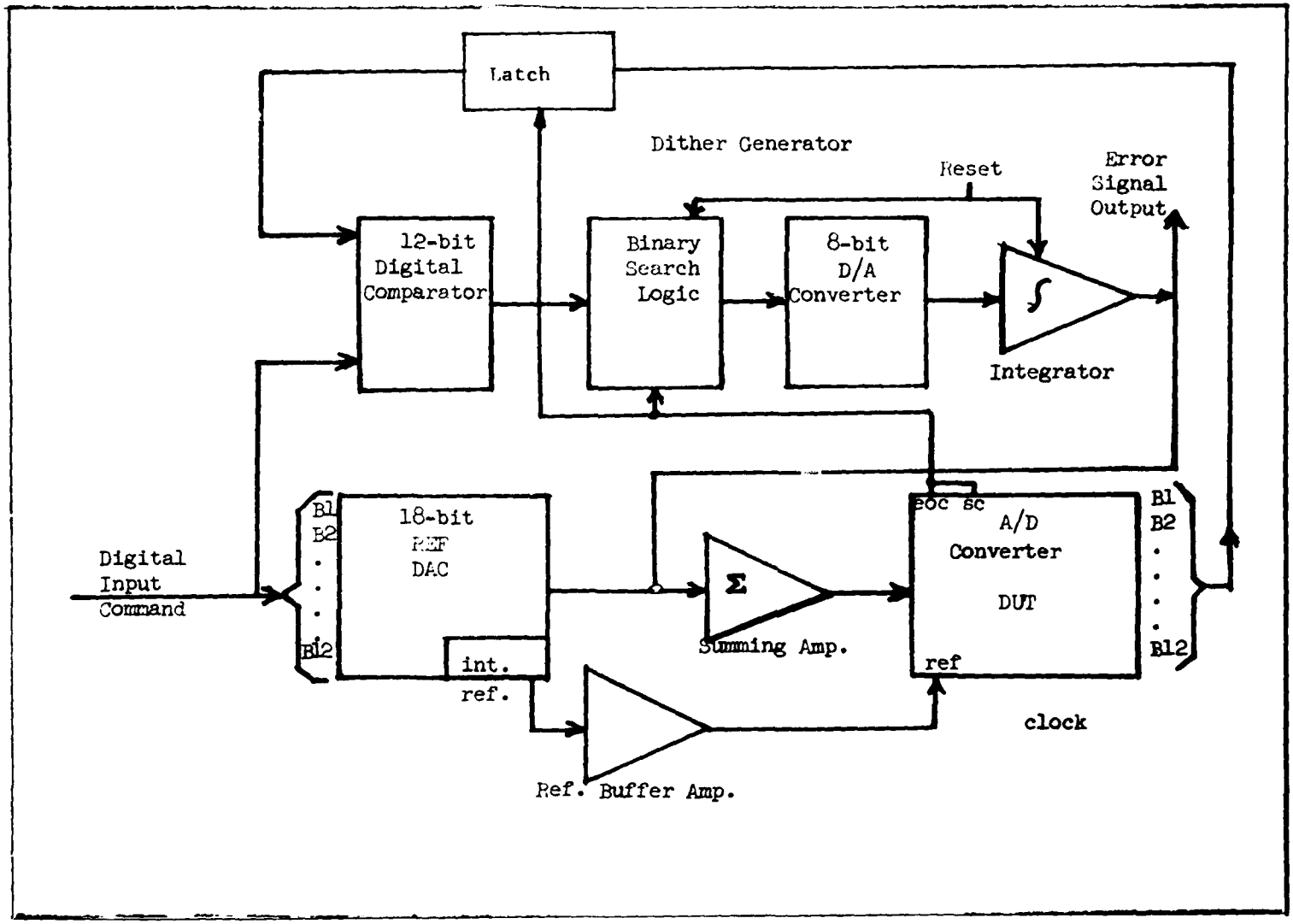


Figure 9-20. Block Diagram of A/D Converter Test Circuit

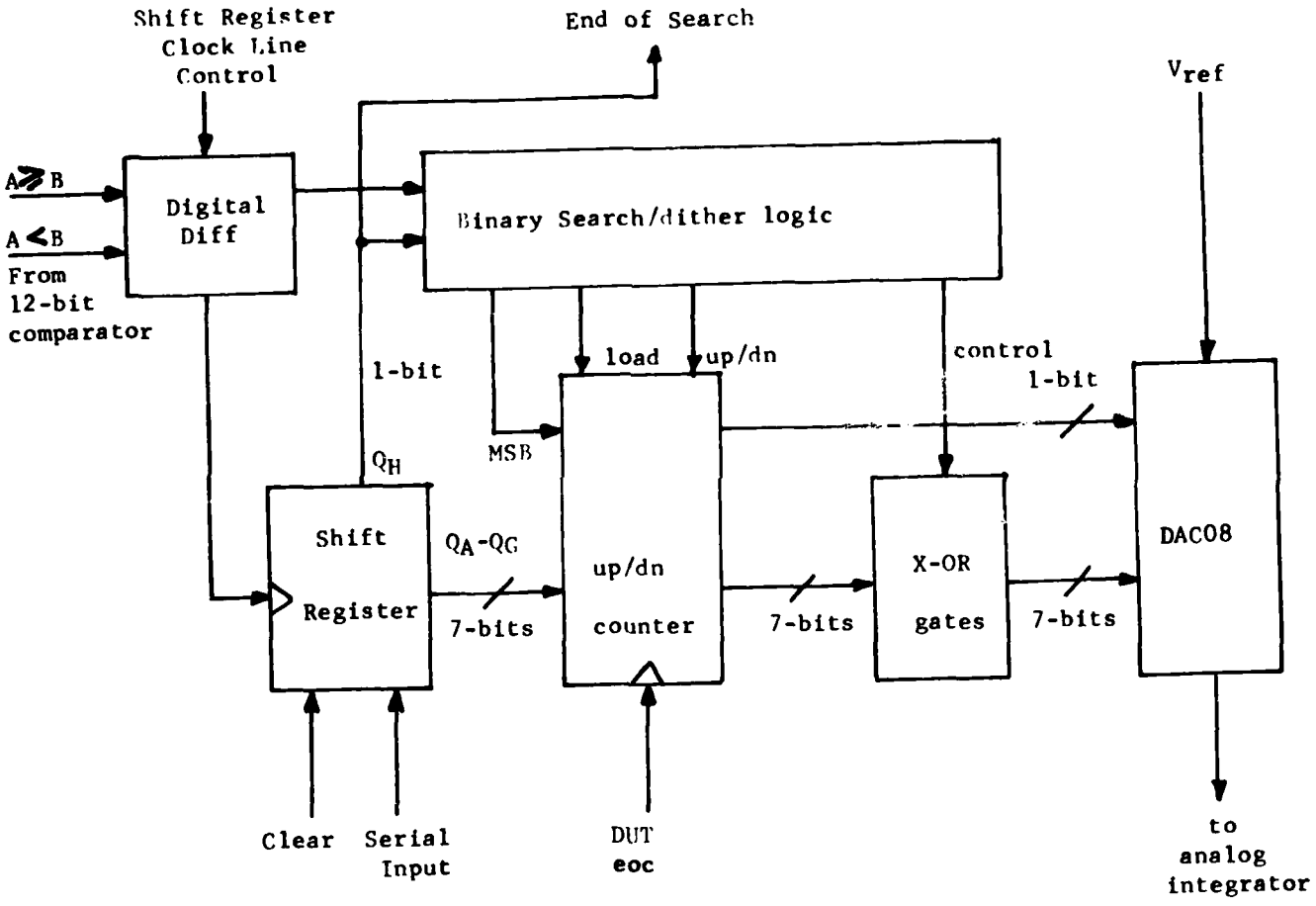


Figure 9-21. Block Diagram of Binary Search and Dither Circuit

The binary search routine commands successively decreasing currents from the DAC08. The search routine begins with an output current of 0.5 mA, absolute. Each time the output of the magnitude comparator changes state, the DAC08 output current is changed in polarity and is reduced by one half in magnitude until it has an absolute value of 1 LSB (7.8 uA).

At this point, the logic circuit automatically switches to the dither mode. In this mode, the up/down counter is activated and is used to control the output current of the DAC08. Each time the output of the comparator changes state, the counter is reset to a condition where the DAC08 output is zero. The new state of the comparator controls the up/down control line of the counter. The counter is then pulsed 1 LSB so that the DAC08 input is either 1000 0001 or 0111 1111. This corresponds to a current output of either - 7.8 uA or + 7.8 uA. The output code-word of the DUT will, therefore, dither between code-words B and B+1. The rate of change of the input analog voltage about the desired d.c. level is ± 0.1 LSB per conversion.

If the comparator output does not change state, the counter will not be reset. Then each time the counter is pulsed, the magnitude of the rate of change of the input analog voltage to the DUT will increase by 0.1 LSB. When the comparator output finally does change, this magnitude will reset to 0.1 LSB per conversion.

The following is an example of the operation of the above circuit. Block diagrams of the test circuit are presented in Figure 9-20 and 9-21. Examples of the integrator output are shown in Figures 9-22 and 9-23.

a) Digital code-word A is simultaneously applied to the 12-bit magnitude comparator and to the 12 MSBs of an 18-bit DAC. The lower six bits are tied low. A logic "1" is applied to the shift register serial input and a logic "0" is applied to the shift register clear. This sets up the circuit to operate in the search mode.

b) On the shift register, the clear input is then driven high, a pulse is applied to the clock input line and the serial input is then driven low. This sets the QA output of the shift register to logic "1" and all other outputs to logic "0". The load lines to the up/down counter now have an input code-word X100 0000. The MSB state is determined by the output of the magnitude comparator. Since the up/down counter is held in a load condition, the parallel output lines have the same code-word, X100 0000 and the counter's clock line is inhibited.

Figure 9-22. DUT Analog Input Voltage During Search Mode

Figure 9-23. DUT Analog Input Voltage During Dither Mode

c) If we assume that the DUT output B momentarily is greater than input code-word, A, then the ORed magnitude comparator outputs $A \leq B$ will be logic "1".

d) This will cause the MSB of the up/down counter to be logic "1" and the control line to the X-ORs to be logic "0". The DAC08 input code-word will be 1100 0000, and the output circuit will sink 0.5 mA. (ie: 64 x 7.8 uA).

e) This will cause the integrator, and thus, the DUT input to slew to a more positive voltage. As a result, the value of DUT output code word, B, will decrease. The high current output of the DAC08 will force the output of the DUT to change at a rate of 6.4 LSBs per conversion. Figure 22 illustrates the waveform of the analog input to the DUT during the search and dither routines. The top trace shows the DUT status output. The center trace shows the end of search signal, and defines the point at which the circuit switches from the binary search mode to the dither mode.

f) When the comparator output changes state, the MSB load line to the up/down counter changes state, the control input line to the X-ORs changes state, a clocking pulse is developed by the digital differentiator and is applied to the clock input of the shift register. The code-word loaded into the up/down counter is, therefore, 0010 0000.

g) Since the X-ORs are set to complement their signal line input, the code-word applied to the DAC08 input is 0101 1111 and the output circuit will source .258 mA. (ie: 33 x 7.8 uA). (The 1 LSB error is due to 1's complement of the code-word. This error occurs only in the search mode.)

h) The new current output from the DAC08 will force the integrator output, and thus, the DUT input to decrease. This results in an increasing DUT output signal. However, where as the DUT output was previously decreasing at a rate of 6.4 LSBs per conversion, it is now increasing at a rate of 3.3 LSBs per conversion.

i) Each time the comparator changes state, the logic "1" at the shift register output is right shifted one place, the direction of the DUT's changing output is reversed and the rate at which the output changes is reduced by half until the logic "1" has shifted to the last output line.

i) Each time the comparator changes state, the logic "1" at the shift register output is right shifted one place, the direction of the DUT's changing output is reversed and the rate at which the output changes is reduced by half until the logic "1" has shifted to the last output line.

j) At this point, the shift register output sets up the circuit that automatically changes the circuit from the search mode to the dither mode as follows:

   1) The clock input line to the shift register is inhibited and the register outputs remain fixed until a clear signal is applied.

   2) The up/down counter load control is released and is now activated each time the output of the magnitude comparator changes state. The counter clock line can now be activated by the low-to-high transition of the status signal.

   3) The X-OR gates are held in a state that allows the gates to pass the counter outputs directly to the DAC08.

   4) The MSB load line to the counter is held in a logic "1" state and the seven LSB load lines are held in a logic "0" state.

k) In the dither mode, each transition of the magnitude comparator output causes the code-word 1000 0000 to be parallel-loaded into the up/down counter during the time that the status is low. This code-word is applied to the DAC08 which results in zero current at the DAC08 output.

l) When the status goes from low to high the counter will be clocked one bit. If the up/down control line is low the new output code-word is 1000 0001. If the up/down control line is high the new output code-word is 0111 1111. Thus, the DAC08 output current is either - 7.8 uA or + 7.8 uA, equivalent to a 1 LSB output current.

m) If the nagnitude comparator output changes state with each conversion, the code-word to the DAC08 oscillates between 1000 0001 and 0111 1111, the magnitude of the rate of change of the input analog voltage will oscillate between + .1 LSB and - .1 LSB and DUT will oscillate between output code-words B and B+1. Figure 23 shows the analog input to the DUT during a single conversion while the test circuit is operating in the dither mode.

All of the bit accuracy and bit linearity methods described herein measure the transition points between DUT output code-words B and (B+1). For a 12-bit converter there are 4095 transitions, and therefore, 4094 LSBs between the first and the last transition. In the closed loop techniques, the first transition is measured by addressing bit (0) and the last transition by addressing bit (4094). If the measured voltages are $V_{m(0)}$ and $V_{m(4094)}$ respectively, the average slope of the gain curve is $(V_{m(4094)} - V_{m(0)})$ /4094. Sine the ideal gain expression has the form y = mx + b, where

y = the ideal input voltage (V_i) to the DUT

x = programmed code-word that corresponds to voltage (V_i).

b = the ideal voltage V_b for x = 0

$m = (V_{m(4094)} - V_{m(0)})/4094$,

then $V_i = (V_{m(4094)} \quad V_{m(0)})/4094 \quad x + V_b$

The adjustment technique, used by Micro Networks, places the first output code transition 1 LSB from the most negative voltage in the full scale range (ie: between code-words 1111 1111 1110 and 1111 1111 1111) and last output code transition 1 LSB from the most positive voltage in the full scale range (ie: between code-words 0000 0000 0000 and 0000 0000 0001). For the measurement technique used by GEOS the value of x in the gain equation is N. When N = 0, the measured voltage at the DUT input is $V_{m(0)}$. Substituting these values into the gain formula yields

$$V_{m(0)} = (V_{m(4094)} - V_{m(0)})/4094 \quad (0) + V_b.$$

From this, $V_b = V_{m(0)}$

and the ideal gain expression can be written as

$$V_i = \frac{(V_{m(4094)} - V_{m(0)})}{4094} \quad (N) + V_{m(0)}$$

The linearity error ($E_{(n)}$ can be determined at any bit by subtracting the value of V_i from $V_{m(n)}$, where $V_{m(n)}$ is the measured input voltage for bit (N). Thus,

$$E_{(N)} = (V_{m(N)} - V_i), \text{ volts}$$

or expressed in LSB

$$E_{(N)} = \frac{V_{m(N)} - V_i}{(V_{m(4094)} - V_{m(0)})/4094} \quad \text{LSB}$$

Assessment of the Selected Automatic Test Approach

GEOS experience with the "binary search and dither" test method has been very favorable at the time of this writing. Inspection of the analog input waveforms shown in Figures 9-22 and 9-23 show a typical peak-to-peak noise level of approximately .25 LSB.

Using a Fluke 8502A DMM any number of samples can be taken for a selected code transition and the min/max values of the transition voltage can also be recorded. Observations show that variations in threshold are typically very small, less than .01 LSB, and repeatability of data is excellent.

All-codes bench data was taken for one MN5216 device using bench test equipment and manually inserting the commanded code. Results of this testing are discussed further in Section 9-7.

Test Adapter Construction

Design and construction of the test adapter required the utmost care because of the mixture of high-speed digital logic circuits and highly accurate low level and high level analog circuits. In order to eliminate the effect of code-dependent digital ground currents on the analog signals, separate ground planes were used for the digital circuits and the analog circuits. Separate voltage regulators were used to power the digital circuits and the analog circuits. These regulators were powered by external ±20 Vdc and +10 Vdc power supplies. In addition, large tantalum capacitors were used at the input of each regulator to eliminate clock frequency cross talk between digital and analog signals.

The power supply return, clock signal return and each ground plane are connected separately to a unipoint ground located at the DUT ground pin. Also, in an effort eliminate pick up noise and line drops associated with coupling analog circuits, the output connections of the op amp feedback resistors were remotely connected to their respective loads.

Dynamic test parameters

Test parameters measured while the DUT is operating in continuous conversion mode comprise a list of dynamic test parameters for characterization. These test parameters are listed in the following:

Symbol	Parameter	Notes
PSS1	Power supply rejection (V_{cc})	Measured at V_o = "0"s & V_o = "1"s
PSS2	Power supply rejection (V_{cc})	Measured at V_o = "0"s & V_o = "1"s
PSS3	Power supply rejection (V_{log})	Measured at V_o = "0" & V_o = "1"s
V_{IO}	Unipolar offset error	At first transition nearest V_i = 0
BPOE	Bipolar offset error	At transition of codes 0000 0000 0000 & 0000 0000 0001
V_{FSE}	Absolute accuracy (gain error)	At V_{max} last transition
LE	Linearity Error	All transitions
MCE	Major carry error	All major carry transitions
N_T	Noise	At transition of codes 0111 1111 1111 & 1000 0000 0000

9.5 Test Results and Data

9.5.1 Discussion of Static Test Data (Method #1)

Static tests were performed on the following device types:

Quantity	Type	Mfr. Code
2	5204	A
2	5212	B
1	5213	B
1	5216	C

Virtually all data was within the specified limits. Representative data for each device type shown above is contained in the Appendix, Table 9-4 . A brief discussion of the parameters follows.

Output short circuit current (I_{OS})

All data for the 14 digital outputs (serial and parallel outputs, plus EOC) is well within limits. Changes with temperature, are not particularly significant (± 15% typical). The maximum current observed was -2.35 mA, at -55°C, compared to a limit of -25 mA. A limit of 10 mA would easily accommodate the device performance, based upon this small sample of data.

Input breakdown current (I_{IBK})

All data for the "start convert" and "clock" inputs is orders of magnitude below the limit of 1 mA. This is not unusual, since junction leakage currents are normally very low until a breakdown condition occurs.

Digital outputs, logic levels, V_{OL}, V_{OH}

For V_{OL}, all data is within the limit of 300 mV, with a maximum value of 235 mV occurring at +125°C.

For V_{OH}, all data is within the limit of 4.5 V, with a maximum value of 3.44 V occurring at + 125°C.

Logic input currents I_{IH}, I_{IL}

For I_{IH}, all data is within the limit of 20 uA, with a maximum value of 8.78 uA occurring at +125°C.

For I_{IL}, all data is within the limits of -440 to -50 uA, with a range of -430 to -194 uA.

Based upon the data from this small sample size, the limit of -490 uA may not be adequate for all devices.

Power supply current drain (I_{CC})

For the +5 V supply, all data is within the limit of 75 mA, with a maximum value of 42.6 mA occurring @ -55°C for manufacturer C. A power supply voltage of 5.5 V was used for the testing.
For the +15 V supply, the following distribution of data was observed (limit = 50 mA @ 15V, data taken at 15.75V).

Mfr.	Max Value	Temp
A	4.75 mA	-55°C
B	26.4 mA	+125°C
C	48.1 mA	All

For the -15V supply, the following distribution of data was observed (limit = -50 mA @ 15V, data taken at-15.75V).

Mfr.	Max Value	Temp
A	-15.7	-55°C
B	-14.2	+25°C
C	-25.4	-55°C

The differences among manufacturers are expected, due to choice of either +15 V or -15 V for developing the internal reference voltage and other internal circuitry. Since an internal reference device was not available from manufacturer A, further differences can be expected for that device type group. The power dissipation specification in Table I of /120 limits the device dissipation to 0.8 W for external reference device types, and 1.0 W for internal reference device types. This parameter is calculated from power supply currents.

Power dissipation calculated from the I_{CC} data is shown in the following table.

S/N	Mfr	Ref	Max Dissipation (over temp)
12	A	ext	410 mw
13	A	ext	516
9	B	int	902
10	B	int	642
11	B	ext	543
14		int	896

Rise time, digital outputs (t_{TLH})

All data is within the limits of 5.0 to 60 nsec, although the maximum data value of 58.5 nsec at +125°C is near the limit.

Fall time, digital outputs (t_{THL})

All data is within the limits of 2.0 to 30 nsec, with a maximum value of 21.3 nsec occurring at -55°C.

Propagation time (t_{pLH})

All data is within the limits of 20 to 160 nsec, with a maximum value of 103 nsec occurring at + 125°C.

Propagation time (t_{pHL})

All data is within the limits of 20 to 160 nsec, with a maximum value of 98 nsec occurring at 25°C.

"Start convert" pulse width (PW_{sc})

All devices responded to a "start convert" pulse having the minimum pulse width of 200 nsec.

Clock input pulse width (PW_{clk})

All devices performed normal conversions with a clock input pulse width of 200 nsec, the minimum value.

9.5.2 Discussion of Cross Plot Test Data (Method #3)

Initial characterization of the 5200 series A/D converter was begun by measuring the dynamic test parameters with a cross-plot test adapter. Although the cross-plot test method is an excellent means of determining converter characteristics, it is a slow and tedious test method where precision measurements are required. Consequentially, only a relatively few data points have been measured. Data was obtained by:

- o setting each bit high one at a time with all other bits low,
- o setting in all combinations of the first four bits with the 8LSBs low,
- o setting the first four bits high and setting each remaining bit high one at a time with the remaining 7LSBs low.

In addition, major carry differential linearity measurements were made between each major carry transition and both the bit transition below the major carry. Also, absolute end-point error measurements were made as well as the zero error measurements. Tables 9-5 through 9-9, in the appendix, show typical characterization data obtained on a 5212 A/D converter using the cross-plot technique.

9.5.3 Discussion of Automatic Test Data (Method #5)

At the time of this writing, GEOS is evaluating its automatic tester for measuring all codes bit linearity data on 12-bit 5200 series A/D converters. Measurements of linearity data are in process. Also, complete analysis and correlation of this data with the Micro Networks data is also in process.

GEOS has presented, in Figure 9-24, a plot of linearity data received from Micro Networks, with their permission. The linearity plot includes the error measurements made on all 4095 bit transitions and is typical of the data received from Micro Networks on five 5216 devices.

By using the test adapter developed for the S3270 Automatic Test Set, in a bench test configuration, GEOS has confirmed the general pattern of the curve and has been able to initially correlate GEOS data to many of the Micro Networks data points. A plot of the data taken by GEOS is shown in Figure 9-25. Figure 9-25 is a plot of each 64N and 64N ± 1 code-words, where $N = 0 \rightarrow 64$.

Using these test points only, most of the high positive and high negative error measurements, shown in Figure 9-24 are duplicated in Figure 9-25 at test point code-words 64N-1.

9.6 Discussion of Results

The static test parameters shown in Table 9-3 is a list of standard test parameters required for digital device conformance. The limits for these parameters are standard digital logic for the respective test parameters. All of the devices tested met the test limits of the tests listed in Table 9-3. The test for input logic current (I_{IL}) was the only parameter with measurements close to the test limit.

The dynamic test parameters listed in section 9.5 are a list of those parameters that affect the conversion accuracy and linearity of the device. Testing is not complete at this time. The plots shown in Figures 9-24 and 9-25 show data plotted from linearity measurements. The largest variations in linearity accuracy occurred at digital code-words 64N-1. Therefore, any set of abbreviated tests will have to examine these code-words. The data taken by Micro Networks and GEOS is similar in the pattern of the errors, however, closer examination of this data is required before data correlation can be established. Because, of the effect of both power supply and temperature on the device accuracy and linearity, additional data analysis is required for correlation. Table 9-9 shows the effect of power supply and temperature variations on zero error, and end-point absolute error.

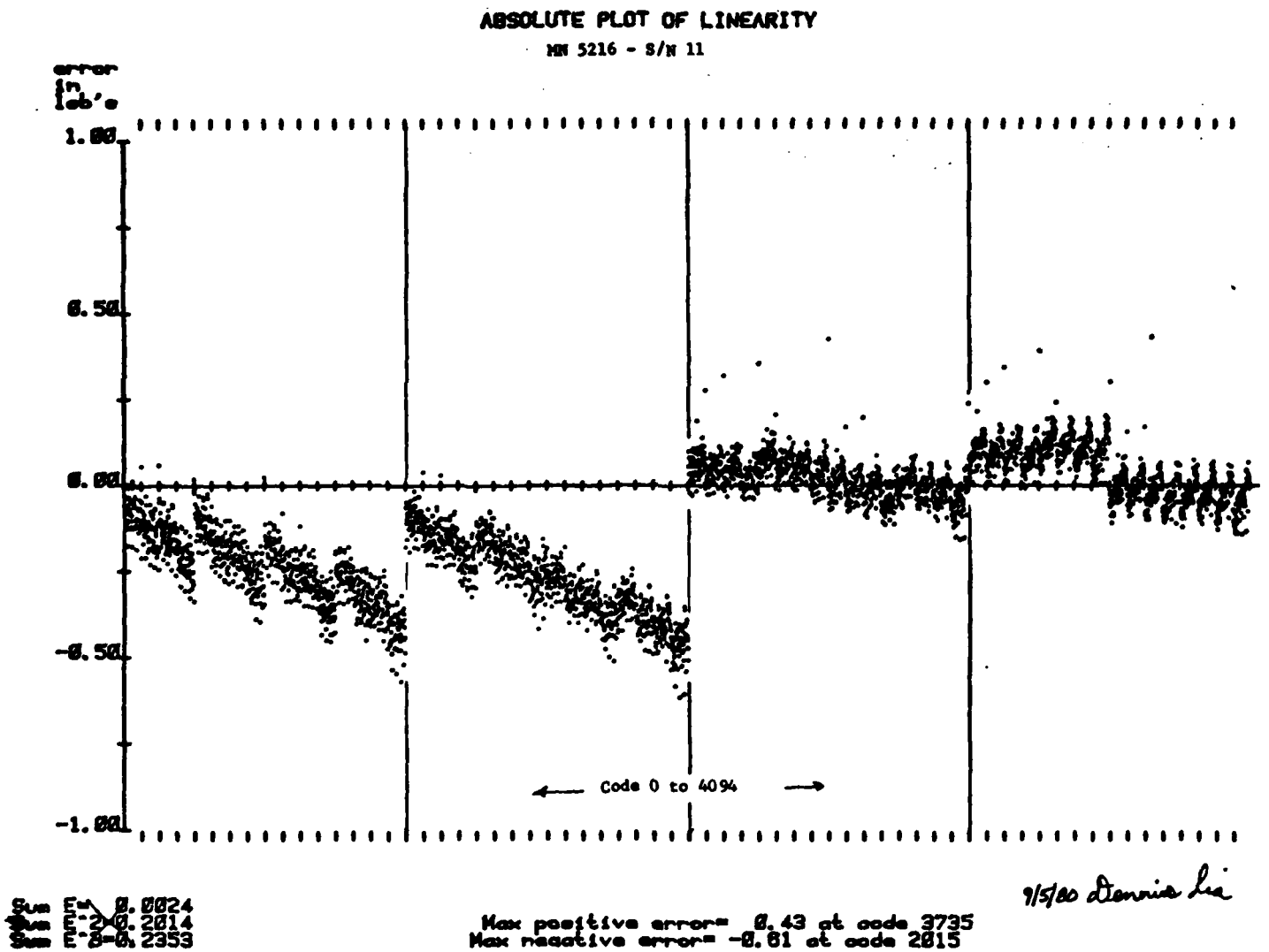


Figure 9-24. Absolute Plot of Linearity (courtesy of Micro Networks)

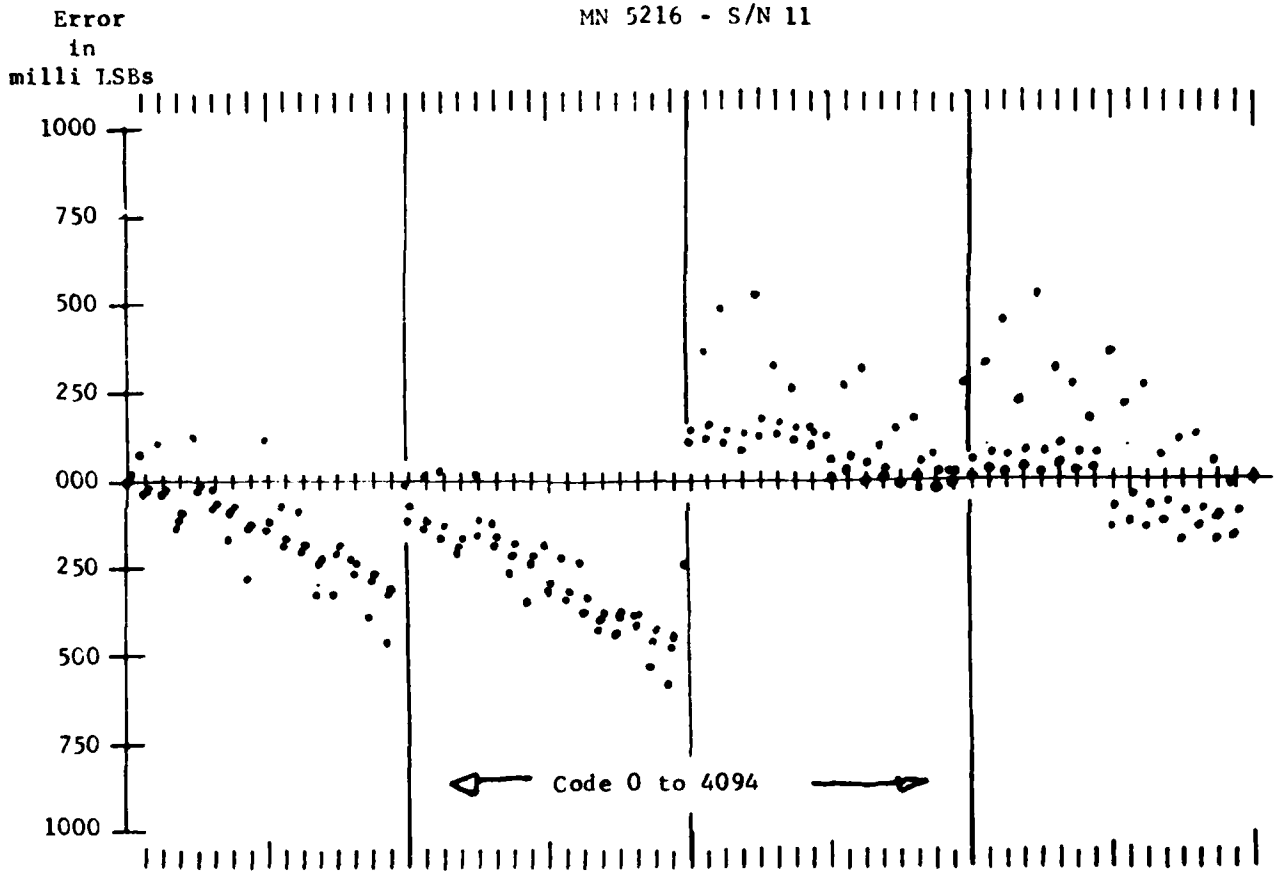


Figure 9-25. Plot of Linearity (Data by GEOS)

.7 Slash Sheet Development

The usual approach to specifying a linear device in a JAN 38510 slash sheet is to design a test circuit, compatible with most automatic test systems, suitable for testing at least 100% test parameters. Table III of the specification is developed to define the specific test steps and test limits for that test circuit. The device manufacturer has to either use that test circuit and procedure, or prove that his is equivalent, at the time when he submits devices for qualification.

In several meetings of the JC-41 5200/5210 A/D Converter Subcommittee, it has become apparent that this classical approach may not be appropriate for linearity testing. Each manufacturer has developed his own approach to testing linearity of A/D Converters, and, due to differences in test systems, each cannot implement identical test circuits. One manufacturer typically uses a manual test using test box adapters which interface with bench instruments. Recently, this manufacturer has also developed automatic test capability. Other manufacturers also are going through evolutionary development of test capability. Proving equivalence to one common test circuit developed for the slash sheet would be a difficult task.

At an Aug 12 '80 meeting of the 5200 Subcommittee, it was proposed that a method of proofing test validity be adopted whereby manufacturers would test a set of "correlation devices" and submit correlation data. Manufacturer data would have to agree with data established by RADC/DESC (via the U.S. Bureau of Standards, or some other certified test activity), on those devices. A set of "proof devices" would be tested first to determine that the tester will not cause the device under test to fail. Other more routine parameters would be specified and tested in the usual manner. At the time of this writing, this correlation approach is still being developed.

9.8 Conclusions and Recommendations

The characterization of the MN5200/5210 family is nearing completion at the time of this writing. The S3270 automatic test adapter has been proofed on the bench,and linearity errors for all codes has been taken on one device. Test software will soon be complete and debugging on the test system will begin. The correlation of GE and Micro Networks data demonstrated in Figures 9-24 and 9-25 is very encouraging.

Testing with the cross-plot method will be refined to accept clock frequencies in the range of 1 MHz.

It is anticipated that incorporation of the correlation approach to specify linearity testing in Mil-M-38510/120 will require further effort, as well as cooperation from device manufacturers.

When these hurdles are overcome, the first slash sheet for a complex hybrid 12-bit A/D converter, including automatic test, will be issued. This will pave the way for future slash sheets for even more complex LSI and hybrid devices.

Without the final characterization data, GE is not yet in a position to make recommendations regarding the suitability of this device family for /120.

However, widespread industry useage in military systems, including GE Ordnance Systems equipments, testify to the device performance. Indeed, all-codes data over the military temperature range will provide a stronger data base for device proofing, as well as a test approach and specification approach for similar devices of the future.

SECTION IX

APPENDIX

Table 9-4. Test Data Using Test Method #1

MANUFACTURER CODE: A ; DEVICE TYPE: 5804 ; S/N: 18 ; DATE CODE: 7834 14 APR 80 15:54:36

STATIC PARAMETER DATA

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	125 DEG C LO-LIM	125 DEG C DATA	125 DEG C HI-LIM	UNITS
IOS FOR BITS 1	-25.0	-1.35	0.00	-25.0	-1.20	0.00	-25.0	-1.00	0.00	MA
IOS FOR BITS 2	-25.0	-1.30	0.00	-25.0	-1.15	0.00	-25.0	-950.M	0.00	MA
IOS FOR BITS 3	-25.0	-1.30	0.00	-25.0	-1.15	0.00	-25.0	-1.00	0.00	MA
IOS FOR BITS 4	-25.0	-1.30	0.00	-25.0	-1.15	0.00	-25.0	-1.00	0.00	MA
IOS FOR BITS 5	-25.0	-1.30	0.00	-25.0	-1.15	0.00	-25.0	-1.00	0.00	MA
IOS FOR BITS 6	-25.0	-1.35	0.00	-25.0	-1.15	0.00	-25.0	-1.00	0.00	MA
IOS FOR BITS 7	-25.0	-1.25	0.00	-25.0	-1.10	0.00	-25.0	-950.M	0.00	MA
IOS FOR BITS 8	-25.0	-1.35	0.00	-25.0	-1.15	0.00	-25.0	-1.00	0.00	MA
IOS FOR BITS 9	-25.0	-1.35	0.00	-25.0	-1.15	0.00	-25.0	-950.M	0.00	MA
IOS FOR BITS 10	-25.0	-1.35	0.00	-25.0	-1.15	0.00	-25.0	-1.00	0.00	MA
IOS FOR BITS 11	-25.0	-1.30	0.00	-25.0	-1.15	0.00	-25.0	-1.00	0.00	MA
IOS FOR BITS 12	-25.0	-1.35	0.00	-25.0	-1.15	0.00	-25.0	-1.00	0.00	MA
IOS FOR END OF CONVERT	-25.0	-1.40	0.00	-25.0	-1.25	0.00	-25.0	-1.05	0.00	MA
IOS FOR SERIAL OUT	-25.0	-1.35	0.00	-25.0	-1.25	0.00	-25.0	-1.00	0.00	MA
IIB FOR START CONVERT	0.00	7.39M	1.00	0.00	733.U	1.00	0.00	7.87M	1.00	MA
IIB FOR CLOCK INPUT	0.00	2.61M	1.00	0.00	603.U	1.00	0.00	6.76M	1.00	MA
VOL FOR BITS 1	0.00	142.	300.	0.00	173.	300.	0.00	199.	300.	MV
VOL FOR BITS 2	0.00	140.	300.	0.00	170.	300.	0.00	196.	300.	MV
VOL FOR BITS 3	0.00	138.	300.	0.00	169.	300.	0.00	195.	300.	MV
VOL FOR BITS 4	0.00	139.	300.	0.00	168.	300.	0.00	194.	300.	MV
VOL FOR BITS 5	0.00	138.	300.	0.00	168.	300.	0.00	194.	300.	MV
VOL FOR BITS 6	0.00	137.	300.	0.00	166.	300.	0.00	194.	300.	MV
VOL FOR BITS 7	0.00	138.	300.	0.00	167.	300.	0.00	194.	300.	MV
VOL FOR BITS 8	0.00	136.	300.	0.00	167.	300.	0.00	195.	300.	MV
VOL FOR BITS 9	0.00	138.	300.	0.00	168.	300.	0.00	195.	300.	MV
VOL FOR BITS 10	0.00	138.	300.	0.00	168.	300.	0.00	196.	300.	MV
VOL FOR BITS 11	0.00	139.	300.	0.00	170.	300.	0.00	198.	300.	MV
VOL FOR BITS 12	0.00	141.	300.	0.00	170.	300.	0.00	196.	300.	MV
VOL FOR END OF CONVERT	0.00	144.	300.	0.00	174.	300.	0.00	202.	300.	MV
VOL FOR SERIAL OUT	0.00	142.	300.	0.00	173.	300.	0.00	201.	300.	MV
VOH FOR BITS 1	2.40	3.21	4.50	2.40	3.28	4.50	2.40	3.40	4.50	V
VOH FOR BITS 2	2.40	3.20	4.50	2.40	3.25	4.50	2.40	3.30	4.50	V
VOH FOR BITS 3	2.40	3.21	4.50	2.40	3.26	4.50	2.40	3.31	4.50	V
VOH FOR BITS 4	2.40	3.21	4.50	2.40	3.26	4.50	2.40	3.31	4.50	V
VOH FOR BITS 5	2.40	3.21	4.50	2.40	3.26	4.50	2.40	3.30	4.50	V
VOH FOR BITS 6	2.40	3.21	4.50	2.40	3.26	4.50	2.40	3.30	4.50	V
VOH FOR BITS 7	2.40	3.21	4.50	2.40	3.27	4.50	2.40	3.29	4.50	V
VOH FOR BITS 8	2.40	3.22	4.50	2.40	3.28	4.50	2.40	3.30	4.50	V
VOH FOR BITS 9	2.40	3.22	4.50	2.40	3.28	4.50	2.40	3.30	4.50	V
VOH FOR BITS 10	2.40	3.22	4.50	2.40	3.28	4.50	2.40	3.30	4.50	V
VOH FOR BITS 11	2.40	3.22	4.50	2.40	3.28	4.50	2.40	3.30	4.50	V
VOH FOR BITS 12	2.40	3.22	4.50	2.40	3.28	4.50	2.40	3.31	4.50	V
VOH FOR END OF CONVERT	2.40	3.22	4.50	2.40	3.27	4.50	2.40	3.38	4.50	V
VOH FOR SERIAL OUT	2.40	3.21	4.50	2.40	3.26	4.50	2.40	3.38	4.50	V
IIH FOR START CONVERT	0.00	8.70	20.0	0.00	637.M	20.0	0.00	6.42	20.0	UA
IIH FOR CLOCK	0.00	1.13	20.0	0.00	509.M	20.0	0.00	6.56	20.0	UA
IIL FOR START CONVERT	-440.	-413.	-50.0	-440.	-348.	-50.0	-440.	-285.	-50.0	UA
IIL FOR CLOCK	-440.	-404.	-50.0	-440.	-348.	-50.0	-440.	-285.	-50.0	UA
ICC (FOR +5V SUPPLY)	0.00	86.1	75.0	0.00	83.8	75.0	0.00	81.1	75.0	MA
ICC1 (FOR +15V SUPPLY)	0.00	4.46	50.0	0.00	3.85	50.0	0.00	3.85	50.0	MA
ICC2 (FOR -15V SUPPLY)	-50.0	-18.5	0.00	-50.0	-11.8	0.00	-50.0	-8.85	0.00	MA

Table 9-4. Test Data Using Test Method #1

MANUFACTURER CODE: A ; DEVICE TYPE:5804; S/N: 18; DATE CODE: 7834 14 APR 80 15:54:56

TRANSIENT PARAMETER DATA

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	125 DEG C LO-LIM	125 DEG C DATA	125 DEG C HI-LIM	UNITS
TTLH (RISE TIME) BIT# 1	5.00	28.1	60.0	5.00	33.0	60.0	5.00	39.8	60.0	NS
TTLH (RISE TIME) BIT# 2	5.00	27.4	60.0	5.00	34.0	60.0	5.00	41.6	60.0	NS
TTLH (RISE TIME) BIT# 3	5.00	29.8	60.0	5.00	36.3	60.0	5.00	45.8	60.0	NS
TTLH (RISE TIME) BIT# 4	5.00	28.3	60.0	5.00	34.8	60.0	5.00	43.2	60.0	NS
TTLH (RISE TIME) BIT# 5	5.00	28.2	60.0	5.00	36.2	60.0	5.00	44.8	60.0	NS
TTLH (RISE TIME) BIT# 6	5.00	26.4	60.0	5.00	32.6	60.0	5.00	42.6	60.0	NS
TTLH (RISE TIME) BIT# 7	5.00	30.3	60.0	5.00	36.2	60.0	5.00	46.9	60.0	NS
TTLH (RISE TIME) BIT# 8	5.00	31.3	60.0	5.00	38.1	60.0	5.00	50.3	60.0	NS
TTLH (RISE TIME) BIT# 9	5.00	28.3	60.0	5.00	34.7	60.0	5.00	44.5	60.0	NS
TTLH (RISE TIME) BIT# 10	5.00	28.2	60.0	5.00	34.6	60.0	5.00	44.2	60.0	NS
TTLH (RISE TIME) BIT# 11	5.00	30.3	60.0	5.00	37.4	60.0	5.00	48.9	60.0	NS
TTLH (RISE TIME) BIT# 12	5.00	25.0	60.0	5.00	30.3	60.0	5.00	41.3	60.0	NS
TTLH (RISE TIME) EOC	5.00	22.4	60.0	5.00	27.0	60.0	5.00	37.2	60.0	NS
TTLH (RISE TIME) SDO	5.00	23.7	60.0	5.00	28.2	60.0	5.00	38.3	60.0	NS
TTHL (FALL TIME) BIT# 1	2.00	18.1	30.0	2.00	13.6	30.0	2.00	11.9	30.0	NS
TTHL (FALL TIME) BIT# 2	2.00	19.1	30.0	2.00	14.0	30.0	2.00	12.0	30.0	NS
TTHL (FALL TIME) BIT# 3	2.00	18.5	30.0	2.00	13.3	30.0	2.00	11.3	30.0	NS
TTHL (FALL TIME) BIT# 4	2.00	17.8	30.0	2.00	12.8	30.0	2.00	10.9	30.0	NS
TTHL (FALL TIME) BIT# 5	2.00	18.1	30.0	2.00	13.2	30.0	2.00	11.3	30.0	NS
TTHL (FALL TIME) BIT# 6	2.00	18.8	30.0	2.00	13.6	30.0	2.00	11.6	30.0	NS
TTHL (FALL TIME) BIT# 7	2.00	18.5	30.0	2.00	13.5	30.0	2.00	11.4	30.0	NS
TTHL (FALL TIME) BIT# 8	2.00	17.8	30.0	2.00	12.9	30.0	2.00	11.0	30.0	NS
TTHL (FALL TIME) BIT# 9	2.00	17.9	30.0	2.00	13.0	30.0	2.00	11.3	30.0	NS
TTHL (FALL TIME) BIT# 10	2.00	18.5	30.0	2.00	13.6	30.0	2.00	11.8	30.0	NS
TTHL (FALL TIME) BIT# 11	2.00	17.6	30.0	2.00	12.7	30.0	2.00	10.9	30.0	NS
TTHL (FALL TIME) BIT# 12	2.00	19.0	30.0	2.00	14.1	30.0	2.00	12.3	30.0	NS
TTHL (FALL TIME) EOC	2.00	13.6	30.0	2.00	10.0	30.0	2.00	8.75	30.0	NS
TTHL (FALL TIME) SDO	2.00	14.8	30.0	2.00	11.1	30.0	2.00	9.35	30.0	NS
TPLH FROM CLK TO BIT# 1	20.0	64.0	160.	20.0	67.0	160.	20.0	75.0	160.	NS
TPLH FROM CLK TO BIT# 2	20.0	60.5	160.	20.0	62.0	160.	20.0	67.5	160.	NS
TPLH FROM CLK TO BIT# 3	20.0	60.5	160.	20.0	62.5	160.	20.0	70.0	160.	NS
TPLH FROM CLK TO BIT# 4	20.0	61.0	160.	20.0	62.5	160.	20.0	68.5	160.	NS
TPLH FROM CLK TO BIT# 5	20.0	60.5	160.	20.0	62.0	160.	20.0	69.0	160.	NS
TPLH FROM CLK TO BIT# 6	20.0	60.5	160.	20.0	61.5	160.	20.0	66.5	160.	NS
TPLH FROM CLK TO BIT# 7	20.0	61.0	160.	20.0	63.0	160.	20.0	69.5	160.	NS
TPLH FROM CLK TO BIT# 8	20.0	60.5	160.	20.0	62.5	160.	20.0	69.5	160.	NS
TPLH FROM CLK TO BIT# 9	20.0	60.5	160.	20.0	62.0	160.	20.0	69.0	160.	NS
TPLH FROM CLK TO BIT# 10	20.0	60.6	160.	20.0	62.0	160.	20.0	69.0	160.	NS
TPLH FROM CLK TO BIT# 11	20.0	60.5	160.	20.0	62.5	160.	20.0	70.0	160.	NS
TPLH FROM CLK TO BIT# 12	20.0	61.0	160.	20.0	63.0	160.	20.0	67.5	160.	NS
TPLH FROM CLK TO EOC	20.0	53.5	160.	20.0	56.0	160.	20.0	81.5	160.	NS
TPLH FROM CLK TO SDO	20.0	58.5	160.	20.0	53.0	160.	20.0	58.0	160.	NS
TPHL FROM CLK TO BIT# 1	20.0	63.0	160.	20.0	63.5	160.	20.0	68.0	160.	NS
TPHL FROM CLK TO BIT# 2	20.0	60.0	160.	20.0	57.5	160.	20.0	64.5	160.	NS
TPHL FROM CLK TO BIT# 3	20.0	61.0	160.	20.0	58.0	160.	20.0	66.0	160.	NS
TPHL FROM CLK TO BIT# 4	20.0	60.5	160.	20.0	57.5	160.	20.0	66.0	160.	NS
TPHL FROM CLK TO BIT# 5	20.0	60.0	160.	20.0	57.0	160.	20.0	64.0	160.	NS
TPHL FROM CLK TO BIT# 6	20.0	60.0	160.	20.0	57.0	160.	20.0	64.0	160.	NS
TPHL FROM CLK TO BIT# 7	20.0	59.5	160.	20.0	56.0	160.	20.0	63.0	160.	NS
TPHL FROM CLK TO BIT# 8	20.0	60.5	160.	20.0	57.0	160.	20.0	64.5	160.	NS
TPHL FROM CLK TO BIT# 9	20.0	59.5	160.	20.0	56.5	160.	20.0	64.0	160.	NS
TPHL FROM CLK TO BIT# 10	20.0	59.5	160.	20.0	56.5	160.	20.0	64.0	160.	NS
TPHL FROM CLK TO BIT# 11	20.0	60.0	160.	20.0	57.0	160.	20.0	64.0	160.	NS
TPHL FROM CLK TO BIT# 12	20.0	61.5	160.	20.0	58.0	160.	20.0	66.0	160.	NS
TPHL FROM CLK TO EOC	20.0	46.5	160.	20.0	44.5	160.	20.0	44.0	160.	NS
TPHL FROM CLK TO SDO	20.0	50.0	160.	20.0	46.0	160.	20.0	48.5	160.	NS

Table 9-4. Test Data Using Test Method #1

MANUFACTURER CODE: B , DEVICE TYPE: 5213 , S/N: 11 , DATE CODE: 7515 14 APR 88 15:53:54

STATIC PARAMETER DATA

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	125 DEG C LO-LIM	125 DEG C DATA	125 DEG C HI-LIM	UNITS
IOS FOR BIT# 1	-25.0	-1.65	0.00	-25.0	-1.50	0.00	-25.0	-1.45	0.00	MA
IOS FOR BIT# 2	-25.0	-1.60	0.00	-25.0	-1.50	0.00	-25.0	-1.40	0.00	MA
IOS FOR BIT# 3	-25.0	-1.65	0.00	-25.0	-1.65	0.00	-25.0	-1.45	0.00	MA
IOS FOR BIT# 4	-25.0	-1.75	0.00	-25.0	-1.65	0.00	-25.0	-1.55	0.00	MA
IOS FOR BIT# 5	-25.0	-1.75	0.00	-25.0	-1.65	0.00	-25.0	-1.55	0.00	MA
IOS FOR BIT# 6	-25.0	-1.75	0.00	-25.0	-1.65	0.00	-25.0	-1.55	0.00	MA
IOS FOR BIT# 7	-25.0	-1.75	0.00	-25.0	-1.65	0.00	-25.0	-1.55	0.00	MA
IOS FOR BIT# 8	-25.0	-1.80	0.00	-25.0	-1.65	0.00	-25.0	-1.60	0.00	MA
IOS FOR BIT# 9	-25.0	-1.75	0.00	-25.0	-1.65	0.00	-25.0	-1.55	0.00	MA
IOS FOR BIT# 10	-25.0	-1.80	0.00	-25.0	-1.65	0.00	-25.0	-1.55	0.00	MA
IOS FOR BIT# 11	-25.0	-1.70	0.00	-25.0	-1.60	0.00	-25.0	-1.50	0.00	MA
IOS FOR BIT# 12	-25.0	-1.80	0.00	-25.0	-1.70	0.00	-25.0	-1.60	0.00	MA
IOS FOR END OF CONVERT	-25.0	-900.M	0.00	-25.0	-800.M	0.00	-25.0	-700.M	0.00	MA
IOS FOR SERIAL OUT	-25.0	-950.M	0.00	-25.0	-800.M	0.00	-25.0	-750.M	0.00	MA
IIB FOR START CONVERT	0.00	22.2M	1.00	0.00	1.50M	1.00	0.00	8.74M	1.00	MA
IIB FOR CLOCK INPUT	0.00	8.68M	1.00	0.00	1.09M	1.00	0.00	7.82M	1.00	MA
VOL FOR BIT# 1	0.00	166.	300.	0.00	200.	300.	0.00	235.	300.	MV
VOL FOR BIT# 2	0.00	160.	300.	0.00	193.	300.	0.00	228.	300.	MV
VOL FOR BIT# 3	0.00	160.	300.	0.00	189.	300.	0.00	224.	300.	MV
VOL FOR BIT# 4	0.00	154.	300.	0.00	185.	300.	0.00	219.	300.	MV
VOL FOR BIT# 5	0.00	154.	300.	0.00	185.	300.	0.00	216.	300.	MV
VOL FOR BIT# 6	0.00	148.	300.	0.00	178.	300.	0.00	209.	300.	MV
VOL FOR BIT# 7	0.00	149.	300.	0.00	179.	300.	0.00	212.	300.	MV
VOL FOR BIT# 8	0.00	152.	300.	0.00	184.	300.	0.00	216.	300.	MV
VOL FOR BIT# 9	0.00	156.	300.	0.00	188.	300.	0.00	222.	300.	MV
VOL FOR BIT# 10	0.00	160.	300.	0.00	193.	300.	0.00	228.	300.	MV
VOL FOR BIT# 11	0.00	161.	300.	0.00	195.	300.	0.00	231.	300.	MV
VOL FOR BIT# 12	0.00	164.	300.	0.00	197.	300.	0.00	233.	300.	MV
VOL FOR END OF CONVERT	0.00	153.	300.	0.00	184.	300.	0.00	216.	300.	MV
VOL FOR SERIAL OUT	0.00	149.	300.	0.00	179.	300.	0.00	212.	300.	MV
VOH FOR BIT# 1	2.40	3.04	4.50	2.40	3.17	4.50	2.40	3.44	4.50	V
VOH FOR BIT# 2	2.40	3.05	4.50	2.40	3.16	4.50	2.40	3.37	4.50	V
VOH FOR BIT# 3	2.40	3.07	4.50	2.40	3.16	4.50	2.40	3.37	4.50	V
VOH FOR BIT# 4	2.40	3.08	4.50	2.40	3.16	4.50	2.40	3.38	4.50	V
VOH FOR BIT# 5	2.40	3.08	4.50	2.40	3.16	4.50	2.40	3.38	4.50	V
VOH FOR BIT# 6	2.40	3.08	4.50	2.40	3.17	4.50	2.40	3.38	4.50	V
VOH FOR BIT# 7	2.40	3.04	4.50	2.40	3.16	4.50	2.40	3.37	4.50	V
VOH FOR BIT# 8	2.40	3.04	4.50	2.40	3.16	4.50	2.40	3.37	4.50	V
VOH FOR BIT# 9	2.40	3.06	4.50	2.40	3.16	4.50	2.40	3.37	4.50	V
VOH FOR BIT# 10	2.40	3.06	4.50	2.40	3.16	4.50	2.40	3.37	4.50	V
VOH FOR BIT# 11	2.40	3.06	4.50	2.40	3.16	4.50	2.40	3.37	4.50	V
VOH FOR BIT# 12	2.40	3.05	4.50	2.40	3.16	4.50	2.40	3.37	4.50	V
VOH FOR END OF CONVERT	2.40	2.88	4.50	2.40	3.16	4.50	2.40	3.37	4.50	V
VOH FOR SERIAL OUT	2.40	3.00	4.50	2.40	3.16	4.50	2.40	3.48	4.50	V
IIH FOR START CONVERT	0.00	8.59	80.0	0.00	1.13	80.0	0.00	7.07	80.0	UA
IIH FOR CLOCK	0.00	3.84	80.0	0.00	818.M	80.0	0.00	6.43	80.0	UA
IIL FOR START CONVERT	-440.	-888.	-50.0	-440.	-836.	-50.0	-440.	-188.	-80.0	UA
IIL FOR CLOCK	-440.	-874.	-50.0	-440.	-830.	-50.0	-440.	-184.	-80.0	UA
ICC (FOR +5V SUPPLY)	0.00	18.5	75.0	0.00	16.0	75.0	0.00	13.8	75.0	MA
ICC1 (FOR +10V SUPPLY)	0.00	85.7	90.0	0.00	85.0	90.0	0.00	83.4	90.0	MA
ICC2 (FOR -10V SUPPLY)	-90.0	-8.30	0.00	-90.0	-8.18	0.00	-90.0	-1.70	0.00	MA

Table 9-4. Test Data Using Test Method #1

MANUFACTURER CODE: B ; DEVICE TYPE:5813; S/N: 11; DATE CODE: 7515 14 APR 86 15:54:14

PARAMETER	TRANSIENT PARAMETER DATA -55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	125 DEG C LO-LIM	125 DEG C DATA	125 DEG C HI-LIM	UNITS
TTLH (RISE TIME) BIT# 1	5.00	33.4	60.0	5.00	38.6	60.0	5.00	47.0	60.0	NS
TTLH (RISE TIME) BIT# 2	5.00	33.8	60.0	5.00	40.2	60.0	5.00	49.0	60.0	NS
TTLH (RISE TIME) BIT# 3	5.00	34.4	60.0	5.00	42.1	60.0	5.00	51.8	60.0	NS
TTLH (RISE TIME) BIT# 4	5.00	33.6	60.0	5.00	40.8	60.0	5.00	48.8	60.0	NS
TTLH (RISE TIME) BIT# 5	5.00	34.0	60.0	5.00	41.1	60.0	5.00	48.1	60.0	NS
TTLH (RISE TIME) BIT# 6	5.00	31.8	60.0	5.00	38.8	60.0	5.00	46.6	60.0	NS
TTLH (RISE TIME) BIT# 7	5.00	36.1	60.0	5.00	43.1	60.0	5.00	48.9	60.0	NS
TTLH (RISE TIME) BIT# 8	5.00	37.2	60.0	5.00	45.7	60.0	5.00	54.7	60.0	NS
TTLH (RISE TIME) BIT# 9	5.00	32.8	60.0	5.00	40.9	60.0	5.00	49.6	60.0	NS
TTLH (RISE TIME) BIT# 10	5.00	33.7	60.0	5.00	41.4	60.0	5.00	49.6	60.0	NS
TTLH (RISE TIME) BIT# 11	5.00	36.3	60.0	5.00	46.9	60.0	5.00	54.4	60.0	NS
TTLH (RISE TIME) BIT# 12	5.00	30.9	60.0	5.00	37.1	60.0	5.00	46.3	60.0	NS
TTLH (RISE TIME) EOC	5.00	28.0	60.0	5.00	36.6	60.0	5.00	50.9	60.0	NS
TTLH (RISE TIME) SDO	5.00	32.5	60.0	5.00	41.1	60.0	5.00	58.5	60.0	NS
TTHL (FALL TIME) BIT# 1	2.00	19.8	30.0	2.00	16.9	30.0	2.00	16.9	30.0	NS
TTHL (FALL TIME) BIT# 2	2.00	20.2	30.0	2.00	17.1	30.0	2.00	16.0	30.0	NS
TTHL (FALL TIME) BIT# 3	2.00	18.5	30.0	2.00	15.4	30.0	2.00	14.9	30.0	NS
TTHL (FALL TIME) BIT# 4	2.00	18.4	30.0	2.00	15.2	30.0	2.00	14.7	30.0	NS
TTHL (FALL TIME) BIT# 5	2.00	19.4	30.0	2.00	15.7	30.0	2.00	15.0	30.0	NS
TTHL (FALL TIME) BIT# 6	2.00	18.8	30.0	2.00	15.6	30.0	2.00	14.9	30.0	NS
TTHL (FALL TIME) BIT# 7	2.00	19.1	30.0	2.00	15.7	30.0	2.00	14.8	30.0	NS
TTHL (FALL TIME) BIT# 8	2.00	18.8	30.0	2.00	15.4	30.0	2.00	14.8	30.0	NS
TTHL (FALL TIME) BIT# 9	2.00	19.9	30.0	2.00	16.1	30.0	2.00	15.4	30.0	NS
TTHL (FALL TIME) BIT# 10	2.00	20.8	30.0	2.00	16.6	30.0	2.00	16.0	30.0	NS
TTHL (FALL TIME) BIT# 11	2.00	18.6	30.0	2.00	15.1	30.0	2.00	14.7	30.0	NS
TTHL (FALL TIME) BIT# 12	2.00	21.3	30.0	2.00	17.2	30.0	2.00	16.6	30.0	NS
TTHL (FALL TIME) EOC	2.00	12.8	30.0	2.00	10.4	30.0	2.00	9.60	30.0	NS
TTHL (FALL TIME) SDO	2.00	13.6	30.0	2.00	11.4	30.0	2.00	10.4	30.0	NS
TPLH FROM CLK TO BIT# 1	20.0	93.0	160.	20.0	101.	160.	20.0	103.	160.	NS
TPLH FROM CLK TO BIT# 2	20.0	86.5	160.	20.0	92.5	160.	20.0	92.5	160.	NS
TPLH FROM CLK TO BIT# 3	20.0	87.0	160.	20.0	92.5	160.	20.0	93.0	160.	NS
TPLH FROM CLK TO BIT# 4	20.0	87.0	160.	20.0	92.0	160.	20.0	92.0	160.	NS
TPLH FROM CLK TO BIT# 5	20.0	86.0	160.	20.0	91.0	160.	20.0	91.0	160.	NS
TPLH FROM CLK TO BIT# 6	20.0	85.5	160.	20.0	90.0	160.	20.0	89.5	160.	NS
TPLH FROM CLK TO BIT# 7	20.0	86.5	160.	20.0	91.5	160.	20.0	91.5	160.	NS
TPLH FROM CLK TO BIT# 8	20.0	86.5	160.	20.0	92.5	160.	20.0	93.0	160.	NS
TPLH FROM CLK TO BIT# 9	20.0	86.0	160.	20.0	91.5	160.	20.0	91.5	160.	NS
TPLH FROM CLK TO BIT# 10	20.0	86.5	160.	20.0	92.0	160.	20.0	91.5	160.	NS
TPLH FROM CLK TO BIT# 11	20.0	86.5	160.	20.0	92.0	160.	20.0	92.5	160.	NS
TPLH FROM CLK TO BIT# 12	20.0	89.5	160.	20.0	96.0	160.	20.0	96.5	160.	NS
TPLH FROM CLK TO EOC	20.0	79.0	160.	20.0	86.5	160.	20.0	86.0	160.	NS
TPLH FROM CLK TO SDO	20.0	68.5	160.	20.0	73.5	160.	20.0	77.5	160.	NS
TPHL FROM CLK TO BIT# 1	20.0	96.0	160.	20.0	98.0	160.	20.0	91.0	160.	NS
TPHL FROM CLK TO BIT# 2	20.0	86.5	160.	20.0	84.5	160.	20.0	78.0	160.	NS
TPHL FROM CLK TO BIT# 3	20.0	84.5	160.	20.0	84.0	160.	20.0	78.5	160.	NS
TPHL FROM CLK TO BIT# 4	20.0	85.0	160.	20.0	84.0	160.	20.0	78.5	160.	NS
TPHL FROM CLK TO BIT# 5	20.0	84.5	160.	20.0	83.5	160.	20.0	78.0	160.	NS
TPHL FROM CLK TO BIT# 6	20.0	83.5	160.	20.0	82.5	160.	20.0	74.0	160.	NS
TPHL FROM CLK TO BIT# 7	20.0	84.0	160.	20.0	82.5	160.	20.0	73.0	160.	NS
TPHL FROM CLK TO BIT# 8	20.0	86.0	160.	20.0	85.5	160.	20.0	77.0	160.	NS
TPHL FROM CLK TO BIT# 9	20.0	86.0	160.	20.0	84.5	160.	20.0	78.0	160.	NS
TPHL FROM CLK TO BIT# 10	20.0	86.0	160.	20.0	84.5	160.	20.0	78.0	160.	NS
TPHL FROM CLK TO BIT# 11	20.0	86.0	160.	20.0	84.5	160.	20.0	78.0	160.	NS
TPHL FROM CLK TO BIT# 12	20.0	88.5	160.	20.0	87.0	160.	20.0	78.0	160.	NS
TPHL FROM CLK TO EOC	20.0	83.5	160.	20.0	83.5	160.	20.0	80.0	160.	NS
TPHL FROM CLK TO SDO	20.0	88.0	160.	20.0	88.0	160.	20.0	83.0	160.	NS

Table 9-4. Test Data Using Test Method #1

MANUFACTURER CODE: B ; DEVICE TYPE: 5218 ; S/N: 9 ; DATE CODE: 7845 14 APR 80 15:53:13

STATIC PARAMETER DATA

PARAMETER	-55 DEG C			25 DEG C			125 DEG C			UNITS
	LO-LIM	DATA	HI-LIM	LO-LIM	DATA	HI-LIM	LO-LIM	DATA	HI-LIM	
IOS FOR BIT# 1	-25.0	-2.15	0.00	-25.0	-2.00	0.00	-25.0	-1.85	0.00	MA
IOS FOR BIT# 2	-25.0	-2.05	0.00	-25.0	-1.90	0.00	-25.0	-1.75	0.00	MA
IOS FOR BIT# 3	-25.0	-2.10	0.00	-25.0	-1.95	0.00	-25.0	-1.80	0.00	MA
IOS FOR BIT# 4	-25.0	-2.10	0.00	-25.0	-1.95	0.00	-25.0	-1.80	0.00	MA
IOS FOR BIT# 5	-25.0	-2.10	0.00	-25.0	-1.95	0.00	-25.0	-1.80	0.00	MA
IOS FOR BIT# 6	-25.0	-2.05	0.00	-25.0	-1.95	0.00	-25.0	-1.80	0.00	MA
IOS FOR BIT# 7	-25.0	-2.00	0.00	-25.0	-1.85	0.00	-25.0	-1.75	0.00	MA
IOS FOR BIT# 8	-25.0	-2.05	0.00	-25.0	-1.90	0.00	-25.0	-1.75	0.00	MA
IOS FOR BIT# 9	-25.0	-2.10	0.00	-25.0	-1.95	0.00	-25.0	-1.80	0.00	MA
IOS FOR BIT# 10	-25.0	-2.10	0.00	-25.0	-1.95	0.00	-25.0	-1.80	0.00	MA
IOS FOR BIT# 11	-25.0	-2.10	0.00	-25.0	-2.00	0.00	-25.0	-1.85	0.00	MA
IOS FOR BIT# 12	-25.0	-2.10	0.00	-25.0	-1.85	0.00	-25.0	-1.80	0.00	MA
IOS FOR END OF CONVERT	-25.0	-1.35	0.00	-25.0	-1.25	0.00	-25.0	-1.05	0.00	MA
IOS FOR SERIAL OUT	-25.0	-1.35	0.00	-25.0	-1.20	0.00	-25.0	-1.00	0.00	MA
IIB FOR START CONVERT	0.00	16.3M	1.00	0.00	1.48M	1.00	0.00	10.9M	1.00	MA
IIB FOR CLOCK INPUT	0.00	1.15M	1.00	0.00	1.18M	1.00	0.00	9.44M	1.00	MA
VOL FOR BIT# 1	0.00	146.	300.	0.00	176.	300.	0.00	216.	300.	MV
VOL FOR BIT# 2	0.00	144.	300.	0.00	175.	300.	0.00	212.	300.	MV
VOL FOR BIT# 3	0.00	143.	300.	0.00	173.	300.	0.00	210.	300.	MV
VOL FOR BIT# 4	0.00	141.	300.	0.00	170.	300.	0.00	205.	300.	MV
VOL FOR BIT# 5	0.00	139.	300.	0.00	169.	300.	0.00	204.	300.	MV
VOL FOR BIT# 6	0.00	138.	300.	0.00	166.	300.	0.00	200.	300.	MV
VOL FOR BIT# 7	0.00	134.	300.	0.00	162.	300.	0.00	195.	300.	MV
VOL FOR BIT# 8	0.00	137.	300.	0.00	164.	300.	0.00	198.	300.	MV
VOL FOR BIT# 9	0.00	139.	300.	0.00	167.	300.	0.00	202.	300.	MV
VOL FOR BIT# 10	0.00	140.	300.	0.00	170.	300.	0.00	204.	300.	MV
VOL FOR BIT# 11	0.00	143.	300.	0.00	172.	300.	0.00	207.	300.	MV
VOL FOR BIT# 12	0.00	146.	300.	0.00	212.	300.	0.00	212.	300.	MV
VOL FOR END OF CONVERT	0.00	131.	300.	0.00	158.	300.	0.00	190.	300.	MV
VOL FOR SERIAL OUT	0.00	134.	300.	0.00	162.	300.	0.00	196.	300.	MV
VOH FOR BIT# 1	2.40	2.75	4.50	2.40	3.02	4.50	2.40	3.36	4.50	V
VOH FOR BIT# 2	2.40	2.73	4.50	2.40	3.00	4.50	2.40	3.30	4.50	V
VOH FOR BIT# 3	2.40	2.74	4.50	2.40	3.01	4.50	2.40	3.31	4.50	V
VOH FOR BIT# 4	2.40	2.74	4.50	2.40	3.01	4.50	2.40	3.31	4.50	V
VOH FOR BIT# 5	2.40	3.82	4.50	2.40	3.26	4.50	2.40	3.42	4.50	V
VOH FOR BIT# 6	2.40	3.81	4.50	2.40	3.26	4.50	2.40	3.42	4.50	V
VOH FOR BIT# 7	2.40	3.81	4.50	2.40	3.25	4.50	2.40	3.41	4.50	V
VOH FOR BIT# 8	2.40	3.81	4.50	2.40	3.25	4.50	2.40	3.41	4.50	V
VOH FOR BIT# 9	2.40	3.82	4.50	2.40	3.27	4.50	2.40	3.42	4.50	V
VOH FOR BIT# 10	2.40	3.81	4.50	2.40	3.27	4.50	2.40	3.42	4.50	V
VOH FOR BIT# 11	2.40	3.82	4.50	2.40	3.82	4.50	2.40	3.41	4.50	V
VOH FOR BIT# 12	2.40	3.82	4.50	2.40	3.82	4.50	2.40	3.42	4.50	V
VOH FOR END OF CONVERT	2.40	3.83	4.50	2.40	3.88	4.50	2.40	3.40	4.50	V
VOH FOR SERIAL OUT	2.40	3.80	4.50	2.40	3.87	4.50	2.40	3.44	4.50	V
IIH FOR START CONVERT	0.00	6.0S	80.0	0.00	1.18	80.0	0.00	8.78	80.0	UA
IIH FOR CLOCK	0.00	838.N	80.0	0.00	1.00	80.0	0.00	7.73	80.0	UA
IIL FOR START CONVERT	-440.	-388.	-80.0	-440.	-388.	-80.0	-440.	-884.	-80.0	UA
IIL FOR CLOCK	-440.	-378.	-80.0	-440.	-384.	-80.0	-440.	-883.	-80.0	UA
IOO (FOR +5V SUPPLY)	0.00	87.4	75.0	0.00	84.8	75.0	0.00	19.4	75.0	MA
IOO1 (FOR +10V SUPPLY)	0.00	14.0	50.0	0.00	14.4	50.0	0.00	88.4	50.0	MA
IOO2 (FOR -10V SUPPLY)	-50.0	-18.8	0.00	-50.0	-13.3	0.00	-50.0	-84.1	0.00	MA

Table 9-4. Test Data Using Test Method #1

MANUFACTURER CODE: B ; DEVICE TYPE:5812; S/N: 9; DATE CODE: 7845 14 APR 80 15:53:33

PARAMETER	TRANSIENT PARAMETER DATA -55 DEG C LO-LIM	DATA	HI-LIM	25 DEG C LO-LIM	DATA	HI-LIM	125 DEG C LO-LIM	DATA	HI-LIM	UNITS
TTLH (RISE TIME) BIT# 1	5.00	23.0	60.0	5.00	25.8	60.0	5.00	33.6	60.0	NS
TTLH (RISE TIME) BIT# 2	5.00	22.3	60.0	5.00	25.4	60.0	5.00	34.6	60.0	NS
TTLH (RISE TIME) BIT# 3	5.00	23.6	60.0	5.00	27.6	60.0	5.00	36.3	60.0	NS
TTLH (RISE TIME) BIT# 4	5.00	22.7	60.0	5.00	27.6	60.0	5.00	36.3	60.0	NS
TTLH (RISE TIME) BIT# 5	5.00	21.7	60.0	5.00	26.5	60.0	5.00	34.8	60.0	NS
TTLH (RISE TIME) BIT# 6	5.00	20.7	60.0	5.00	24.1	60.0	5.00	33.0	60.0	NS
TTLH (RISE TIME) BIT# 7	5.00	22.6	60.0	5.00	27.4	60.0	5.00	34.9	60.0	NS
TTLH (RISE TIME) BIT# 8	5.00	23.8	60.0	5.00	28.9	60.0	5.00	37.3	60.0	NS
TTLH (RISE TIME) BIT# 9	5.00	21.4	60.0	5.00	26.4	60.0	5.00	34.8	60.0	NS
TTLH (RISE TIME) BIT# 10	5.00	21.8	60.0	5.00	26.3	60.0	5.00	33.9	60.0	NS
TTLH (RISE TIME) BIT# 11	5.00	22.8	60.0	5.00	28.2	60.0	5.00	36.5	60.0	NS
TTLH (RISE TIME) BIT# 12	5.00	19.2	60.0	5.00	23.8	60.0	5.00	32.0	60.0	NS
TTLH (RISE TIME) EOC	5.00	20.2	60.0	5.00	24.5	60.0	5.00	35.6	60.0	NS
TTLH (RISE TIME) SDO	5.00	21.6	60.0	5.00	25.8	60.0	5.00	37.4	60.0	NS
TTHL (FALL TIME) BIT# 1	2.00	16.3	30.0	2.00	13.2	30.0	2.00	11.2	30.0	NS
TTHL (FALL TIME) BIT# 2	2.00	17.1	30.0	2.00	13.5	30.0	2.00	11.1	30.0	NS
TTHL (FALL TIME) BIT# 3	2.00	16.3	30.0	2.00	12.7	30.0	2.00	10.6	30.0	NS
TTHL (FALL TIME) BIT# 4	2.00	15.8	30.0	2.00	12.2	30.0	2.00	10.1	30.0	NS
TTHL (FALL TIME) BIT# 5	2.00	16.4	30.0	2.00	12.5	30.0	2.00	10.4	30.0	NS
TTHL (FALL TIME) BIT# 6	2.00	16.3	30.0	2.00	12.7	30.0	2.00	10.7	30.0	NS
TTHL (FALL TIME) BIT# 7	2.00	16.5	30.0	2.00	12.7	30.0	2.00	10.6	30.0	NS
TTHL (FALL TIME) BIT# 8	2.00	15.8	30.0	2.00	11.9	30.0	2.00	9.90	30.0	NS
TTHL (FALL TIME) BIT# 9	2.00	16.0	30.0	2.00	12.3	30.0	2.00	10.4	30.0	NS
TTHL (FALL TIME) BIT# 10	2.00	16.5	30.0	2.00	12.8	30.0	2.00	11.0	30.0	NS
TTHL (FALL TIME) BIT# 11	2.00	15.6	30.0	2.00	11.9	30.0	2.00	10.0	30.0	NS
TTHL (FALL TIME) BIT# 12	2.00	17.4	30.0	2.00	13.4	30.0	2.00	11.3	30.0	NS
TTHL (FALL TIME) EOC	2.00	11.1	30.0	2.00	8.70	30.0	2.00	7.65	30.0	NS
TTHL (FALL TIME) SDO	2.00	12.3	30.0	2.00	9.95	30.0	2.00	8.45	30.0	NS
TPLH FROM CLK TO BIT# 1	20.0	67.5	160.	20.0	71.0	160.	20.0	77.0	160.	NS
TPLH FROM CLK TO BIT# 2	20.0	65.0	160.	20.0	66.5	160.	20.0	71.0	160.	NS
TPLH FROM CLK TO BIT# 3	20.0	65.0	160.	20.0	66.5	160.	20.0	72.0	160.	NS
TPLH FROM CLK TO BIT# 4	20.0	66.0	160.	20.0	67.0	160.	20.0	71.0	160.	NS
TPLH FROM CLK TO BIT# 5	20.0	65.0	160.	20.0	66.0	160.	20.0	70.0	160.	NS
TPLH FROM CLK TO BIT# 6	20.0	65.0	160.	20.0	65.0	160.	20.0	68.0	160.	NS
TPLH FROM CLK TO BIT# 7	20.0	64.0	160.	20.0	65.0	160.	20.0	70.5	160.	NS
TPLH FROM CLK TO BIT# 8	20.0	64.0	160.	20.0	65.0	160.	20.0	71.0	160.	NS
TPLH FROM CLK TO BIT# 9	20.0	63.5	160.	20.0	65.0	160.	20.0	70.0	160.	NS
TPLH FROM CLK TO BIT# 10	20.0	63.5	160.	20.0	65.0	160.	20.0	70.5	160.	NS
TPLH FROM CLK TO BIT# 11	20.0	64.0	160.	20.0	66.0	160.	20.0	71.0	160.	NS
TPLH FROM CLK TO BIT# 12	20.0	66.0	160.	20.0	68.0	160.	20.0	70.0	160.	NS
TPLH FROM CLK TO EOC	20.0	56.5	160.	20.0	60.0	160.	20.0	65.0	160.	NS
TPLH FROM CLK TO SDO	20.0	52.0	160.	20.0	54.0	160.	20.0	61.0	160.	NS
TPHL FROM CLK TO BIT# 1	20.0	70.0	160.	20.0	71.0	160.	20.0	88.5	160.	NS
TPHL FROM CLK TO BIT# 2	20.0	64.0	160.	20.0	68.0	160.	20.0	88.0	160.	NS
TPHL FROM CLK TO BIT# 3	20.0	64.5	160.	20.0	68.0	160.	20.0	88.5	160.	NS
TPHL FROM CLK TO BIT# 4	20.0	64.5	160.	20.0	68.0	160.	20.0	88.5	160.	NS
TPHL FROM CLK TO BIT# 5	20.0	66.0	160.	20.0	68.5	160.	20.0	88.5	160.	NS
TPHL FROM CLK TO BIT# 6	20.0	65.0	160.	20.0	68.0	160.	20.0	88.5	160.	NS
TPHL FROM CLK TO BIT# 7	20.0	65.5	160.	20.0	68.0	160.	20.0	87.5	160.	NS
TPHL FROM CLK TO BIT# 8	20.0	67.0	160.	20.0	68.5	160.	20.0	88.0	160.	NS
TPHL FROM CLK TO BIT# 9	20.0	66.0	160.	20.0	68.5	160.	20.0	88.5	160.	NS
TPHL FROM CLK TO BIT# 10	20.0	66.0	160.	20.0	68.5	160.	20.0	88.5	160.	NS
TPHL FROM CLK TO BIT# 11	20.0	66.5	160.	20.0	68.0	160.	20.0	88.0	160.	NS
TPHL FROM CLK TO BIT# 12	20.0	67.5	160.	20.0	68.0	160.	20.0	88.0	160.	NS
TPHL FROM CLK TO EOC	20.0	47.5	160.	20.0	47.0	160.	20.0	48.0	160.	NS
TPHL FROM CLK TO SDO	20.0	49.5	160.	20.0	50.5	160.	20.0	49.0	160.	NS

Table 9-4. Test Data Using Test Method #1

MANUFACTURER CODE: C ; DEVICE TYPE: 5818 ; S/N: 14 ; DATE CODE: 7837 15 APR 80 18:50:08

STAT:C PARAMETER DATA

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	125 DEG C LO-LIM	125 DEG C DATA	125 DEG C HI-LIM	UNITS
IOS FOR BIT# 1	-25.0	-1.55	0.00	-25.0	-1.35	0.00	-25.0	-1.15	0.00	MA
IOS FOR BIT# 2	-25.0	-1.50	0.00	-25.0	-1.30	0.00	-25.0	-1.10	0.00	MA
IOS FOR BIT# 3	-25.0	-1.50	0.00	-25.0	-1.35	0.00	-25.0	-1.15	0.00	MA
IOS FOR BIT# 4	-25.0	-1.50	0.00	-25.0	-1.35	0.00	-25.0	-1.10	0.00	MA
IOS FOR BIT# 5	-25.0	-1.50	0.00	-25.0	-1.35	0.00	-25.0	-1.10	0.00	MA
IOS FOR BIT# 6	-25.0	-1.50	0.00	-25.0	-1.35	0.00	-25.0	-1.15	0.00	MA
IOS FOR BIT# 7	-25.0	-1.40	0.00	-25.0	-1.25	0.00	-25.0	-1.05	0.00	MA
IOS FOR BIT# 8	-25.0	-1.40	0.00	-25.0	-1.25	0.00	-25.0	-1.10	0.00	MA
IOS FOR BIT# 9	-25.0	-1.45	0.00	-25.0	-1.30	0.00	-25.0	-1.10	0.00	MA
IOS FOR BIT# 10	-25.0	-1.45	0.00	-25.0	-1.30	0.00	-25.0	-1.10	0.00	MA
IOS FOR BIT# 11	-25.0	-1.45	0.00	-25.0	-1.30	0.00	-25.0	-1.10	0.00	MA
IOS FOR BIT# 12	-25.0	-1.35	0.00	-25.0	-1.30	0.00	-25.0	-1.10	0.00	MA
IOS FOR END OF CONVERT	-25.0	-1.25	0.00	-25.0	-1.10	0.00	-25.0	-900.M	0.00	MA
IOS FOR SERIAL OUT	-25.0	-1.15	0.00	-25.0	-1.00	0.00	-25.0	-800.M	0.00	MA
IIB FOR START CONVERT	0.00	778.U	1.00	0.00	1.03M	1.00	0.00	9.27M	1.00	MA
IIB FOR CLOCK INPUT	0.00	579.U	1.00	0.00	819.U	1.00	0.00	7.86M	1.00	MA
VOL FOR BIT# 1	0.00	120.	300.	0.00	143.	300.	0.00	165.	300.	MV
VOL FOR BIT# 2	0.00	118.	300.	0.00	139.	300.	0.00	162.	300.	MV
VOL FOR BIT# 3	0.00	118.	300.	0.00	138.	300.	0.00	160.	300.	MV
VOL FOR BIT# 4	0.00	118.	300.	0.00	137.	300.	0.00	158.	300.	MV
VOL FOR BIT# 5	0.00	114.	300.	0.00	135.	300.	0.00	156.	300.	MV
VOL FOR BIT# 6	0.00	115.	300.	0.00	135.	300.	0.00	155.	300.	MV
VOL FOR BIT# 7	0.00	116.	300.	0.00	137.	300.	0.00	158.	300.	MV
VOL FOR BIT# 8	0.00	117.	300.	0.00	136.	300.	0.00	156.	300.	MV
VOL FOR BIT# 9	0.00	115.	300.	0.00	136.	300.	0.00	158.	300.	MV
VOL FOR BIT# 10	0.00	115.	300.	0.00	137.	300.	0.00	158.	300.	MV
VOL FOR BIT# 11	0.00	115.	300.	0.00	137.	300.	0.00	159.	300.	MV
VOL FOR BIT# 12	0.00	142.	300.	0.00	141.	300.	0.00	160.	300.	MV
VOL FOR END OF CONVERT	0.00	119.	300.	0.00	138.	300.	0.00	160.	300.	MV
VOL FOR SERIAL OUT	0.00	117.	300.	0.00	138.	300.	0.00	162.	300.	MV
VOH FOR BIT# 1	2.40	3.12	4.50	2.40	3.15	4.50	2.40	3.41	4.50	V
VOH FOR BIT# 2	2.40	3.14	4.50	2.40	3.17	4.50	2.40	3.37	4.50	V
VOH FOR BIT# 3	2.40	3.14	4.50	2.40	3.17	4.50	2.40	3.37	4.50	V
VOH FOR BIT# 4	2.40	3.15	4.50	2.40	3.17	4.50	2.40	3.37	4.50	V
VOH FOR BIT# 5	2.40	3.15	4.50	2.40	3.17	4.50	2.40	3.37	4.50	V
VOH FOR BIT# 6	2.40	3.15	4.50	2.40	3.17	4.50	2.40	3.37	4.50	V
VOH FOR BIT# 7	2.40	3.15	4.50	2.40	3.15	4.50	2.40	3.36	4.50	V
VOH FOR BIT# 8	2.40	3.16	4.50	2.40	3.19	4.50	2.40	3.37	4.50	V
VOH FOR BIT# 9	2.40	3.16	4.50	2.40	3.19	4.50	2.40	3.37	4.50	V
VOH FOR BIT# 10	2.40	3.16	4.50	2.40	3.19	4.50	2.40	3.37	4.50	V
VOH FOR BIT# 11	2.40	3.16	4.50	2.40	3.19	4.50	2.40	3.37	4.50	V
VOH FOR BIT# 12	2.40	3.17	4.50	2.40	3.19	4.50	2.40	3.38	4.50	V
VOH FOR END OF CONVERT	2.40	3.14	4.50	2.40	3.17	4.50	2.40	3.38	4.50	V
VOH FOR SERIAL OUT	2.40	3.14	4.50	2.40	3.17	4.50	2.40	3.40	4.50	V
IIH FOR START CONVERT	0.00	698.N	80.0	0.00	708.N	80.0	0.00	7.07	80.0	UA
IIH FOR CLOCK	0.00	610.N	80.0	0.00	711.N	80.0	0.00	6.67	80.0	UA
IIL FOR START CONVERT	-440.	-348.	-80.0	-440.	-388.	-80.0	-440.	-320.	-80.0	UA
IIL FOR CLOCK	-440.	-380.	-80.0	-440.	-378.	-80.0	-440.	-381.	-80.0	UA
ICC (FOR +5V SUPPLY)	0.00	48.6	75.0	0.00	38.1	75.0	0.00	28.9	75.0	MA
ICC1 (FOR +10V SUPPLY)	0.00	—	80.0	0.00	8.4	80.0	0.00	—	80.0	MA
ICC2 (FOR -10V SUPPLY)	-80.0	-85.4	0.00	-80.0	-84.8	0.00	-80.0	-88.9	0.00	MA

Table 9-4. Test Data Using Test Method #1

MANUFACTURER CODE: C ; DEVICE TYPE:6816; S/N: 14; DATE CODE: 7937 15 APR 80 18:50:28

TRANSIENT PARAMETER DATA

PARAMETER	-55 DEG C			25 DEG C			125 DEG C			UNITS
	LO-LIM	DATA	HI-LIM	LO-LIM	DATA	HI-LIM	LO-LIM	DATA	HI-LIM	
TTLH (RISE TIME) BIT# 1	5.00	27.8	60.0	5.00	31.1	60.0	5.00	42.4	60.0	NS
TTLH (RISE TIME) BIT# 8	5.00	28.3	60.0	5.00	32.8	60.0	5.00	44.9	60.0	NS
TTLH (RISE TIME) BIT# 3	5.00	28.4	60.0	5.00	34.7	60.0	5.00	48.2	60.0	NS
TTLH (RISE TIME) BIT# 4	5.00	30.9	60.0	5.00	33.3	60.0	5.00	45.7	60.0	NS
TTLH (RISE TIME) BIT# 5	5.00	26.8	60.0	5.00	33.4	60.0	5.00	46.1	60.0	NS
TTLH (RISE TIME) BIT# 6	5.00	25.7	60.0	5.00	32.0	60.0	5.00	45.5	60.0	NS
TTLH (RISE TIME) BIT# 7	5.00	28.9	60.0	5.00	34.5	60.0	5.00	47.8	60.0	NS
TTLH (RISE TIME) BIT# 8	5.00	31.4	60.0	5.00	37.1	60.0	5.00	52.6	60.0	NS
TTLH (RISE TIME) BIT# 9	5.00	28.2	60.0	5.00	32.9	60.0	5.00	46.0	60.0	NS
TTLH (RISE TIME) BIT# 10	5.00	24.8	60.0	5.00	32.8	60.0	5.00	46.1	60.0	NS
TTLH (RISE TIME) BIT# 11	5.00	28.4	60.0	5.00	36.0	60.0	5.00	49.7	60.0	NS
TTLH (RISE TIME) BIT# 12	5.00	26.6	60.0	5.00	31.1	60.0	5.00	43.9	60.0	NS
TTLH (RISE TIME) EOC	5.00	24.3	60.0	5.00	30.3	60.0	5.00	43.4	60.0	NS
TTLH (RISE TIME) SDO	5.00	26.9	60.0	5.00	33.9	60.0	5.00	47.8	60.0	NS
TTHL (FALL TIME) BIT# 1	2.00	15.3	30.0	2.00	12.7	30.0	2.00	11.9	30.0	NS
TTHL (FALL TIME) BIT# 2	2.00	15.8	30.0	2.00	13.1	30.0	2.00	11.5	30.0	NS
TTHL (FALL TIME) BIT# 3	2.00	15.0	30.0	2.00	12.1	30.0	2.00	11.2	30.0	NS
TTHL (FALL TIME) BIT# 4	2.00	14.4	30.0	2.00	11.6	30.0	2.00	10.6	30.0	NS
TTHL (FALL TIME) BIT# 5	2.00	14.8	30.0	2.00	12.0	30.0	2.00	11.0	30.0	NS
TTHL (FALL TIME) BIT# 6	2.00	15.2	30.0	2.00	12.4	30.0	2.00	11.4	30.0	NS
TTHL (FALL TIME) BIT# 7	2.00	16.6	30.0	2.00	13.1	30.0	2.00	11.5	30.0	NS
TTHL (FALL TIME) BIT# 8	2.00	15.0	30.0	2.00	12.0	30.0	2.00	10.8	30.0	NS
TTHL (FALL TIME) BIT# 9	2.00	15.2	30.0	2.00	12.2	30.0	2.00	11.3	30.0	NS
TTHL (FALL TIME) BIT# 10	2.00	15.5	30.0	2.00	12.7	30.0	2.00	11.7	30.0	NS
TTHL (FALL TIME) BIT# 11	2.00	14.7	30.0	2.00	11.7	30.0	2.00	10.8	30.0	NS
TTHL (FALL TIME) BIT# 12	2.00	16.3	30.0	2.00	13.0	30.0	2.00	12.1	30.0	NS
TTHL (FALL TIME) EOC	2.00	11.6	30.0	2.00	9.20	30.0	2.00	8.15	30.0	NS
TTHL (FALL TIME) SDO	2.00	13.8	30.0	2.00	11.4	30.0	2.00	9.70	30.0	NS
TPLH FROM CLK TO BIT# 1	20.0	71.0	160.	20.0	76.0	160.	20.0	85.5	160.	NS
TPLH FROM CLK TO BIT# 2	20.0	68.0	160.	20.0	70.0	160.	20.0	77.0	160.	NS
TPLH FROM CLK TO BIT# 3	20.0	68.5	160.	20.0	70.5	160.	20.0	78.5	160.	NS
TPLH FROM CLK TO BIT# 4	20.0	68.5	160.	20.0	70.0	160.	20.0	77.5	160.	NS
TPLH FROM CLK TO BIT# 5	20.0	67.0	160.	20.0	69.0	160.	20.0	77.0	160.	NS
TPLH FROM CLK TO BIT# 6	20.0	68.0	160.	20.0	69.5	160.	20.0	76.0	160.	NS
TPLH FROM CLK TO BIT# 7	20.0	68.5	160.	20.0	70.5	160.	20.0	78.0	160.	NS
TPLH FROM CLK TO BIT# 8	20.0	69.5	160.	20.0	71.5	160.	20.0	79.0	160.	NS
TPLH FROM CLK TO BIT# 9	20.0	67.5	160.	20.0	69.5	160.	20.0	77.0	160.	NS
TPLH FROM CLK TO BIT# 10	20.0	67.5	160.	20.0	70.0	160.	20.0	77.5	160.	NS
TPLH FROM CLK TO BIT# 11	20.0	68.5	160.	20.0	70.5	160.	20.0	78.0	160.	NS
TPLH FROM CLK TO BIT# 12	20.0	70.0	160.	20.0	70.5	160.	20.0	78.0	160.	NS
TPLH FROM CLK TO EOC	20.0	62.0	160.	20.0	64.5	160.	20.0	72.0	160.	NS
TPLH FROM CLK TO SDO	20.0	59.0	160.	20.0	60.5	160.	20.0	68.0	160.	NS
TPHL FROM CLK TO BIT# 1	20.0	70.5	160.	20.0	78.0	160.	20.0	70.5	160.	NS
TPHL FROM CLK TO BIT# 2	20.0	65.0	160.	20.0	63.0	160.	20.0	60.0	160.	NS
TPHL FROM CLK TO BIT# 3	20.0	65.5	160.	20.0	63.5	160.	20.0	60.5	160.	NS
TPHL FROM CLK TO BIT# 4	20.0	65.5	160.	20.0	63.5	160.	20.0	60.0	160.	NS
TPHL FROM CLK TO BIT# 5	20.0	66.0	160.	20.0	63.5	160.	20.0	59.5	160.	NS
TPHL FROM CLK TO BIT# 6	20.0	66.0	160.	20.0	63.5	160.	20.0	59.5	160.	NS
TPHL FROM CLK TO BIT# 7	20.0	66.5	160.	20.0	63.0	160.	20.0	59.0	160.	NS
TPHL FROM CLK TO BIT# 8	20.0	66.0	160.	20.0	63.5	160.	20.0	60.5	160.	NS
TPHL FROM CLK TO BIT# 9	20.0	65.5	160.	20.0	63.0	160.	20.0	60.0	160.	NS
TPHL FROM CLK TO BIT# 10	20.0	66.0	160.	20.0	63.0	160.	20.0	60.0	160.	NS
TPHL FROM CLK TO BIT# 11	20.0	65.0	160.	20.0	63.0	160.	20.0	59.5	160.	NS
TPHL FROM CLK TO BIT# 12	20.0	66.5	160.	20.0	65.5	160.	20.0	62.0	160.	NS
TPHL FROM CLK TO EOC	20.0	66.5	160.	20.0	48.5	160.	20.0	48.5	160.	NS
TPHL FROM CLK TO SDO	20.0	66.0	160.	20.0	66.0	160.	20.0	64.5	160.	NS

TABLE 9-5.

BIT ERROR DATA (NON-LINEARITY) DEVICE TYPE 5212

FOR DEVICE S/N 9 @ 25 DEGREES C (RANGE = 20.00 VOLTS)
(V+MAX= 10.0000 VOLTS)

TEST	DECIMAL ADDR	MEASURED VALUE	IDEAL VALUE	BIT ERROR	UNITS
1	1.000	9.99560	9.99512	98.83M	LSB
2	2.000	9.99250	9.99023	464.1M	LSB
3	4.000	9.98220	9.98047	354.5M	LSB
4	8.000	9.96150	9.96094	115.2M	LSB
5	16.00	9.92250	9.92188	127.9M	LSB
6	32.00	9.84410	9.84375	71.69M	LSB
7	64.00	9.68770	9.68750	41.03M	LSB
8	128.0	9.37600	9.37500	204.9M	LSB
9	256.0	8.75050	8.75000	102.3M	LSB
10	512.0	7.50070	7.50000	143.4M	LSB
11	768.0	6.25000	6.25000	0.000	LSB
12	1.024K	5.00020	5.00000	40.92M	LSB
13	1.280K	3.75030	3.75000	61.43M	LSB
14	1.536K	2.50080	2.50000	163.9M	LSB
15	1.792K	1.25090	1.25000	184.4M	LSB
16	2.048K	500.0001U	0.00000	102.3M	LSB
17	2.304K	-1.24940	-1.25000	122.9M	LSB
18	2.560K	-249.930M	-2.50000	460.8	LSB
19	2.816K	-3.74940	-3.75000	122.9M	LSB
20	3.072K	-5.00000	-5.00000	0.000	LSB
21	3.328K	-6.25090	-6.25000	-184.4M	LSB
22	3.584K	-7.49950	-7.50000	102.3M	LSB
23	3.840K	-8.74950	-8.75000	102.3M	LSB
24	3.968K	-9.37410	-9.37500	184.4M	LSB
25	3.904K	-9.06290	-9.06250	-92.03M	LSB
26	3.872K	-8.90620	-8.90625	10.16M	LSB
27	3.856K	-8.82830	-8.82813	-35.94M	LSB
28	3.848K	-8.78870	-8.78906	74.22M	LSB
29	3.844K	-8.77080	-8.76953	-259.8M	LSB
30	3.842K	-8.75720	-8.75977	525.4M	LSB
31	3.841K	-8.75420	-8.75488	139.8M	LSB

TABLE 9-6

BIT ERROR DATA (NON-LINEARITY) DEVICE TYPE 5212

FOR DEVICE S/N 9 @ 125 DEGREES C (RANGE = 20.00 VOLTS)
(V+MAX= 10.00 VOLTS)

TEST	DECIMAL ADDR	MEASURED VALUE	IDEAL VALUE	BIT ERROR	UNITS
1	1.000	9.99450	9.99512	-126.4M	LSB
2	2.000	9.99060	9.99023	74.80M	LSB
3	4.000	9.98060	9.98047	26.95M	LSB
4	8.000	9.96100	9.96094	12.89M	LSB
5	16.00	9.92180	9.92188	-15.43M	LSB
6	32.00	9.84360	9.84375	-30.65M	LSB
7	64.00	9.68720	9.68750	-61.51M	LSB
8	128.0	9.37560	9.37500	122.9M	LSB
9	256.0	8.75010	8.75000	20.51M	LSB
10	512.0	7.50050	7.50000	102.4M	LSB
11	768.0	6.25120	6.25000	245.8M	LSB
12	1.024K	4.99980	5.00000	-40.92M	LSB
13	1.280K	3.75020	3.75000	41.02M	LSB
14	1.536K	2.50080	2.50000	163.9M	LSB
15	1.792K	1.25120	1.25000	245.7M	LSB
16	2.048K	0.00000	0.00000	0.000	LSB
17	2.304K	-1.24980	-1.25000	41.02M	LSB
18	2.560K	-2.49930	-2.50000	143.4M	LSB
19	2.816K	-3.74900	-3.75000	204.7M	LSB
20	3.072K	-5.00020	-5.00000	-41.02M	LSB
21	3.328K	-6.25000	-6.25000	0.000	LSB
22	3.584K	-7.49940	-7.50000	122.7M	LSB
23	3.840K	-8.74890	-8.75000	225.0M	LSB
24	3.968K	-9.37340	-9.37500	327.7M	LSB
25	3.904K	-9.06180	-9.06250	143.4M	LSB
26	3.872K	-8.90550	-8.90625	153.5M	LSB
27	3.856K	-8.82740	-8.82813	148.4M	LSB
28	3.848K	-8.78780	-8.78906	258.6M	LSB
29	3.844K	-8.76870	-8.76953	170.3M	LSB
30	3.842K	-8.75880	-8.75977	197.7M	LSB
31	3.841K	-8.75420	-8.75488	139.9M	LSB

TABLE 9-7

BIT ERROR DATA (NON-LINEARITY) DEVICE TYPE 5212

FOR DEVICE S/N 9 @ -55 DEGREES C (RANGE = 20.00 VOLTS)
(V+MAX= 10.00 VOLTS)

TEST	DECIMAL ADDR	MEASURED VALUE	IDEAL VALUE	BIT ERROR	UNITS
1	1.000	9.99470	9.99512	-85.35M	LSB
2	2.000	9.99020	9.99023	-7.031M	LSB
3	4.000	9.98060	9.98047	26.95M	LSB
4	8.000	9.96090	9.96094	-7.615M	LSB
5	16.00	9.92170	9.92188	-35.74M	LSB
6	32.00	9.84330	9.84375	-92.18M	LSB
7	64.00	9.68700	9.68750	-102.3M	LSB
8	128.0	9.37540	9.37500	81.87M	LSB
9	256.0	8.74970	8.75000	-61.52M	LSB
10	512.0	7.50000	7.50000	0.000	LSB
11	768.0	6.25000	6.25000	0.000	LSB
12	1.024K	4.99970	5.00000	-61.43M	LSB
13	1.280K	3.74950	3.75000	-102.3M	LSB
14	1.536K	2.49980	2.50000	-40.92M	LSB
15	1.792K	1.24970	1.25000	-61.52M	LSB
16	2.048K	-200.0000	0.00000	-41.02M	LSB
17	2.304K	-1.25090	-1.25000	-184.4M	LSB
18	2.560K	-2.50070	-2.50000	-143.4M	LSB
19	2.816K	-3.75100	-3.75000	-204.9M	LSB
20	3.072K	-5.00110	-5.00000	-225.4M	LSB
21	3.328K	-6.25150	-6.25000	-307.4M	LSB
22	3.584K	-7.50120	-7.50000	-245.7M	LSB
23	3.840K	-8.75120	-8.75000	-245.7M	LSB
24	3.968K	-9.37600	-9.37500	-205.1M	LSB
25	3.904K	-9.06440	-9.06250	-389.1M	LSB
26	3.872K	-8.90810	-8.90625	-378.9M	LSB
27	3.856K	-8.83000	-8.82813	-384.0M	LSB
28	3.848K	-8.79100	-8.78906	-294.5M	LSB
29	3.844K	-8.77140	-8.76953	-382.8M	LSB
30	3.842K	-8.76110	-8.75977	-273.4M	LSB
31	3.841K	-8.75140	-8.75488	713.3M	LSB

/TABLE 9-8
MAJOR CARRY DATA (DIFFERENTIAL NON-LINEARITY) DEVICE 5212

FOR DEVICE S/N 9 @ 25 DEGREES C (RANGE = 20.00 VOLTS)

BIT#	MC(+)	MC(-)	UNITS
1	64.96M	474.6M	LSB
2	146.9M	-139.8M	LSB
3	-119.4M	-160.3M	LSB
4	-139.8M	-221.8M	LSB
5	-385.6M	-385.6M	LSB
6	-119.4M	-160.3M	LSB
7	-37.44M	-57.92M	LSB
8	24.00M	3.520M	LSB
9	-221.8M	-37.44M	LSB
10	64.96M	-2.624M	LSB
11	48.58M	105.9M	LSB
12	146.9M	228.8M	LSB

FOR DEVICE S/N 9 @ 125 DEGREES C (RANGE = 20.00 VOLTS)

BIT#	MC(+)	MC(-)	UNITS
1	187.8M	290.2M	LSB
2	392.6M	515.5M	LSB
3	-37.44M	105.9M	LSB
4	-78.40M	44.48M	LSB
5	-303.7M	-180.8M	LSB
6	24.00M	167.4M	LSB
7	64.96M	228.8M	LSB
8	85.44M	249.3M	LSB
9	85.44M	228.8M	LSB
10	24.00M	208.3M	LSB
11	3.520M	228.8M	LSB
12	187.8M	269.8M	LSB

FOR DEVICE S/N 9 @ -55 DEGREES C (RANGE = 20.00 VOLTS)

BIT#	MC(+)	MC(-)	UNITS
1	392.6M	495.0M	LSB
2	24.00M	126.4M	LSB
3	-78.40M	24.00M	LSB
4	-78.40M	24.00M	LSB
5	-303.7M	-262.7M	LSB
6	-57.92M	24.00M	LSB
7	24.00M	85.44M	LSB
8	64.96M	146.9M	LSB
9	64.96M	146.9M	LSB
10	24.00M	146.9M	LSB
11	85.44M	290.2M	LSB
12	146.9M	249.3M	LSB

TABLE 9-9. ZERO ERROR, ABSOLUTE END POINT ERROR
DEVICE 5212

S/N 9 @ 25°C

VCC	VEE	ZERO ERROR (VOLTS)	ABSOLUTE ERROR(+) (VOLTS)	ABSOLUTE ERROR(-) (VOLTS)
15.45V	-15.45V	2.50000M	9.99360	-9.99520
14.55V	-15.45V	2.20000M	10.0019	-10.0033
14.55V	-14.55V	2.30000M	9.98370	-9.98470
15.45V	-14.55V	2.30000M	9.98470	-9.98560

DEVICE S/N 9 @ 125°C

VCC	VEE	ZERO ERROR (VOLTS)	ABSOLUTE ERROR(+) (VOLTS)	ABSOLUTE ERROR(-) (VOLTS)
15.45V	-15.45V	400.000U	10.0097	-10.0080
14.55V	-15.45V	1.60000M	10.0079	-10.0077
14.55V	-14.55V	700.000U	9.98680	-9.98530
15.45V	-14.55V	0.00000	9.98780	-9.98600

DEVICE S/N 9 @ -55°C

VCC	VEE	ZERO ERROR (VOLTS)	ABSOLUTE ERROR(+) (VOLTS)	ABSOLUTE ERROR(-) (VOLTS)
15.45V	-15.45V	1.81000M	10.0009	-9.99720
14.55V	-15.45V	1.90000M	10.0000	-9.99660
14.55V	-14.55V	1.70000M	9.98360	-9.98080
15.45V	-14.55V	1.10000M	9.98460	-9.98110

SECTION X

ADJUSTABLE POSITIVE VOLTAGE REGULATORS

MIL-M-38510/117

TABLE OF CONTENTS

SECTION X

ADJUSTABLE POSITIVE VOLTAGE REGULATORS

MIL-M-38510/117

10.1 Introduction

Prior characterization efforts for RADC resulted in the development of slash sheet MIL-M-38510/107 for 3-terminal Fixed Positive Voltage Regulators. That slash sheet specified regulators with 5 Volts, 12 Volts, 15 Volts and 24 Volts which survey shows are the predominate positive supply voltage requirements for both digital or analog circuits.

New innovative IC and hybrid devices such as D/A & A/D Converters, incorporate precision circuitry and as such require tight tolerance supply voltages. In addition, most large systems require a variety of supply voltages to provide power for digital circuits, analog circuits, display circuits, transducers, etc. The logistic problems associated with the variety of voltages needed to power these devices can be greatly reduced by use of one or more adjustable voltage regulators together with a few standard value resistors.

Adjustable voltage regulators are available in several case sizes and current outputs. Device types 78G and 78MG were chosen for this characterization because of their similarity to the 78XX and 78MXX families. Device types LM117H and LM117K were chosen for this characterization because of their user acceptance. In addition, all device types were selected by a joint decision of RADC, the JC-41 Committee and the Circuit Design Engineering activity of GEOS.

Table 10-1 lists the device types specified for this characterization.

Table 10-1. Device Types Specified.

Device Type	Generic Type	Manufacturer	Voltage Output Range	Output Current	Case Type	No. of Terminals
11701	78MG	Fairchild	5V $\leq$Vo <30V	-0.5A	TO-5	4
11702	78G	Fairchild	5V $\leq$Vo <30V	-1.0A	TO-3	4
11703	LM117H	NSC	1.25V $\leq$Vo <37V	-0.5A	TO-5	3
11704	LM117K	NSC	1.25V $\leq$Vo <37V	-1.5A	TO-3	3

10.2 Description of Device Types

The major physical distinctions between the various voltage regulators characterized for this slash sheet are shown in Table 10-1. The major distinguishing features are: 1) voltage range, 2) maximum output current, 3) number of terminals and 4) case size. Whereas, the 4-terminal adjustable regulators are evolved from their fixed voltage counterparts by deleting the two internal resistors used to set the output voltage and by bringing the error amplifier summing point out of the case, the 3-terminal adjustable regulators represent a different approach in IC voltage regulator design and do not have 3-terminal fixed voltage counterparts.

All of these devices contain protective circuitry common to many of the available IC voltage regulators. These circuits include a) output current limiting, b) short circuit protection, c) safe operating area protection and d) thermal shut down. In addition, the regulators included in these slash sheets feature "band-gap" reference voltage circuitry to fix and stabilize the output voltage. These reference voltage circuits are characterized by improved noise and long-term-stability. Generally, these characteristics are 10-100 times better than those found in standard avalanche breakdown reference voltage zener diodes.

General block diagrams for the 4-terminal adjustable positive voltage regulator and the 3-terminal adjustable positive voltage regulator are, respectively, shown in Figures 10-1 and 10-2.

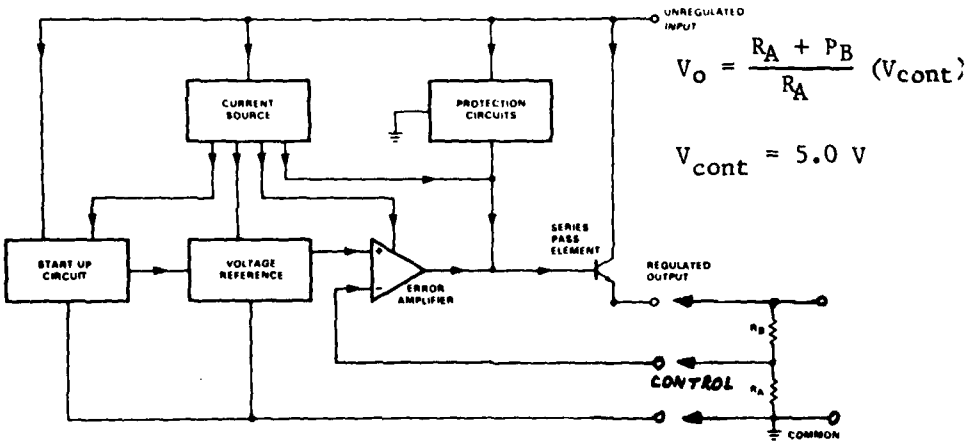


Figure 10-1. Block Diagram of 4-Terminal Adjustable Positive Voltage Regulators.)

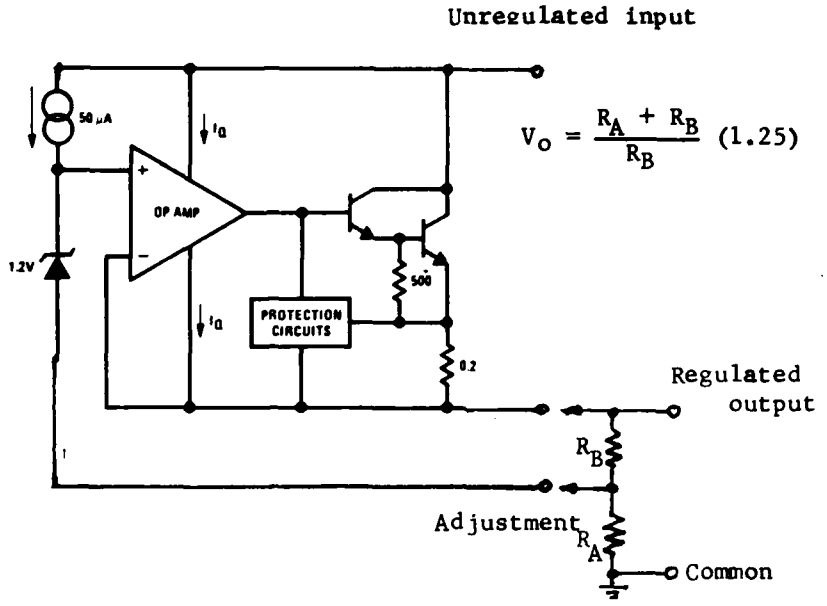


Figure 10-2. Block Diagram of 3-Terminal Adjustable Positive Voltage Regulators.)

The 4-terminal regulator circuits consist of a) a start-up circuit to insure that the device is rapidly brought into regulation, b) a temperature-compensated voltage reference with a current source to eliminate the effect of the unregulated input voltage, c) an error amplifier that compares a fraction of the output voltage with the internal reference voltage, d) a series pass regulating transistor that controls the current output to the load, e) a series resistor and current limit to regulate the peak output current, f) a safe operating area circuit which operates with the current limit to reduce the regulator's peak output current as the input voltage increases and g) a thermal shut-down circuit that turns off the pass transistor when its temperature exceeds 150°C - 190°C.

The 3-terminal adjustable voltage regulators vary markedly from the 4-terminal adjustable voltage regulators. The most outstanding features of the 3-terminal regulators are that a) the quiescent current flows out of the regulator output instead of flowing out of the regulator adj (common) pin, b) the only current flowing out of the regulator adj pin is a low level current (50 uA) for the reference circuit, c) the error amplifier is a fixed unity gain amplifier and is therefore easily frequency stabilized, d) the voltage reference circuit does not require a special start-up circuit and d) large voltage stresses are restricted to the series pass transistor and to the on-chip current sources. The

voltage (Vo - Vadj) is a constant 1.25 volts. In addition, circuit refinements have resulted in improved thermal and load regulation. A detailed discussion of the regulator circuits can be found in reference 2 of the bibliography.

10.3 Test Development

Devices used in these characterizations were selected by a joint decision of RADC, the JC-41 Committee and the Circuit Design Engineering activity of GEOS. The devices were obtained from two manufacturers on the JC-41 Committee and from their distributors. Table 10-2 lists the device types characterized.

Table 10-2. Device Types Characterized.

Device Type	S/N	Manufacturer	Date Codes
11701	1-5	Fairchild	7649, 7551, 7846
11702	1-5	Fairchild	7837
11703	1-10	NSC	7901
11704	1-10	NSC	7832

Test Parameter Development

Test parameters were recommended by the manufacturer and were approved by the JC-41 Committee. In addition, extra tests were added by GEOS to extend the characterization study beyond the recommended tests in Table I of the device slash sheet. Tests were performed at -55°C, 25°C and 125°C unless device performance was jeopardized by the test conditions (ie excessive power dissipation). One output voltage measurement was made at 150°C to check the low temperature limit of the thermal shut down operation mode. A list of the electrical parameters tested during characterization is presented in Table 10-3.

Table 10-3. Test Parameters for Characterization.

Test No	Symbol	Parameter
1	V_{OUT}	Output Voltage
2	V_{RLINE}	Line Regulation
3	V_{RLOAD}	Load Regulation
4	V_{RTH}	Thermal Regulation
5	I_{ADJ}	Adjustment Pin Current
6	I_{ADJ} (Line)	Adjustment Pin Current Line Regulation
7	I_{ADJ} (Load)	Adjustment Pin Current Load Regulation
8	I_{OS}	Output Short Circuit Current
9	I_{peak}	Output Current with Forced Output Voltage of 1.0 Volts
10	V_{OUT} (RECOV)	Output Voltage Recovery After Output Short Circuit
11	V_{START}	Output Voltage Start-up with Maximum Load
12	I_Q	Quiescent Current
13	$(V_{IN})/(V_{OUT})$	Ripple Rejection
14	N_o	Output Noise
15	$(V_{OUT})/V_{IN})$	Line Transient Response
16	$(V_{OUT})/(I_L)$	Load Transient Response

These parameters are arranged into two groups. One group of parameters, test number 1-12, consists of the static test parameters and includes all of those tests that can readily be performed on the Tektronix S-3260/70 Automatic Test Set. These tests are performed at three temperatures. The other group, test number 13-16, consists of the dynamic test parameters and includes those tests that can best be performed in a bench test set-up. These tests are performed at 25°C only.

Test Adapter Development

At the beginning test development, the accuracy and capability of the S-3260/70 Automatic Test Set is determined for each parameter. A table of this accuracy capability has been developed and is shown in Section II of this report. Because of basic tester limitations, several special circuits have been developed and are used on the interface test adapter to the S-3260/70. The schematic of the test adapter is shown in Figure 10-3.

The test adapter, shown in Figures 10-4 and 10-5, has been designed to provide an interface between the DUT and the Test System. The adapter has the ability to test positive and negative, 3-terminal and 4-terminal, 1/2 amp, 1 amp, 1.5 amp and 5 amp regulators. This capability is achieved by using a separate plug-in carrier for each type of DUT. The carrier contains the input and output capacitor for the

DUT, and plugs into the S-3260/70 main test adapter. In addition, diodes and transistors used in the test circuit are on separate carriers and sockets and are changed when the voltage polarity of the DUT to be tested is changed. Other components, such as, load resistors and output voltage fixing resistors, which are changed for the various device types are also mounted on plug-in carriers. Also the voltage measurement system has made extensive use of Kelvin test leads to insure that measurements are made at the precise point of interest (eg V_{OUT} is measured at the case).

The main DUT currents are carried by separate buses and are controlled by the automatic test system via the power Darlington transistor circuits. Through the use of external power supplies, the adapter test circuits permit control of currents that are larger than the current capacity of the automatic test system.

The input power Darlington transistor circuit can force the value of the DUT input voltage and can be used to control it for testing a) output voltage versus input voltage, b) line regulation, c) short circuit current versus input voltages, d) start up, e) line transient and f) ripple voltage rejection. The output power Darlington transistor circuit can be used to force a current and measure the voltage or to force a voltage and measure the current. The circuit can be controlled for testing a) output voltage versus load current, b) load regulation, c) thermal regulation, d) short circuit current, e) voltage recovery, and f) load transient. The current-to-voltage amplifier is used to measure the milliampere and microampere currents for a) the standby current drain tests, b) the control current tests, c) the adjust pin current tests and d) the quiescent current test under a forced voltage condition.

Tester Correlation

During the development of the S-3260/70 Automatic Tests, it is necessary to correlate the automatic test circuit to a basic test circuit. This is done for each parameter in accordance with the methods described in Section II of this report. All correlation data taken on the automatic tester and on a bench test set up agree within the "20% of parameter tolerance" criteria used by GEOS.

Dynamic tests for the voltage regulators include a) ripple rejection. b) line transient response, c) load transient response and d) output noise. No dynamic tests were run the 78MG or 78G because of their similarity to the 78MXX and 78XX voltage regulator families which were characterized on a previous contract.

Dynamic bench test circuit schematics are shown in Figures 10-6 thru 10-9. The noise test circuit schematic is shown in Figure 10-6. The test is performed using an oscilloscope with a differential preamplifier with bandwidth control. The bandwidth is set for a pass band from 10 Hz

to 10 kHz and the peak-to-peak measurement of the noise was made. The ripple rejection test circuit schematic is shown in Figure 10-7. The test is performed using the above oscilloscope. The bandwidth is adjusted to reduce the high frequency noise without affecting the 2400 Hz ripple frequency. The 2400 Hz ripple at the regulator is measured on the oscilloscope as a peak-to-peak voltage. Line transient response and load transient response test circuit schematics are shown in Figures 10-8 and 10-9. The peak measurements are made on an oscilloscope with a wide bandwidth pre-amp. Oscillographs of these tests are presented in Figures 10-10 and 10-11.

10.4 Test Results and Data

78MG and 78G Test Results

The 78MG and 78G Adjustable Positive Voltage Regulators meet all of the tested electrical specifications in the slash sheet. Because these devices have design characteristics similar to the 78MXX and 78XX series, the dynamic test were not performed. Typically, the measured data is in the middle of the specified tolerance band and the band spread appears to be reasonable for several parameters. However, the tolerance band spread for several of the parameters appears to be much greater than is necessary for even 100% yield. Typically data sheets for these two device types are shown in Tables 10-4 and 10-5, respectively. Tables 10-6 and 10-7, respectively, summarize the data distribution for these two device types.

Several 78G devices were destroyed during test, however, analysis of this problem revealed a tester problem. A negative voltage pulse was applied to the output of the DUT, by the tester, during the output short circuit current and voltage recovery test.

117H and 117K Test Results

Typical data sheets for the LM117H and LM117K are shown in Tables 10-8 and 10-9, respectively, and tables for data distribution are shown in Tables 10-10 and 10-11, respectively. All of the devices, except for one LM117H met all of the specifications on the slash sheet. This unit was further analyzed in a bench test set up using an oscilloscope. Pictures of the measurements were taken a) at the case, b) on the output lead 1/8 inch below the case, and c) on the output lead 3/8 inch below the case and are shown in Figures 10-12 thru 10-14, respectively. The load regulation measurements at these points were approximately 1 mV, 4.5 mV and 9 mV, respectively. Discussions with the manufacturer revealed that the leads on the TO-5 type cases are made of Kovar. The resistivity of Kovar can be as much as 28 times that of copper. This high resistivity is the reason for the high load regulation measurements. Other devices were checked in a bench test and similar results were observed.

Two units, serial numbers 5 and 6, failed thermal regulation at -55°C. Since this measurement is not recommended at either -55°C or 125°C, these devices were not considered failures. However, these two units were sent to the vendor for their measurement and analysis.

Tabulation of dynamic test data taken in a bench test set up for the LM117H Adjustable Positive Voltage Regulators is presented in Table 10-12. The tests were performed at 25°C and are of a) ripple rejection, b) output voltage noise, c) line transient response and d) load transient response. All of the bench measurements made on these devices were stable and showed reasonable safe margin for the recommended tolerances. Oscillographs of the line and load transient responses are shown in Figures 10-10 and 10-11. Dynamic test data and oscillographs were also obtained for the LM117K Adjustable Positive Voltage Regulators. These measurements were nearly identical to those taken on the LM117H regulators.

10.5 Discussion of Results

All of the test data taken on the 78MG and 78G voltage regulators was within the tolerances recommended by the manufacturer and the JC-41 Committee. The absolute measurements, such as, output voltage, standby current drain, output short circuit current and control current were reasonably centered between the hi-limit and the lo-limit of the test parameter. However, the test parameter such as line regulation, load regulation or change of standby current versus line voltage and load current had test parameter tolerances that were excessively conservative in light of the measured data. GEOS communicated this information to the manufacturer but, because of the extremely small characterization sample (ie 5 devices), was unsuccessful in promoting tighter test limits. The data distribution for these devices is presented in Tables 10-6 and 10-7.

A major test problem developed during the measurement of output short circuit current on the 78G devices. Although this test had been performed previously on the LM117 regulators without incident, three of the 78G regulators were destroyed during the test. An analysis of test circuit showed that a - 15 volt pulse was being applied to the regulator output from the load current amplifier as the forced output 0-volt condition was switched off. Since the summing point of th DUT error amplifier is connected directly to the DUT output for these tests, the negative voltage pulse is also applied directly to the summing point. Failure analysis showed that considerable chip distribution resulted during these failures. Both the test circuit and the controlling software were then modified to eliminate the negative voltage pulse. The burned out devices were replaced by the manufacturer and testing continued without incident. Testing of the LM117H and LM117K voltage regulators was performed on the same test adapter used for testing the 78MG and 78G voltage regulators. The

devices all met the parameter tolerances specified in Table I of the slash sheet, with one exception. This device failed load regulation as described in Section 10.4 As a result of the investigation of this failure, the slash sheet was modified to insure that the output voltages are made at the case of the DUT. GEOS believes that this measurement technique must be used to insure correlative test results between various test facilities. The remainder of the test measurements were reasonably well centered within the specified parameter tolerances. The data distribution for these devices is presented in Tables 10-10 and 10-11.

10.6 Slash Sheet Development

A modified Table I was received from each of the two manufacturer committee members supplying parts for the characterization. These parameters were modified to include a voltage recovery measurement after the output short circuit current test and a start up test with an R-C load. In general, the parameters and test circuits are the same as those used in MIL-M-38510/117 to test fixed positive voltage regulators. A summary of the MIL-M-38510/117 Table I is shown in Tables 10-13 and 10-14 for device types 11701 through 11704.

10.7 Conclusions and Recommendations

The test circuits used in these characterizations were developed for use either by an automatic tester or in a bench type set-up. Measurements were taken in both test set-ups and excellent tester correlation was observed. The test circuits are easily constructed; however, because of the high currents involved at the input and output of the DUT, a difference of several millivolts may be observed across a connector terminal. Extreme care must be observed to insure that the voltmeter sense leads are connected to the proper test points in the test circuit.

When the above procedures were properly observed, all of the devices perform well in their individual test circuits. The regulation tests have very conservative tolerances and could be easily reduced from their present ± 150mV limits. These limits could be reduced to ± 0 mV.

10.8 Bibliography

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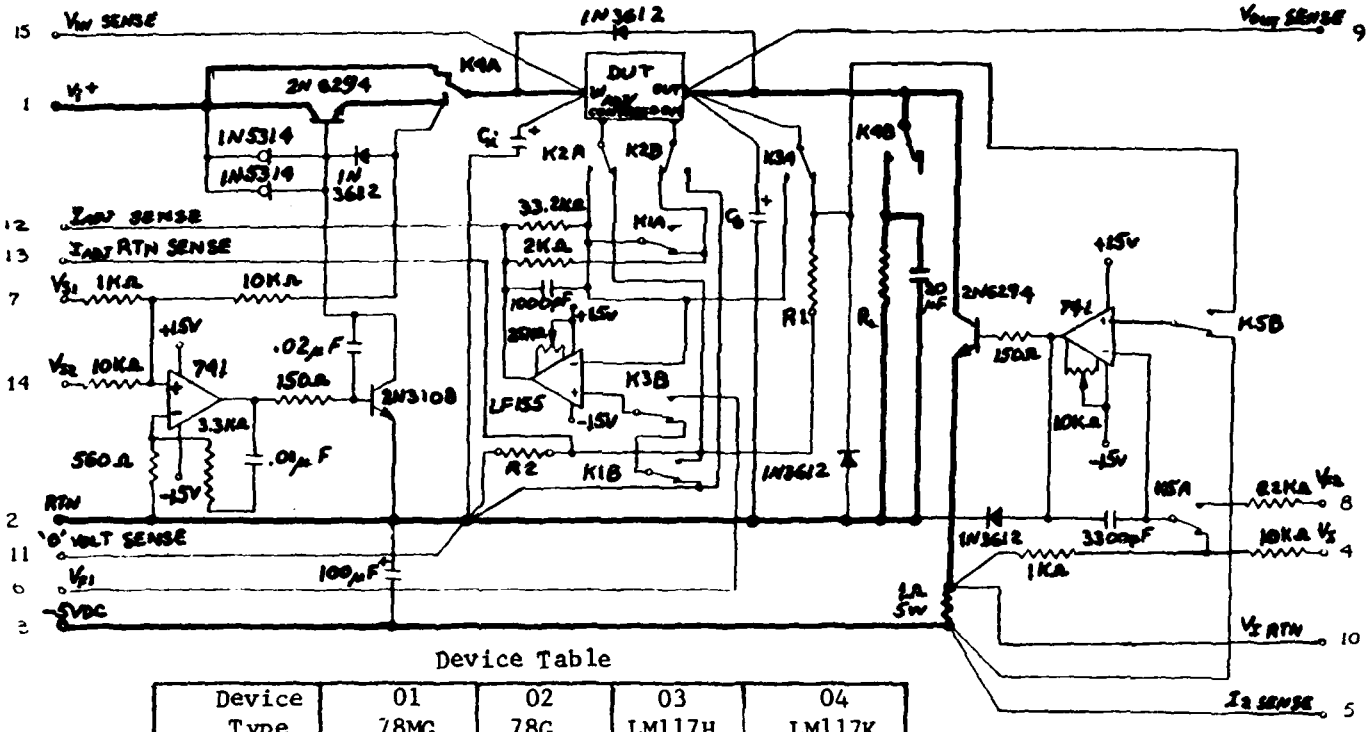


Device Table

Device Type	01 78MG	02 78G	03 LM117H	04 LM117K
R_1	0	0	249Ω	249Ω
R_2	5.0KΩ	5.0KΩ	0	0
R_L	10Ω	5Ω	2.5Ω	.833Ω
C_i	0.33uF	0.33uF	1.0uF	1.0uF
C_o	0.1uF	0.1uF	1.0uF	1.0uF

Figure 10-3. Positive voltage regulator test circuit for static tests.

Notes:

1. Heavy current paths ($I \geq 1.0A$) are indicated by bold lines.

2. Kelvin connections must be used for all output current and voltage measurements.

3. Op amp stabilization networks may vary with test adapter construction. Alternate drive circuits for the power transistor may be used to develop the proper load current and input voltage pulses.

4. Relay switch positions are defined in the appropriate Table III of the slash sheet.

5. Load currents of 5 mA are established via the load resistors R_1 and R_2. All other load currents shall be established via the pulse load circuit.

6. The pulse generator for the pulse load circuit shall have the following characteristics.

   a. Pulse amplitude = $-10(|I_L| - V_o/(R_1 + R_2)$ volts

   b. Pulse width = 1.0 mS (unless otherwise stated)

   c. Duty cycle = 2% (maximum)

7. Load circuits shall be determined by the voltage measured across the 1 ohm resistor. Measurements shall be made 0.5 ms after the start of the pulse.

8. V_{in} (LOW) and V_{in} (HIGH) per the appropriate Table III of the slash sheet.

9. $V_{RLINE} = V_B - V_A$

10. The output voltage is samples at specified intervals. Strobe pulse width is 100 us maximum.

11. $|I_L|$ (minimum) and $|I_L|$ (maximum) per the appropriate Table III of the slash sheet.

12. $V_{RLOAD} = V_D - V_C$

13. $V_{RTH} = V_D - V_E$

14. Force voltage, $V_I = -15$ volts; Relay K4 is energized.

15. $I_{OS} = (I_L)$ Amps

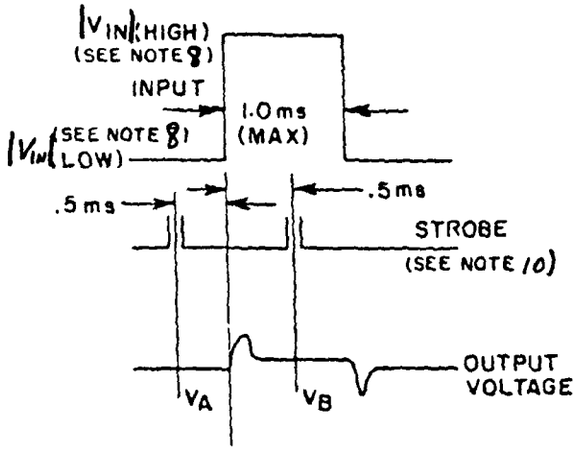
Figure 10-3. Positive voltage regulator test circuit for static tests. (cont'd)

16. $I_{pk} = (I_L + V_o/R_L + V_o/(R_1 + R_2)$ Amps

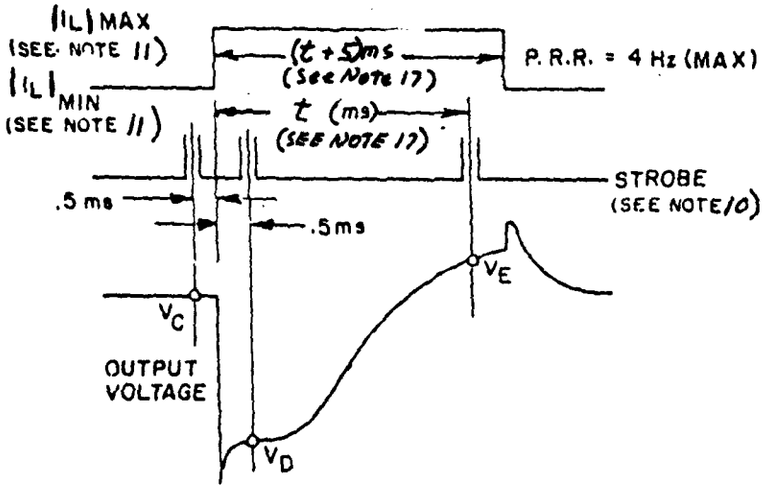
17. For device types 01 & 02, t = 10.5 msec.
    For device types 03 & 04, t = 20.5 msec.

Figure 10-3. Positivevoltage regulator test circuit for static tests. (cont'd)

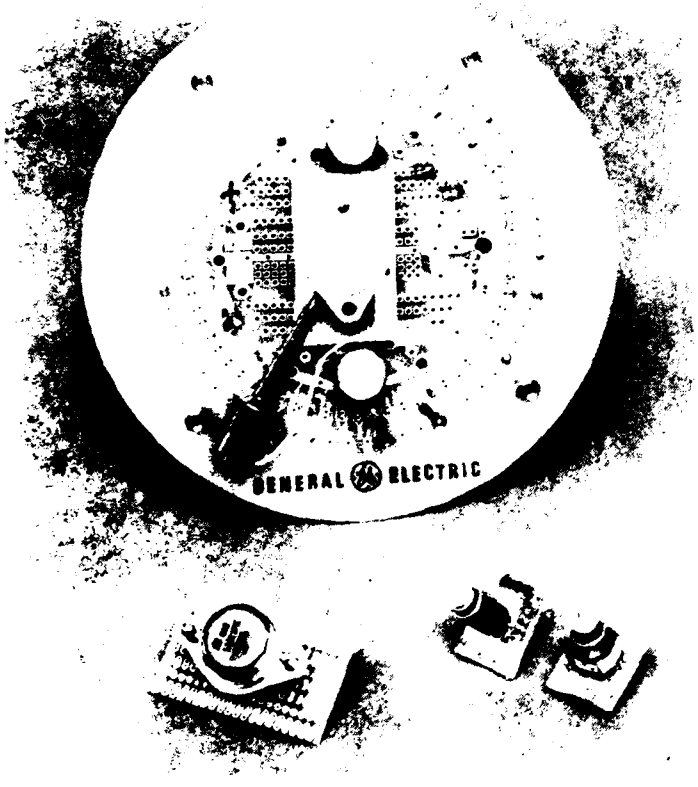
LINE REGULATION WAVEFORMS



LOAD REGULATION WAVEFORMS



igure 10-3. Positive voltage regulator test circuit for static tests (cont'd).

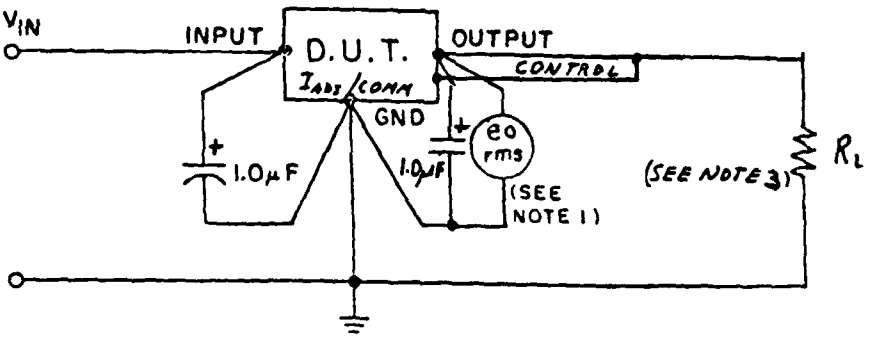


(Top View)

Figure 10-4 Voltage Regulator Test Adapter

(Bottom View)

Figure 10-5 Voltage Regulator Test Adapter



Device Table

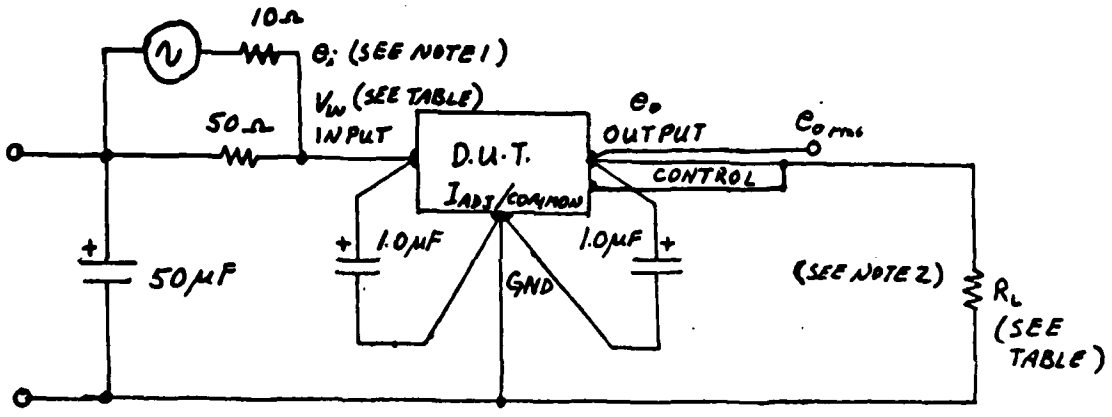
Device Type	01 78MG	02 78G	03 LM117H	04 LM117K
V_{IN}	10 V	10 V	6.25 V	6.25 V
R_L	100 ohm	50 ohm	25 ohm	12.5 ohm

The input 50 ohm resistor and R_L shall be type RER 70 or equivalent.

Notes:

1. The meter for measuring $e_o$rms shall have a minimum bandwidth from 10 Hz to 10 kHz and shall measure true rms voltages.
2. $N_o = e_o$ rms.
3. The control pin connection is required for device types 01 and 02 only.

Figure 10-6. Noise test circuit for positive voltage regulators.



Device Table

Device Type	01 78MG	02 78G	03 LM117H	04 LM117K
V_{IN}	10 V	10 V	6.25 V	6.25 V
R_L	40.2 ohm	14.3ohm	10 ohm	2.5 ohm

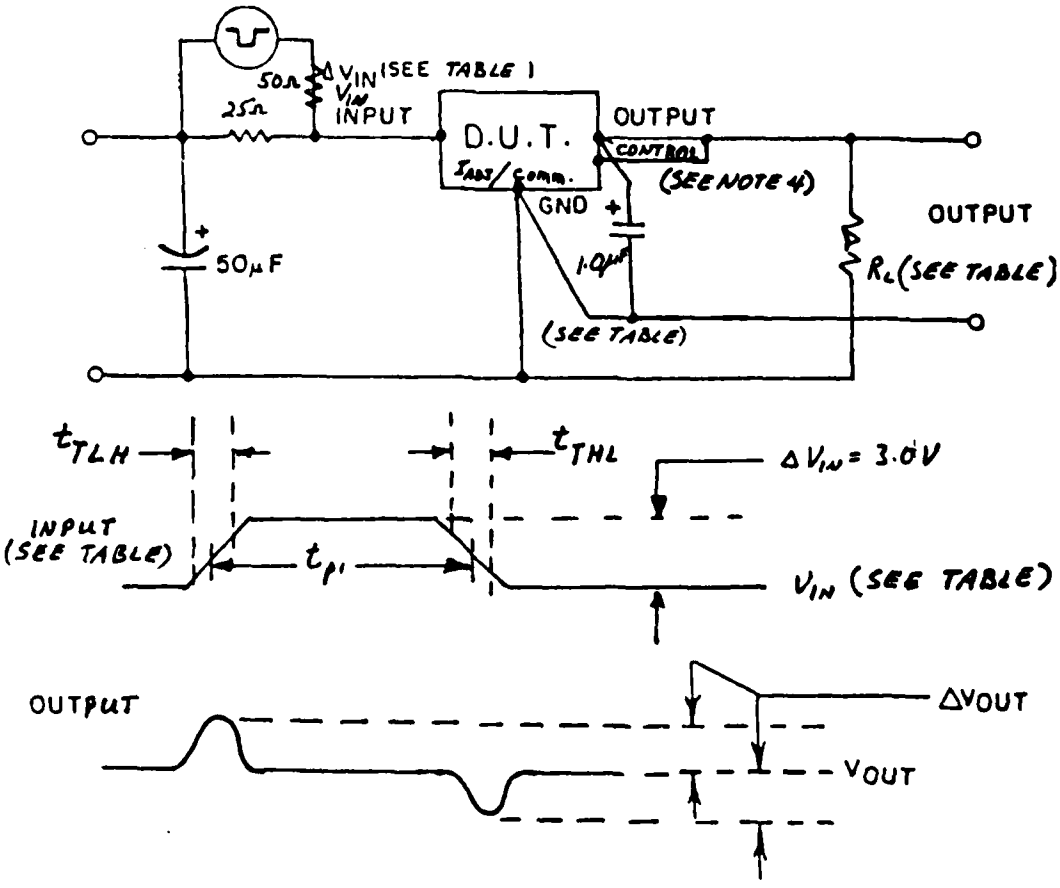
The input 50 ohm resistor and R_L shall be type RER 70 or equivalent.

Notes:

1. e_i = 1 Vrms f = 2400 Hz (measured at the input terminals of the DUT) ripple rejection = 2 - log $(e_i rms)/(e_o rms)$.

2. The control pin connection is required for device types 01 and 02 only.

Figure 10-7. Ripple rejection test circuit for positive voltage regulators.



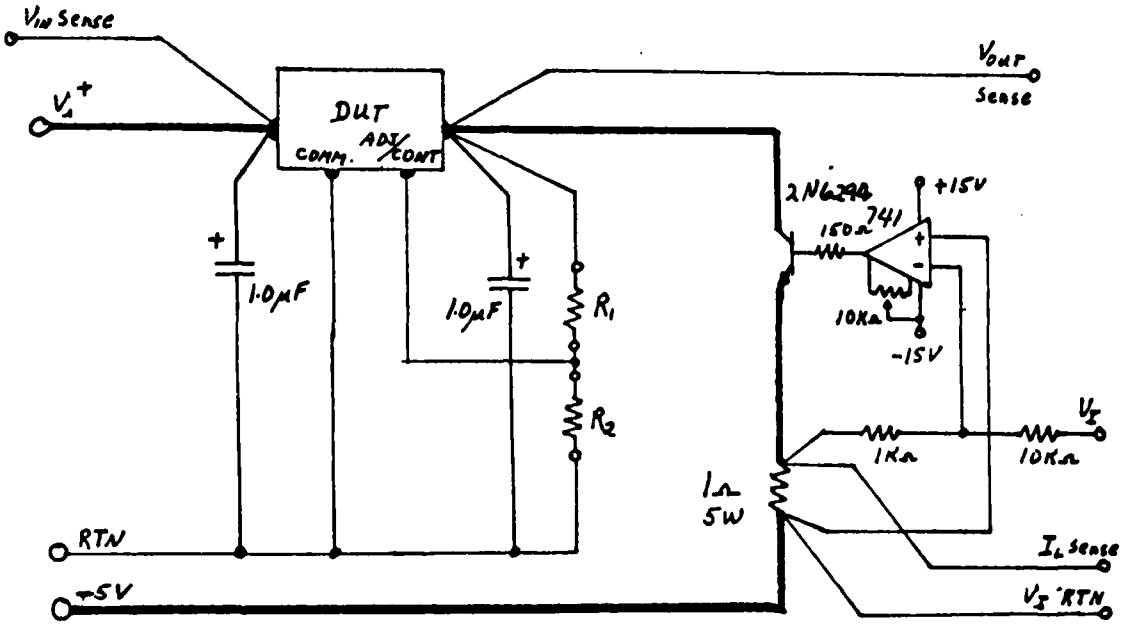
Device Table

Device Type	01 78MG	02 78G	03 LM117H	04 LM117G	Notes
V_{IN}	10 V	10 V	6.25 V	6.25 V	1
V_{IN}	3.0 V	3.0 V	3.0 V	3.0 V	1
R_L	1.25Kohm	1.25kohm	120ohm	120 ohm	
$t_{PHL}=t_{PLH}$	5.0us	5.0us	5.0us	5.0us	1

NOTES:

1. Measured at device input.
2. Pulse width tpl = 25 us; duty cycle = 3% (maximum).
3. Oscilloscope bandwidth = 5 MHz to 15 MHz.
4. The control pin connection is required for device types 01 and 02.

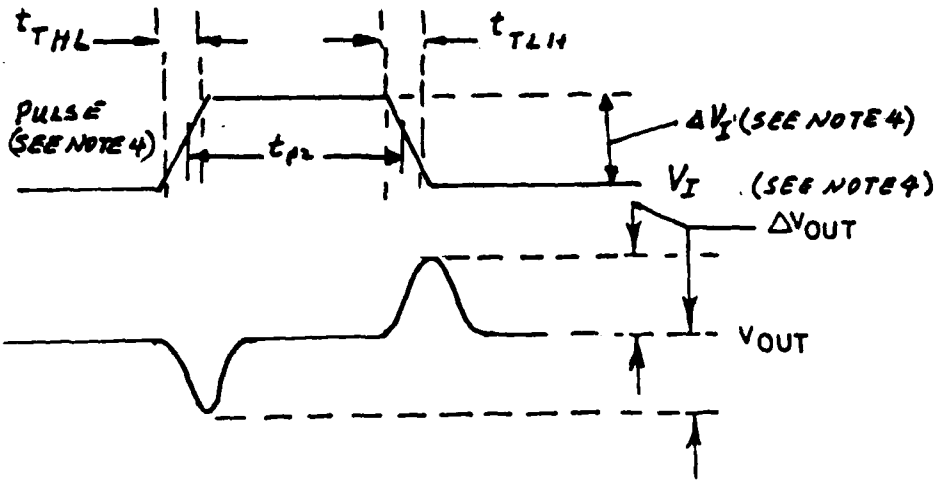
Figure 10-8. Line transient response test circuit for positive voltage regulators.



Device Table

Device Type	01 78MG	02 78G	03 LM117H	04 LM117G
R_1	0	0	249ohm	249ohm
R_2	5.0Kohm	5.0Kohm	0	0
I_L	-50mA	-100mA	-50mA	-100mA
I_L	-200mA	-400mA	-200mA	400mA
V_I	-0.49V	-0.99V	-0.45V	-0.95V
V_I	-2.0V	-4.0V	-2.0V	-4.0V

Figure 10.9. Load transient response test circuit for positive voltage regulators.



Notes:

1. Heavy current paths (I > 1.0A) are indicated by bold lines.
2. Kelvin connections must be used for all output current and voltage measurements.
3. Op amp stabilization networks may vary with test adapter construction. Alternate drive circuits for the 2N6294 may be used to develop the proper load current and input voltage pulses.
4. The pulse generator for the pulse load circuit shall have the following characteristics. (see device Table III)
   a. Voltage level (V_I) = - 10 (I_L - V_o)/(R_1 + R_2) volts.
   b. Pulse width (t_{p2}) = 25 u sec.
   c. Duty cycle = 3% (maximum).
   d. t_{THL} = t_{TLH} = 1.0 usec for device types 01 and 02.
   e. tT_{HL} = t_{TLH} = 5.0 usec for device types 03 and 04.
   f. Difference voltage level (delta V_I) = 10 (I_L) volts.
5. a. delta Vout = 500 mV maximum for device type 01.
   b. delta Voput = 1000 mV maximum for device type 02.
   c. delta Vout = 120 mV maximum for devices type 03 and 04.
   (These values guarantee the specified limits for load transient response.)
6. Oscilloscope minimum bandwidth shall be 9 MHz to 15 MHz.

Figure 10-9. Load transient response test circuit for positive voltage regulators (cont'd.).

LM117H Load Regulation

V = 5 mV/cm
H = .2 ms/cm

Unit #4

Figure 10-10. Oscillograph of LM117H load regulation measured at the case.

LM117K Load Regulation

V = 5 mV/cm
H = .2 ms/cm

Unit #4

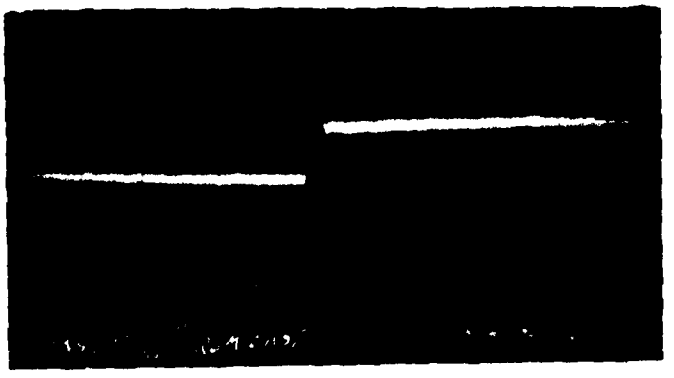


Figure 10-11. Oscillograph of LM117H load regulation measured 1/8" below case.

LM117H Load Regulation

V = 5 mV/cm
H = .2 ms/cm

Unit #4

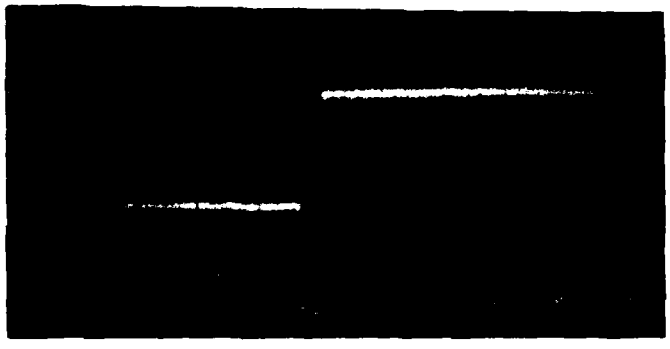


Figure 10-12. Oscillograph of LM117H load regulation measured 3/8" below case.

LM117H Line Transient Response

V/cm = 5 mV
Time/cm = 5 us

Unit #2

Figure 10-13. Oscillograph of LM117H line transient response test.

LM117H Load Transient Response

V/cm = .02 Unit #10
Time/cm = 5 us

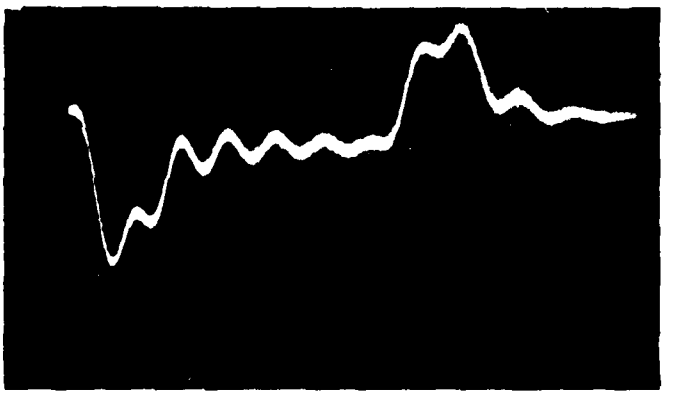


Figure 10-14. Oscillograph of LM117H load transient response test.

Table 10-4.

POS. ADJ. VOLTAGE REGULATORS-78MG ; TEMPERATURE: 25 DEG C ; 20 NOV 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI-LIMIT	UNITS
VOUT1	8.00	-5	4.750	4.968	4.930	4.964	4.915	4.984	[illegible]	C
VOUT2	8.00	-500	4.750	4.948	4.909	4.944	4.895	4.964	[illegible]	C
VOUT3	20.00	-5	4.750	4.957	4.930	4.964	4.916	4.984	[illegible]	C
VOUT4	20.00	-500	4.750	4.950	4.919	4.954	4.904	4.973	[illegible]	C
VOUT5	30.00	-5	4.750	4.957	4.930	4.964	4.917	4.984	[illegible]	C
VOUT6	30.00	-50	4.750	4.965	4.931	4.967	4.918	4.988	[illegible]	C
VRLINE1	8.00 30.00	-50	-150.0M	-1.560M	-1.620M	-770.1U	-10.01U	-1.160M	150.0M	V
VRLINE2	8.00 25.00	-350	-50.00M	-8.050M	-13.49M	-11.27M	-13.54M	-10.38M	50.00M	V
VRLOAD1	10.00	-5 -500	-100.0M	-2.060M	-2.440M	-2.400M	-2.970M	-2.430M	100.0M	V
VRLOAD2	30.00	-5 -50	-150.0M	-620.4U	-970.4U	-1.580M	-840.2U	-680.0U	150.0M	V
VRTH	15.00	-500	-50.00M	0.000	-5.321M	-7.982M	-7.982M	-2.660M	50.00M	V
(IL APPLIED FOR 10.5MSEC.)										
ISCD1 (LINE)	10.00	-5	-7.000M	-2.883M	-2.858M	-3.064M	-3.062M	-2.952M	-500.0U	A
ISCD2 (LINE)	30.00	-5	-8.000M	-3.104M	-3.071M	-3.310M	-3.318M	-3.173M	-500.0U	A
DISCD1 (LINE)	8.00 30.00	-5	-1.000M	260.6U	230.1U	262.9U	268.1U	233.3U	1.000M	A
DISCD2 (LOAD)	10.00	-5 -500	-500.0U	4.034U	1.957U	2.523U	2.911U	2.166U	500.0U	A
ICTL	10.00	-350	10.00M	606.7N	561.5N	475.1N	394.0N	539.5N	5.000U	A
IOS1	8.00	VF=0U	-2.000	-960.0M	-895.0M	-895.0M	-865.0M	-960.0M	-10.00M	A
(VOUT, RECOV.			4.750	4.949	4.917	4.957	4.904	4.981	5.250	V
IOS2	10.00	VF=0U	-2.000	-930.0M	-865.0M	-870.0M	-830.0M	-930.0M	-10.00M	A
(VOUT, RECOV.			4.750	4.946	4.917	4.954	4.898	4.981	5.250	V
IOS3	25.00	VF=0U	-1.500	-616.0M	-514.5M	-530.5M	-390.5M	-573.0M	-10.00M	A
(VOUT, RECOV.			4.750	4.943	4.909	4.943	4.896	4.973	5.250	V
IOS4	30.00	VF=0U	-1.000	-507.5M	-399.0M	-419.5M	-239.5M	-463.0M	-10.00M	A
(VOUT, RECOV.			4.750	4.938	4.909	4.949	4.896	4.970	5.250	V
IPEAK	8.00	VF=VOUT-.48	-2.000	-988.0M	-945.0M	-948.2M	-937.6M	-1.012	-50.00M	A
(VOUT, RECOV.			4.750	4.951	4.920	4.959	4.904	4.986	5.250	V
VSTART	20.00	-500	4.750	4.957	4.930	4.962	4.920	4.991	5.250	V

NOTE #1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 10-5.

POS. ADJ. VOLTAGE REGULATORS-78G ; TEMPERATURE: 25 DEG C ; 16 NOV 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI-LIMIT	UNITS
VOUT1	8.00	-5	4.750	4.978	4.969	4.928	4.918	4.939	5.250	V
VOUT2	8.00	-1000	4.750	4.978	4.910	4.924	4.919	4.939	5.250	V
VOUT3	20.00	-5	4.750	4.973	4.918	4.926	4.921	4.939	5.250	V
VOUT4	20.00	-1000	4.750	4.974	4.913	4.929	4.922	4.941	5.250	V
VOUT5	30.00	-5	4.750	4.973	4.914	4.929	4.923	4.940	5.250	V
VOUT6	30.00	-100	4.750	4.973	4.916	4.931	4.924	4.939	5.250	V
VRLINE1	8.00 30.00	-100	-150.0M	690.0U	1.310M	1.350M	1.310M	710.0U	150.0M	V
VRLINE2	8.00 25.00	-50	-50.00M	2.430M	2.200M	2.350M	2.610M	2.170M	50.00M	V
VRLOAD1	10.00	-5 -1000	-100.0M	-490.2U	380.0U	-249.9U	380.0U	-519.8U	100.0M	V
VRLOAD2	30.00	-5 -100	-150.0M	-269.8U	210.3U	-239.8U	239.8U	-10.01U	150.0M	V
VRTH (IL APPLIED FOR 10.5Msec.)	15.00	-1000	-50.00M	5.321M	-2.661M	5.321M	0.000	5.321M	50.00M	V
ISCD1 (LINE)	10.00	-5	-7.000M	-2.977M	-3.073M	-3.012M	-3.083M	-3.087M	-500.0U	A
ISCD2 (LINE)	30.00	-5	-8.000M	-3.273M	-3.376M	-3.335M	-3.388M	-3.397M	-500.0U	A
DISCD1 (LINE)	8.00 30.00	-5	-1.000M	338.1U	327.8U	335.1U	331.2U	353.1U	1.000M	A
DISCD2 (LOAD)	10.00	-5 -1000	-500.0U	501.8N	-233.5N	-253.3N	-84.52N	605.8N	500.0U	A
ICTL	10.00	-50	10.00N	543.1N	445.2N	434.4N	418.8N	745.2N	5.000U	A
IOS1	8.00	UF=0U	-4.000	-2.175	-1.950	-2.035	-2.035	-2.065	-20.00M	A
(VOUT) RECOV.			4.750	4.970	4.912	4.933	4.925	4.936	5.250	V
IOS2	10.00	UF=0U	-4.000	-2.040	-1.855	-1.930	-1.940	-1.935	-20.00M	A
(VOUT) RECOV.			4.750	4.970	4.914	4.933	4.928	4.936	5.250	V
IOS3	25.00	UF=0U	-3.000	-1.400	-1.160	-1.215	-1.340	-1.235	-20.00M	A
(VOUT) RECOV.			4.750	4.962	4.904	4.928	4.920	4.930	5.250	V
IOS4	30.00	UF=0U	-2.000	-1.160	-950.0M	-1.025	-1.125	-1.036	-20.00M	A
(VOUT) RECOV.			4.750	4.957	4.900	4.926	4.922	4.926	5.250	V
IPEAK	8.00	UF=VOUT-.48	-4.000	-2.198	-2.032	-2.111	-2.094	-2.111	-1.000	A
(VOUT) RECOV.			4.750	4.967	4.918	4.930	4.925	4.933	5.250	V
VSTART	30.00	-1000	4.750	4.981	4.925	4.943	4.938	4.946	5.250	V

NOTE :1 UF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 10-6. 78MG Data Distribution & Parameter Limits.

PARAMETER ($-55^{o}C \leq T_A \leq 125^{o}C$)	* [///DATA////] * LL<-------LIMIT-------->HL	UNIT
Output Voltage	* [/////] * 4.75 . . . . 5 . . . . 5.25	V
Output Voltage ($T_A = 150^{o}C$)	* [/] * 4.75 . . . . 5 . . . . 5.25	V
Line Regulation 1	* [] * -150 . . . . . 0 150	mV
Line Regulation 2	* [] * -50 . 0 . 50	mV
Load Regulation 1	* [] * -100 . . . 0 . . . 100	mV
Load Regulation 2	* [] * -150 . . . . . 0 150	mV
Thermal Regulation ($T_A = 25^{o}C$)	* [] * -50 . 0 . 50	mV
Standby Current Drain 1	* [] * -7 0	mA
Standby Current Drain 2	* [] * -8 0	mA
Delta Standby Current Drain 1	* [] * -1 . . . 0 . . . 1	mV
Delta Standby Current Drain 2	* [] * -500 . . . . 0 500	uA

Table 10-6. 78 MG Data Distribution & Parameter Limits. (Continued)

PARAMETER ($-55^{o}C \leq T_A \leq 125^{o}C$)	* [///DATA////] * LL<-------LIMIT------->HL	UNIT
Control Current ($T_A = 25^{o}C$)	* [/] * .01 5	uA
Control Current	*[//] * .01 8	uA
Output Short Circuit Current 1 & 2 and peak output current	* [//] * -2.0 . . 0.5	A
Output Short Circuit Current 3	* [///] * -1.5 . . 0	A
Output Short Circuit Current 4	* [///] * -1.0 . 0	A

Table 10-7. 78G Data Distribution & Parameter Limits.

PARAMETER ($-55^{o}C \leq T_A \leq 125^{o}C$)	* [///DATA////] * LL<-------LIMIT------->HL	UNIT
Output Voltage	* [////] * 4.75 . . . . 5 . . . . 5.25	V
Output Voltage ($T_A = 150^{o}C$)	* [///] * 4.75 . . . . 5 . . . . 5.25	V
Line Regulation 1	* [] * -150 . . . . . 0 150	mV
Line Regulation 2	* [] * -50 . 0 . 50	mV
Load Regulation 1	* [] * -100 . . . 0 . . . 100	mV
Load Regulation 2	* [] * -150 . . . . . 0 150	mV
Thermal Regulation ($T_A = 25^{o}C$)	* [] * -50 . 0 . 50	mV
Standby Current Drain 1	* [/] * -7 0	mA
Standby Current Drain 2	* [] * -8 0	mA
Delta Standby Current Drain 1	* [] * -1 . . . 0 . . . 1	mV
Delta Standby Current Drain 2	* [] * -500 . . . . 0 500	uA

Table 10-7. 78G Data Distribution & Parameter Limits. (Continued)

PARAMETER ($-55^{o}C \leq T_A \leq 125^{o}C$)	* [///DATA////] * LL<-------LIMIT-------->HL	UNIT
Control Current ($T_A = 25^{o}C$)	*[] * .01 5	uA
Control Current	*[/] * .01 8	uA
Output Short Circuit Current 1 & 2 and peak output current	* [////] * -4.0 . . 1.0	A
Output Short Circuit Current 3	* [///] * -3.0 . . 0	A
Output Short Circuit Current 4	* [///] * -2.0 . 0	A

Table 10-8.

POS. ADJ. VOLTAGE REGULATORS-LM117H; TEMPERATURE: 25 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI-LIMIT	UNITS
VOUT1	+4.25	-5	1.200	1.236	1.249	1.245	1.233	1.251	1.300	V
VOUT2	+4.25	-500	1.200	1.228	1.242	1.237	1.225	1.242	1.300	V
VOUT3	+41.25	-5	1.200	1.240	1.254	1.251	1.239	1.257	1.300	V
VOUT4	+41.25	-50	1.200	1.239	1.252	1.249	1.239	1.256	1.300	V
VRLINE	+4.25 +41.25	-5	-9.000M	5.203M	5.316M	6.334M	5.429M	6.334M	9.000M	V
VRLOAD1	+6.25	-5 -500	-3.500M	-1.697M	-1.244M	-2.488M	-4.750M‡	-1.697M	3.500M	V
VRLOAD2	+41.25	-5 -50	-3.500M	-1.470M	-1.470M	-1.810M	-1.357M	-1.810M	3.500M	V
VRTH (IL APPLIED FOR 20.5msec.)	+41.25	-125	-5.000M	2.715M	3.619M	2.941M	678.7U	4.298M	5.000M	V
IADJ1 (LINE)	+4.25	-5	-100.0U	-41.48U	-49.48U	-56.82U	-42.99U	-57.38U	-15.00U	A
IADJ2 (LINE)	+41.25	-5	-100.0U	-41.97U	-50.07U	-57.58U	-43.53U	-58.16U	-15.00U	A
DIADJ1 (LINE)	+4.25 +41.25	-5	-5.000U	-490.0N	-593.0N	-762.5N	-533.5N	-771.0N	5.000U	A
DIADJ2 (LOAD)	+6.25	-5 -500	-5.000U	-575.0N	-705.0N	-768.0N	-510.5N	-861.0N	5.000U	A
IOS1 (VOUT)	+4.25 RECOV.	VF=0V	-1.800 1.200	-1.205 1.232	-1.240 1.244	-1.205 1.240	-1.255 1.227	-1.285 1.247	-500.0M 1.300	A V
IOS2 (VOUT)	+40.00 RECOV.	VF=0V	-500.0M 1.200	-260.0M 1.243	-210.0M 1.256	-195.0M 1.254	-280.0M 1.241	-195.0M 1.260	-50.00M 1.300	A V
IPEAK (VOUT)	+4.25 RECOV.	VF=+1.0V	-1.800 1.200	-1.210 1.232	-1.250 1.244	-1.200 1.239	-1.250 1.226	-1.285 1.246	-500.0M 1.300	A V
IQ1	+4.25	VF=+1.4V	-3.000M	-1.188M	-1.298M	-1.395M	-1.227M	-1.372M	-500.0U	A
IQ2	+14.25	VF=+1.4V	-3.000M	-1.440M	-1.568M	-1.713M	-1.498M	-1.685M	-500.0U	A
IQ3	+41.25	VF=+1.4V	-5.000M	-2.988M	-3.442M	-3.875M	-3.202M	-3.832M	-1.000M	A
VSTART	+4.25	-500	1.200	1.229	1.242	1.238	1.225	1.243	1.300	V

NOTE ‡1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 10-9.

POS. ADJ. VOLTAGE REGULATORS-LM117K; TEMPERATURE: 25 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI LIMIT	UNITS
VOUT1	+4.25	-5	1.200	1.249	1.249	1.239	1.240	1.248	1.300	V
VOUT2	+4.25	-1500	1.200	1.249	1.247	1.236	1.239	1.247	1.300	V
VOUT3	+41.25	-5	1.200	1.253	1.254	1.242	1.247	1.253	1.300	V
VOUT4	+41.25	-200	1.200	1.251	1.251	1.240	1.244	1.249	1.300	V
VRLINE	+4.25 +41.25	-5	-9.000M	3.959M	4.298M	3.506M	6.221M	4.072M	9.000M	V
VRLOAD1	+6.25	-5 -1500	-3.500M	226.3U	565.5U	452.4U	-1.131M	-339.4U	3.500M	V
VRLOAD2	+41.25	-5 -200	-3.500M	-1.810M	-1.810M	-1.923M	-2.715M	-2.375M	3.500M	V
VRTH (IL APPLIED FOR 20.5Msec.)	+41.25	-500	-5.000M	3.846M	4.637M	3.280M	2.036M	2.488M	5.000M	V
IADJ1 (LINE)	+4.25	-5	-100.0U	-56.66U	-56.10U	-52.02U	-54.31U	-59.98U	-15.00U	A
IADJ2 (LINE)	+41.25	-5	-100.0U	-57.05U	-56.47U	-52.29U	-54.83U	-60.34U	-15.00U	A
DIADJ1 (LINE)	+4.25 +41.25	-5	-5.000U	-392.0N	-373.5N	-276.0N	-513.5N	-357.0N	5.000U	A
DIADJ2 (LOAD)	+6.25	-5 -1500	-5.000U	-214.5N	-272.5N	-152.0N	-63.50N	-141.0N	5.000U	A
IOS1 (VOUT)	+4.25 RECOV.	VF=0V	-3.500 1.200	-2.905 1.250	-2.495 1.251	-2.710 1.240	-2.565 1.241	-2.730 1.248	-1.500 1.300	A V
IOS2 (VOUT)	+40.00 RECOV.	VF=0V	-1.000 1.200	-495.0M 1.254	-445.0M 1.253	-455.0M 1.242	-465.0M 1.246	-400.0M 1.253	-180.0M 1.300	A V
IPEAK (VOUT)	+4.25 RECOV.	VF=+1.0V	-3.500 1.200	-2.490 1.251	-2.330 1.249	-2.430 1.239	-2.330 1.240	-2.220 1.248	-1.500 1.300	A V
IQ1	+4.25	VF=+1.4V	-3.000M	-1.370M	-1.392M	-1.252M	-1.117M	-1.443M	-500.0U	A
IQ2	+14.25	VF=+1.4V	-3.000M	-1.750M	-1.800M	-1.525M	-1.543M	-1.740M	-500.0U	A
IQ3	+41.25	VF=+1.4V	-5.000M	-3.845M	-3.903M	-3.395M	-3.593M	-3.922M	-1.000M	A
VSTART	+4.25	-1500	1.200	1.249	1.249	1.239	1.240	1.249	1.300	V

NOTE :1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 10-10. LM117H Data Distribution & Parameter Limits.

PARAMETER ($-55^{o}C \leq T_A \leq 125^{o}C$)	* [///DATA////] * LL<-------LIMIT------->HL	UNIT
Output Voltage	* [///////] * 1.20 . . . . . 1.30	V
Output Voltage ($T_A = 150^{o}C$)	* [/] 1.20 . . . . . 1.30	V
Line Regulation 1 ($T_A = 25^{o}C$)	* [/]* -9 . 0 . 9	mV
Line Regulation 1	* [/] * -23. . . . 0 23	mV
Load Regulation 1 ($T_A = 25^{o}C$)	*[//] * -3.5 0 3.5	mV
Load Regulation 1	* [///] * -12. . 0 . .12	mV
Load Regulation 2 ($T_A = 25^{o}C$)	*[] * -3.5 0 3.5	mV
Load Regulation 2	* [] * -12. . 0 . .12	mV
Thermal Regulation ($T_A = 25^{o}C$)	* [/]* -5 . 0 . 5	mV
Adjust Pin Current	* [/////] * -100 . . . . . -15	uA
Delta Adjust Pin Current (Line & Load)	*[///] * -5. . 0 . .5	uA

Table 10-10. LM117H Data Distribution & Parameter Limits. (Continued)

PARAMETER ($-55^{o}C \leq T_A \leq 125^{o}C$)	* [///DATA////] * LL<-------LIMIT-------->HL	UNIT
Minimum Load Current 1 & 2	* [///]* -3 . . . . -.5	mA
Minimum Load Current 3	* [/////] * -5 . . . . . -1	mA
Output Short Circuit Current 1 and peak output current	* [/] * -1.8. . . . . -.5	A
Output Short Circuit Current 2	*[/]* -.5 . -.05	A

Table 10-11. LM117K Data Distribution & Parameter Limits.

PARAMETER ($-55^{o}C \leq T_A \leq 125^{o}C$)	* [///DATA////] * LL<------LIMIT------>HL	UNIT
Output Voltage	* [//////] * 1.20 . . . . . 1.30	V
Output Voltage ($T_A = 150^{o}C$)	* [//////] * 1.20 . . . . . 1.30	V
Line Regulation 1 ($T_A = 25^{o}C$)	* [/]* -9 . 0 . 9	mV
Line Regulation 1	* [/] * -23. . . . 0 23	mV
Load Regulation 1 ($T_A = 25^{o}C$)	* [/] * -3.5 0 3.5	mV
Load Regulation 1	* [/] * -12. . 0 . .12	mV
Load Regulation 2 ($T_A = 25^{o}C$)	*[] * -3.5 0 3.5	mV
Load Regulation 2	* [/] * -12. . 0 . .12	mV
Thermal Regulation ($T_A = 25^{o}C$)	* [/]* -5 . 0 . 5	mV
Adjust Pin Current	* [//] * -100 . . . . . -15	uA
Delta Adjust Pin Current (Line & Load)	* [] * -5. . 0 . .5	uA

Table 10-11. LM117K Data Distribution & Parameter Limits. (Continued)

PARAMETER ($-55^{o}C \leq T_A \leq 125^{o}C$)	* [///DATA////] * LL<-------LIMIT-------->HL	UNIT
Minimum Load Current 1 & 2	* [///]* -3 . . . . -.5	mA
Minimum Load Current 3	* [//] * -5 . . . . . -1	mA
Output Short Circuit Current 1 and peak output current	*[/////]* -3.5 . . . -1.5	A
Output Short Circuit Current 2	*[/]* -1 . -.18	A

Table 10-12 POS. ADJ. VOLTAGE REGULATOR - LM117H T_A = 25°C 6-15-79 (cont'd).

PARAMETER	CONDITIONS	LO - LIMIT	S/N1	S/N2	S/N4	S/N5	S/N6	HI - LIMIT	UNITS
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = 6.25V e_i = 1 V_{RMS} @ 2400 Hz I_L = -125 mA	65	> 80	> 80	> 80	> 80	> 80	-	dB
V_{NO}	V_{IN} = 6.25 V I_L = -50 mA	-	100	100	95	100	100	120	uV_{RMS}
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = 6.25 V ΔV_{IN} = 3.0 V I_L = - 10 mA	-	1.6	1.6	1.6	2.0	1.6	6	mV/V
$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = 6.25 V I_L = - 50 mA ΔI_L = -200 mA	-	.25	.20	.20	.19	.18	0.6	mV/mA

Table 10-13 Electrical performance characteristics
(-55oC ≤ TA ≤ 125oC unless otherwise stated)

Characteristic	Symbol	Test Conditions	Device Type	Limits Min	Limits Max	Units
Output voltage	VOUT	VIN = 8V				
		IL = -5mA, -500mA	01	4.75	5.25	V
		IL = -5mA, -1.0A	02	4.75	5.25	V
		VIN = 30V				
		IL = -5mA, -50mA	01	4.75	5.25	V
		IL = -5mA, -100mA	02	4.75	5.25	V
		VIN = 38V				
		IL = -500mA	01	28.5	31.5	V
		IL = -1A	02	28.5	31.5	V
		VIN = 10V				
		IL = -5mA;TA=150oC	01,02	4.75	5.25	V
Line regulation	VRLINE	8V ≤ VIN ≤ 30V				
		IL = -50mA	01	-150	150	mV
		IL = -100mA	02	-150	150	mV
		8V ≤ VIN ≤ 25V				
		IL = -350mA	01	- 50	50	mV
		IL = -500mA	02	- 50	50	mV
Load regulation	VRLOAD	VIN = 10V				
		-500mA ≤ IL ≤ -5mA	01	-100	100	mV
		-1.0A ≤ IL ≤ -5mA	02	-100	100	mV
		VIN = 30V				
		-50mA ≤ IL ≤ -5mA	01	-150	150	mV
		-100mA ≤ IL ≤ -5mA	02	-150	150	mV
Thermal regulation	VRTH	VIN = 15V				
		IL = -500mA;TA=25oC	01	- 50	50	mV
		IL = -1.0A ;TA=25oC	02	- 50	50	mV
Standby current drain	ISCD	VIN = 10V				
		IL = -5mA	01,02	-7.0	-0.5	mA
		VIN = 30V				
		IL = -5mA	01,02	-8.0	-0.5	mA
Standby current drain change versus line voltage	D-ISCD (LINE)	8V ≤ VIN ≤ 30V				
		IL = -5mA	01,02	-1.0	1.0	mA
Standby current drain change versus load current	D-ISCD (LOAD)	VIN = 10V				
		-500mA ≤ IL ≤ -5mA	01	-0.5	0.5	mA
		-1.0A ≤ IL ≤ -5mA	02	-0.5	0.5	mA

Table 10-13 Electrical performance characteristics (Cont'd)
(55°C ≤ TA ≤ 125°C unless otherwise stated)

Characteristic	Symbol	Test Conditions	Device Type	Limits Min	Limits Max	Units
Control pin current	ICTL	VIN = 10V				
		IL = -350mA ;TA=25°C	01	- 5.0	-0.01	uA
		IL = -350mA	01	- 8.0	-0.01	uA
		IL = -500mA ;TA=25°C	02	- 5.0	-0.01	uA
		IL = -500mA	02	- 8.0	-0.01	uA
Output short circuit current	IOS1	VIN = 10V	01	- 2.0	-0.01	A
		VIN = 10V	02	- 4.0	-0.02	A
	IOS2	VIN = 30V	01	- 1.0	-0.01	A
		VIN = 30V	02	- 2.0	-0.02	A
Output voltage recovery after output short	VOUT (RECOV)	VIN = 10V;(after IOS1) RL = 10 ohms; CL=20uF	01	4.75	5.25	V
		RL = 5 ohms ; CL=20uF	02	4.75	5.25	V
		IN = 30V;(after IOS2) RL = 5 Kohms				
Voltage start-up	VSTART	VIN = 20V				
		RL = 10 ohms; CL=20uF	01	4.75	5.25	V
		RL = 5 ohms ; CL=20uF	02	4.75	5.25	V
Ripple rejection	D-VIN /D-VOUT	VIN = 10V ei = 1 VRMS;f=2400Hz				
		IL=-125mA ;TA=25°C	01	45	-	dB
		IL=-350mA ;TA=25°C	02	45	-	dB
Output noise voltage	No	VIN = 10V				
		IL = -50mA ;TA=25°C	01	-	125	uVr
		IL = -100mA;TA=25°C	02	-	250	uVr
Line transient response	D-VOUT /D-VIN	VIN = 10V D-VIN = 3V				
		IL = -5mA ;TA=25°C	01,02	-	30	mV/
Load transient response	D-VOUT /D-IL	VIN = 10V IL = -50mA ;TA=25°C				
		D-IL = -200mA	01	-	2.5	mV/
		VIN = 10V IL = -100mA;TA=25°C				
		D-IL = -400 mA	02	-	2.5	mV/

Table 10-14. Electrical performance characteristics.
($-55^{o}C \leq TA \leq 125^{o}C$ unless otherwise stated)

Characteristic	Symbol	Test Conditions	Device Type	Limits Min	Limits Max	Unit
Output voltage	VOUT	VIN = 4.25V				
		IL = -5mA, -500mA	03	1.20	1.30	V
		IL = -5mA, -1.5A	04	1.20	1.30	V
		VIN = 41.25V				
		IL = -5mA, -50mA	03	1.20	1.30	V
		IL = -5mA, -200mA	04	1.20	1.30	V
		VIN = 6.25V				
		IL = -5mA ;TA=150°C	03,04	1.20	1.30	V
Line regulation	VRLINE	$4.25V \leq VIN \leq 41.25V$				
		IL = -5mA ;TA=25°C	03,04	- 9	9	mV
		IL = -5mA	03	-23	23	mV
Load regulation	VRLOAD	VIN = 6.25V				
		$-500mA \leq TA \leq -5mA$				
		TA=25°C	03	-3.5	3.5	mV
		$-1.5mA \leq IL \leq -5mA$				
		TA=25°C	04	-3.5	3.5	mV
		$-500mA \leq IL \leq -5mA$	03	-12	12	mV
		$-1.5mA \leq IL \leq -5mA$	04	-12	12	mV
		VIN = 41.25V				
		$-50mA \leq IL \leq -5mA$				
		TA=25°C	03	-3.5	3.5	mV
		$-150mA \leq IL \leq -5mA$				
		TA=25°C	04	-3.5	3.5	mV
		$-50mA \leq IL \leq -5mA$	03	-12	12	mV
		$-150mA \leq IL \leq -5mA$	04	-12	12	mV
Thermal regulation	VRTH	VIN = 14.6V				
		IL = -750mA ;TA=25°C	03	- 5	5	mV
		IL = -1.5mA ;TA=25°C	04	- 5	5	mV
Adjust pin current	IADJ	VIN = 4.25V				
		IL = -5mA	03,04	-100	-15	uA
		VIN = 41.25V				
		IL = -5mA	03,04	-100	-15	uA
Adjust pin current change versus voltage	D-IADJ (LINE)	$4.25V \leq VIN \leq 41.25V$ IL = -5mA	03,04	- 5	5	uA line

Table 10-14. Electrical performance characteristics. (cont'd)
($-55^{o}C \leq TA \leq 125^{o}C$ unless otherwise stated)

Characteristic	Symbol	Test Conditions	Device Type	Limits Min	Limits Max	Unit
Adjust pin current change versus current	D-IADJ (LOAD)	VIN = 6.25V $-500mA \leq IL \leq -5mA$	03	- 5	5	uA load
		$-1.5A \leq IL \leq -5mA$	04	- 5	5	uA
Minimum load current	IQ	$4.25V \leq VIN \leq 14.25V$ (forced VOUT = 1.4V)	03,04	-3.0	-.5	mA
		VIN = 41.25 (forced VOUT = 1.4V)	03,04	-5.0	-.5	mA
Output short circuit current	IOS1	VIN = 4.25V	03	-1.8	- .5	A
			04	-3.5	-1.5	A
	IOS2	VIN = 40V	03	- .5	- .05	A
			04	-1.0	- .18	A
Output voltage recovery after output short	VOUT (RECOV)	VIN=4.25V (after IOS1) RL=2.5 ohms ; CL=20uF	03	1.20	1.30	V
		RL=0.83 ohms; CL=20uF	04	1.20	1.30	V
		VIN = 40V (after IOS2) RL = 250 ohms	03,04	1.20	1.30	V
Voltage start-up	VSTART	VIN = 4.25 RL=2.5 ohms ; CL=20uF	03	1.20	1.30	V
		RL=0.83 ohms; CL=20uF	04	1.20	1.30	V
Ripple rejection	D-VIN /D-VOUT	VIN = 6.25V ei = 1 Vrms; fo=2400Hz TA=25°C				
		IL = -125 mA	03	65	-	dB
		IL = -500 mA	04	65	-	dB
Output noise	No	VIN = 6.25V voltage TA=25°C				
		IL = -50 mA	03	-	120	uV
		IL = -100 mA	04	-	120	uV
Line transient response	D-VOUT /D-VIN	VIN = 6.25V D-VIN = 3.0V TA=25°C				
		IL = -10mA	03,04	-	6	mV/V
Load transient response	D-VOUT /D-IL	VIN = 6.25 TA=25°C IL = -50 mA				
		D-IL = -200 mA	03	-	0.6	mV/mA
		IL = -100 mA D-IL = -400 mA	04	-	0.3	mV/mA

SECTION XI

ADJUSTABLE POSITIVE VOLTAGE REGULATORS

MIL-M-38510/117

(3 amp & 5 amp Devices)

TABLE OF CONTENTS

SECTION XI

ADJUSTABLE POSITIVE VOLTAGE REGULATORS

MIL-M-38510/117

(3 amp & 5 amp Devices)

11.1 Introduction

Prior characterization efforts for this slash sheet included the 4-terminal -0.5A & -1.0A regulators and the 3-terminal -.5A and -1.5A regulators and is reported in Section X.

The growth of LSI and the expected growth of VLSI is placing more circuitry in a smaller volume. Regardless of the efforts to reduce the power requirements of the chip circuits, the total subsystem power requirements are expected to increase. This trend will prompt the need for larger voltage regulators capable of handling more current.

To meet the growing needs for higher current devices, RADC and the Circuit Design Engineering activity of GEOS proposed the addition of the LM150K and the LM138K Adjustable Positive Voltage Regulators to the slash sheet. These devices were chosen because a) they have electrical characteristics that are similar to device type 11703 and 11704 voltage regulators and b) they have complete socket interchangeability with the device type 11704 voltage regulator.

Table 11-1 lists the device types specified for this characterization.

Table 11-1 Device Types Specified.

Device Type	Generic Type	Manufacturer	Output voltage Range	Output Current	Case Type	No. of Terminals
11705	LM150K	NSC	$1.25V \leq VO \leq 37V$	-3.0A	TO-3	3
11706	LM138K	NSC	$1.25V \leq VO \leq 37V$	-5.0A	TO-3	3

11.2 Description of Device Types

The major physical distinctions for these devices are identical, except for output current capability, to those described for device type 11704 in Section X, Table 10-1. The 3-terminal adjustable positive voltage regulators all have very similar characteristics, and generally, show improved performance with increased output current. Both of these devices contain protective circuitry common to all of the IC voltage

regulators described in Sections X, XI and XII. The general block diagram for the 3-terminal adjustable positive voltage regulator is shown in Figure 11-1.

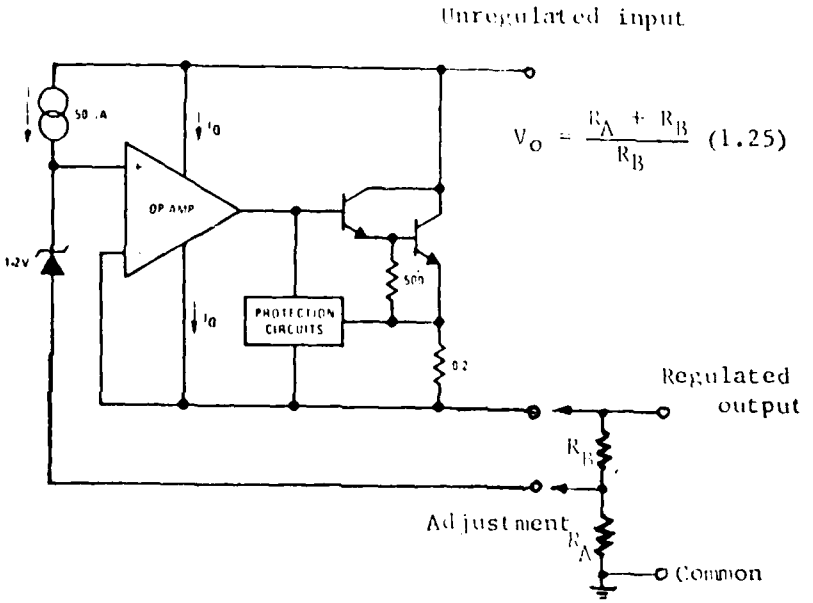


Figure 11-1. Block Diagram
of 3-Terminal Adjustable Positive Voltage Regulators

The 3-terminal adjustable voltage regulators described in this report all have similar design features. These features are a) the quiescent current flows out of the regulator output pin instead of flowing out of the regulator adj (common) pin, b) the only current flowing out of the regulator adj pin is a low level current (50 uA) for the reference circuit, c) the error amplifier is a fixed unity gain amplifier and is therefore easily frequency stabilized, d) the voltage reference circuit does not require a special start-up circuit and d) large voltage stresses are restricted to the series pass transistor and to the on-chip current sources. The voltage (Vo - Vadj) is a constant 1.25 volts. A detailed discussion of the regulator circuits can be found in reference 1 of the bibliography.

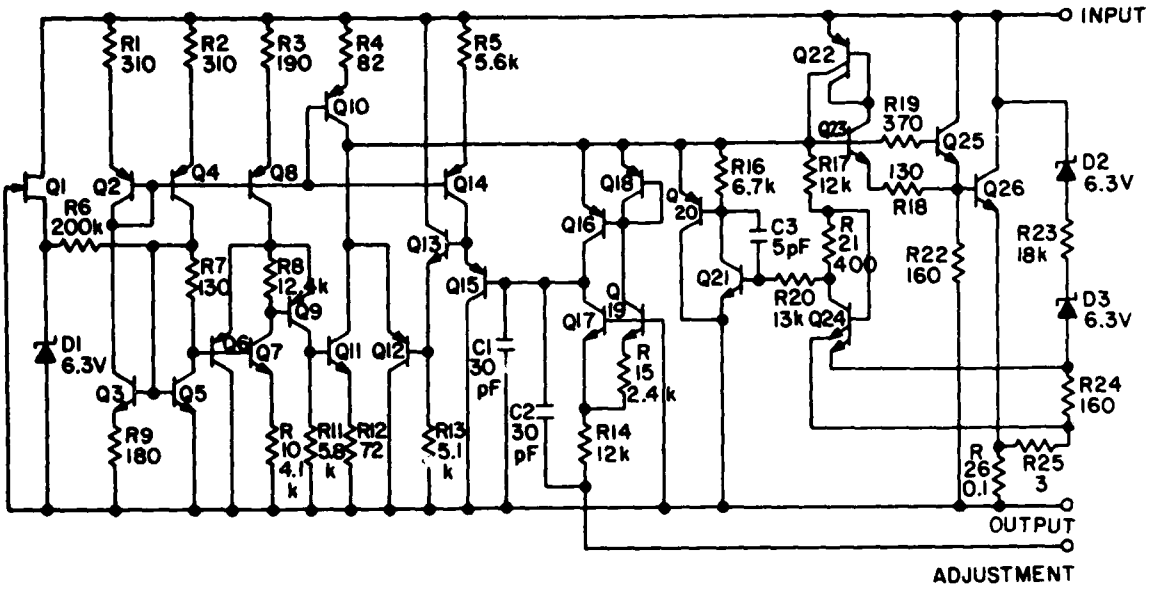


Figure 11-2. Schematic Diagram of 3-Terminal Adjustable Positive Voltage Regulator

The schematic presented in figure 11-2 represents a typical 3-terminal voltage regulator of the type characterized for this slash sheet. The typical features of these regulators are described as follows:

a) The current regulators, comprised of Q1, Q2, Q4, Q8, Q10 & Q14, supply constant current to sensitive parts of the voltage regulator and act as a buffer to render the regulator essentially insensitive to line voltage variations,

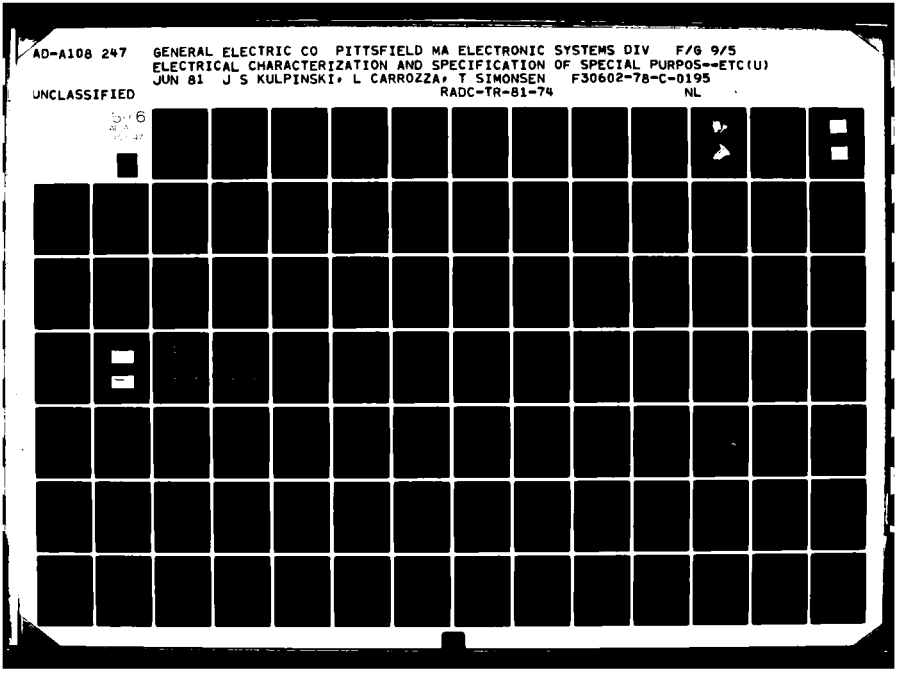
b) Transistors Q3, Q5, Q6, Q7 & Q9 provide the circuitry for the band gap voltage reference used to stabilize the regulator output voltage,

c) Transistors Q12 through Q19 make up the unity gain feedback amplifier,

d) Transistors Q20 & Q21 provide the circuitry for thermal shut-down,

e) Transistors Q22 through Q24 provide the circuitry for the current limit and the safe operating area protection circuits and

f) Transistors Q25 & Q26 make up the power Darlington regulating pass transistor.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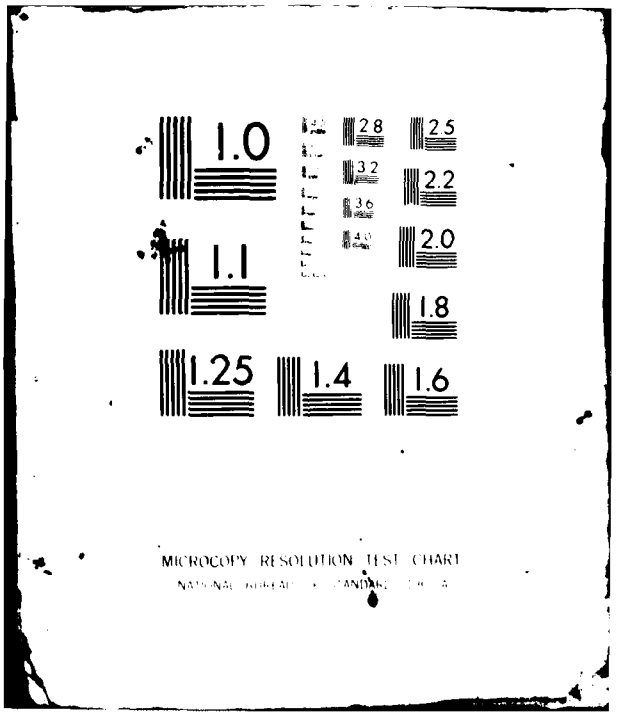
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1.1
1.25
1.4
1.6
2.8
3.2
3.6
4.0
2.5
2.2
2.0
1.8
MICROCOPY RESOLUTION TEST CHART

11-3 Test Development

Devices used in these characterizations were selected by a joint decision of RADC, and the Circuit Design Engineering activity of GEOS and were approved by the JC-41 Committee. The devices were obtained from National Semiconductor Corporation and from their distributors. Table 11-2 lists the device types characterized.

Table 11-2. Device Types Characterized.

Device Types	S/N	Manufacturer	Date Codes
11705	34-47	NSC	7846
11706	34-45	NSC	7911, 7917

Test Parameter Development

Test parameters were recommended by the manufacturer and are idential to those defined for device type 11704, except for output current. A list of the electrical parameters tested during characterization is repeated in Table 11-3 from Section X.

Table 11-3. Test Parameters for Characterization

Item No	Symbol	Parameter
1	V_{OUT}	Output Voltage
2	V_{RLINE}	Line Regulation
3	V_{RLOAD}	Load Regulation
4	V_{RTH}	Thermal Regulation
5	I_{ADJ}	Adjustment Pin Current
6	I_{ADJ} (Line)	Adjustment Pin Current Line Regulation
7	I_{ADJ} (Load)	Adjustment Pin Current Load Regulation
8	I_{OS}	Output Short Circuit Current
9	I_{peak}	Output Current with Forced Output Voltage of 1.0 Volts
10	V_{OUT} (RECOV)	Output Voltage Recovery After Output Short Circuit
11	V_{START}	Output Voltage Start-up with Maximum Load
12	I_Q	Quiescent Current
13	V_{IN}/V_{OUT}	Ripple Rejection
14	N_O	Output Noise
15	V_{OUT}/V_{IN}	Line Transient Response
16	V_{OUT}/I_L	Load Transient Response

Test Adapter Development

The development of the test adapter for use on the S-3260/70 Automatic Test Set evolved from the test adapter used for characterization of those devices described in Section X. A quick analysis of this test adapter showed that it was capable of testing with output currents as high as 5 amperes. GEOS decided, therefore, to test the LM150K and all the LM138K parameters with currents of 5 amperes or less by using the test adapter on the S3260/70. The schematic for this adapter is shown in Section X, Figure 10-3 and the adapter is shown in Figures 10-4 and 10-5.

For those LM138K parameters with load currents greater than 5 amperes, a separate test circuit was constructed. Because of the larger currents, the Darlington transistors, used to control the input voltage and the output current to the DUT, were replaced with larger devices. Thus, the general philosophy for testing voltage regulators was maintained. The entire test circuit, for testing with load currents greater than 5A, was constructed on a S3260/70 test adapter card and all tests were performed in a bench test set up. These measurements were a) VOUT with IL = 7.0 A and b) IOS where the peak value is specified as 16.0 A.

By using pulse generators, the load currents, short circuit currents and input voltages were pulsed at rates of one pulse per second to ensure that the average chip temperature remained at ambient. Measurements were made using an oscilloscope with a voltage comparator pre-amp. Scope probes were connected directly to the point to be measured.

A schematic of the test circuit for measuring the high current test parameters is shown in Figure 11-3 and the test adapter is shown in Figures 11-4 and 11-5.

The dynamic test circuit schematics are shown in Section X, Figures 10-6 through 10-9. Since the dynamic test conditions for testing LM150K and LM138K voltage regulators are identical with those required for testing LM117K voltage regulators, the same test circuits and test procedures described in Section X were used.

Burn-in

A burn-in rack was constructed and five each LM150K's and LM138K's were burn-in tested in accordance with the slash sheet. The preburn-in and burn-in schematics are shown in Figure 11-6 and 11-7. The pre-burn-in test is run for 4 hours at 25°C and the burn-in test is run for 168 hours at 125°C.

Tester Correlation

The test circuit was correlated by using an ammeter in series with a low level load current and by comparing this reading with the voltage measurement made on the oscilloscope. Also the steady state output voltage measurement was correlated between the oscilloscope measurement and a voltmeter measurement. Both readings correlated to within $\pm$ 5% of each other.

11.4 Test Results and Data

The static tests for the LM150K were performed on the S3260/70 Automatic Tester. Except for serial number 36, the LM150K voltage regulators passed all of the static and dynamic test limits. A summary of these test measurements is presented by showing data distribution and parameter limits in Table 11-4.

Serial number 36 of the LM150K voltage regulators failed the quiescent current (I_Q1) test. Investigations, proposed by the vendor, showed that the device failed to start without the proper load resistance (ie R_L = 249 ohm), with 1.4 volts applied to the output pin and with V_{in} = 4.25 V. Bench measurements were made by first turning on the device with R_L = 249 ohm, then applying 1.4 volts through an ammeter to the output, and finally removing the load resistor. The measured value for I_Q1 at 25°C was -730UA which of the 14 devices tested is the lowest value recorded for this parameter. A sample of the static test data taken at 25°C is presented in Table 11-5.

The static tests that were performed on the S3260/70 Automatic Tester for the LM138K regulators were all within the recommended test limits.

In addition, all of the bench test measurements for the LM138 with load currents greater than 5A met the slash sheet test requirements. A summary of these test measurements is presented by showing data distribution and parameter limits in Table 11-6. A sample of the static data taken at 25°C is presented in Table 11-7.

Tables 11-8, 11-9 and 11-10 list the mean values of data taken on each of the device type test parameters at 25°C, -55°C and 125°C. The tables include data for all of the 3-terminal devices, such as, the LM117H, LM117K, LM150K and LM138K. The comparison demonstrates the device data similarities of output voltage, adjust pin current and quiescent current. It also demonstrates the device data differences in regulation capabilities, and output short circuit current load.

A serious anomaly was detected during the output voltage measurement with a pulsed 7 ampere load current. As the load current was switched from 5 mA to 7A, the output voltage dropped out of regulation. Since

the load current is controlled via a current sink circuit connected to -7 Vdc, the output voltage dropped to a negative voltage. This, however, was limited by protection diodes in the test circuit. The output voltage recovered after a period of from 100 n sec to 600 n sec. As the rise time of the current pulse is varied from 20 usec to 80 usec, the dropout period decreases from its maximum time to zero time.

The two oscillographs in Figures 11-8 and 11-9 demonstrate the affect on the output voltage of a change in the current pulse rise time.

11.5 Discussion of Data

The data distribution summarized in Tables 11-4 and 11-6 demonstrates the band spread of the data versus the band spread of the limits for the LM150K and the LM137K devices, respectively. Because of the limited sample size of these parts, no statistical analysis was performed. The data shows that the distribution is generally narrow and within the band spread of the parameter limits.

One of the LM150K devices failed the quiescent current test. Analysis and investigation showed that the failure occurred because the part failed to start up in a totally unloaded condition. Since this represents an unrealistic user application, since the slash sheet specifies a 249 ohm resistor from output to adjust pins and since start-up testing is inherent in the test procedure, GEOS concludes that user oriented start-up problems will be readily detected. The failure is not one that would occur in a user application. In addition, the marginally low quiescent current did not degrade any of the other parameters.

All of the LM138K devices exhibited the same anomaly for fast rising current pulses. The oscillographs in Figures 11-8 and 11-9 demonstrate the affect of these pulses on output voltage.

As the rise time is slowed the output voltage drop out period decreases and is eventually eliminated. The addition of capacitance at the output of the regulator had the affect of slowing the rise time of the current pulse. Therefore, the slash sheet recommends that, in applications where fast rising high current pulses are anticipated, an output capacitor of 20 uF or more shall be used.

All of the devices passed the post burn-in tests performed on the S3260/70. One LM138K, serial number 44, was destroyed during the high current bench tests as a result of a set up fault. The remaining devices passed the postburn-in bench tests.

11.6 Slash Sheet Development

The slash sheet for these devices was essentially complete at the beginning of the characterization effort. Section X of this report describes the characterization effort that initiated slash sheet MIL-M-38510/117. The devices described in this section were added to MIL-M-38510/117. To do this, device types 11705 and 11706 were added to Tables I through IV of the slash sheet. Figure 17 was added to describe the test circuit required for the high current static tests and minor modifications to the text were required to include the new device type. The test circuit is presented in Figure 11-3.

A summary of the slash sheet Table I for device types 11705 and 11706, respectively, is presented in Table 11-11.

11.7 Conclusions and Recommendations

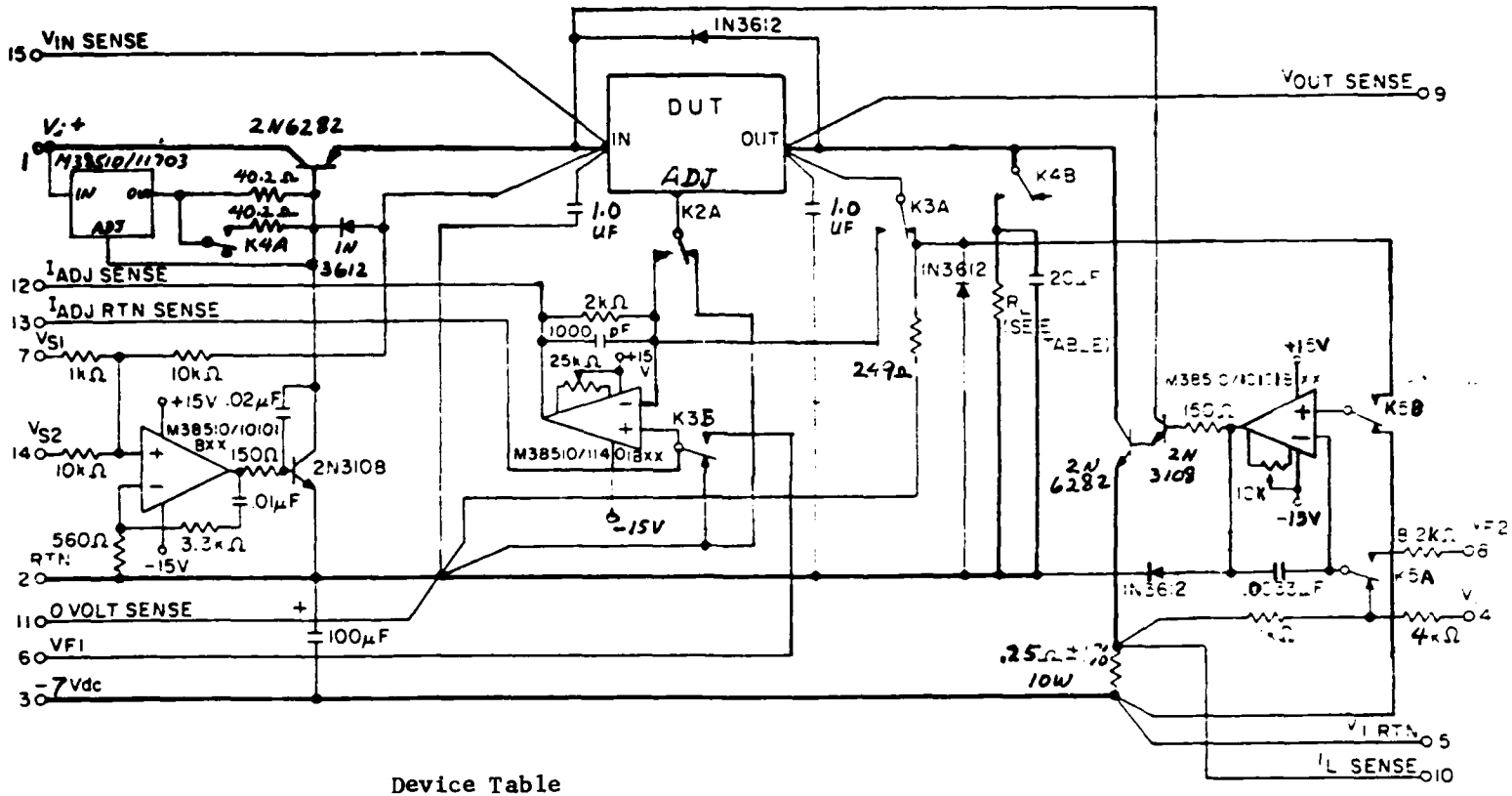
The test circuits used in these characterizations can be used either with automatic testers or in bench type set-ups. The test circuits are readily constructed; however, precautions must be taken in operating the circuits.

1. The circuits are designed for pulse operation and excessive power dissipation can damage some of the components.

2. High currents (ie. 7 amperes) will result in voltage measurement errors i.e. 7 millivolts/milliohm) unless differential voltage measurements are made directly at and across the points of interest.

In order to prevent excessive power dissipation during turn-on of the bench test circuit, GEOS recommends that normally closed relay contacts be added between the base and ground base and emitter of the output power transistor. This relay can be used to control current during power turn-on and turn-off. In addition, voltage sense lines of the input power transistor and between should be used abundantly and should be tied to or soldered to the point to be measured.

Many applications will require switching of heavy load currents at the output of the voltage regulator. For these applications, a large capacitor (ie. 20 uF or greater) should be connected between the regulator output and ground. When these recommendations are properly observed the test circuits and the devices perform "as advertized".

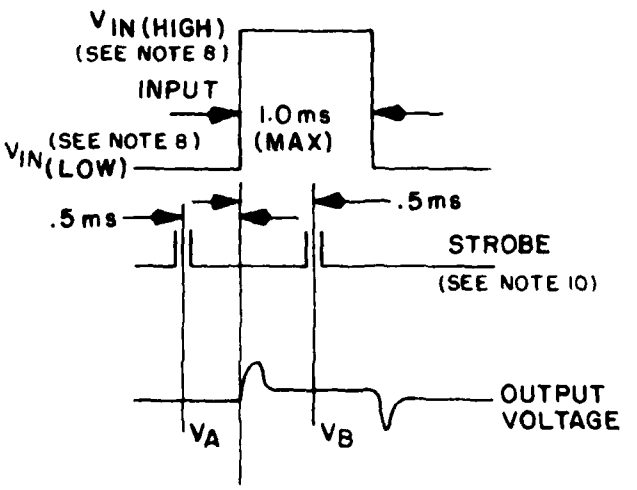


Device Table

Device Type	05	06
R_L	0.416Ω	0.25Ω

Figure 11-3. Test circuit for static tests for device types 05 and 06.

LINE REGULATION WAVEFORMS



LOAD REGULATION WAVEFORMS

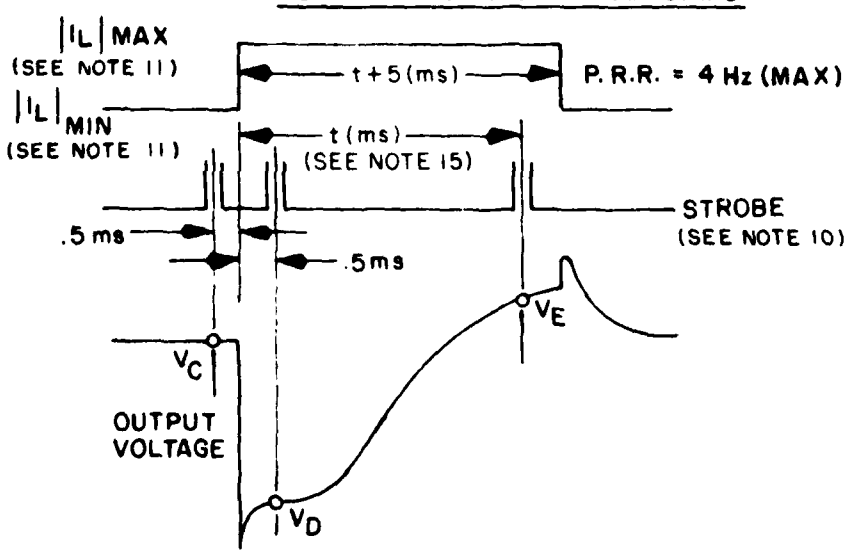


Figure 11-3. Test circuit for static tests for device types 05 and 06. (cont'd)

Notes:

1. Heavy current paths ($I < 1.0A$) are indicated by bold lines.

2. Kelvin connections must be used for all output current and voltage measurements.

3. Op amp stabilization networks may vary with test adapter construction. Alternate drive currents for the power transistor may be used to develop the proper load current and input voltage pulses.

4. Relay switch positions are defined in the appropriate Table III of the slash sheet.

5. Load currents of 5 mA are established via the load resistors R_1 and R_2. All other load currents shall be established via the pulse load circuit.

6. The pulse generator for the pulse load circuit shall have the following characterisitics.

   a. Pulse amplitude = $-10(I_L - V_o/(R_1 + R_2))$ volts

   b. Pulse width = 1.0 mS (unless otherwise stated)

   c. Duty cycle = 2% (maximum)

7. Load circuits shall be determined by the voltage measured across the 1 ohm resistor. Measurements shall be made 0.5 ms after the start of the pulse.

8. V_{in} (LOW) and V_{in} (HIGH) per the appropriate Table III of the slash sheet.

9. $V_{RLINE} = V_B - V_A$

10. The output voltage is samples at specified intervals. Strobe pulse width is 100 us maximum.

11. I_L (minimum) and I_L (maximum) per the appropriate Table III of the slash sheet.

12. $V_{RLOAD} = V_D - V_C$

13. $V_{RTH} = V_D - V_E$

14. Force voltage, V_I = - 15 volts; Relay K4 is energized.

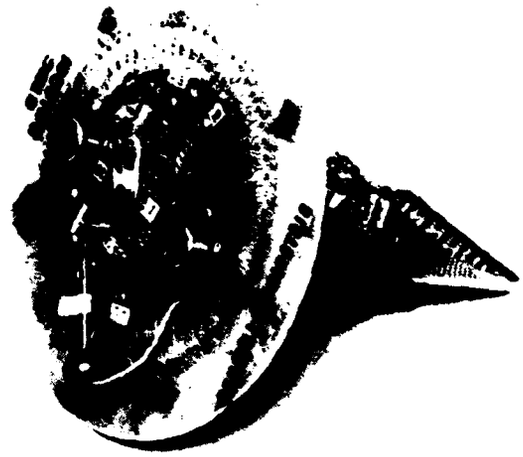
15. $I_{OS} = (I_L)$ Amps

Figure 11-3. Test circuit for static tests for device types 05 and 06.

16. $I_{pk} = (I_L + V_o/R_L + V_o/(R_1 + R_2)$ Amps

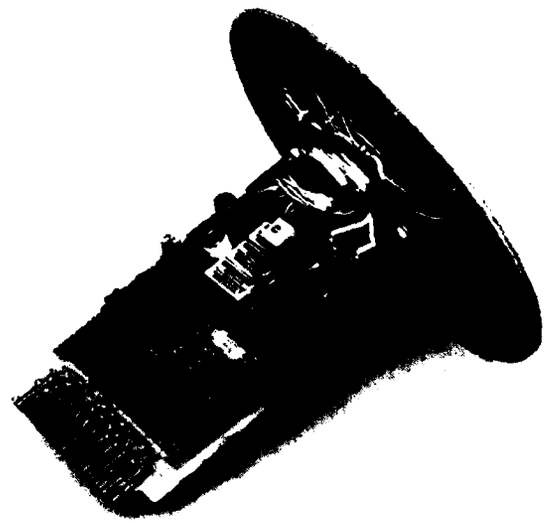
17. For device types 01 & 02, t = 10.5 msec.
For device types 03 & 04, t = 20.5 msec.

Figure 11-3. Test circuit for static tests for device types 05 and 06. (cont'd)



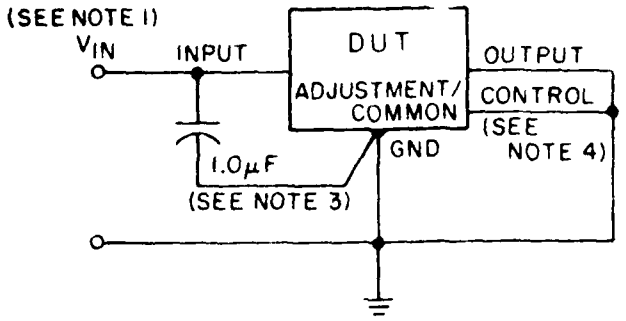
(Top View)

Figure 11-4 High Current Voltage Regulator Test Adapter



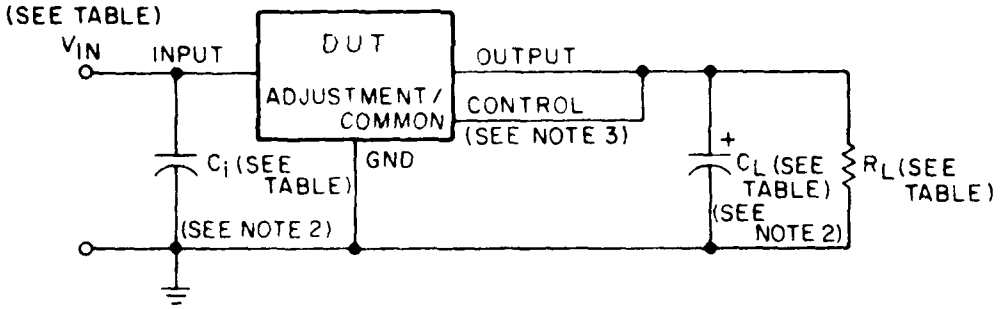
(Bottom View)

Figure 11-5 High Current Voltage Regulator Test Adapter



NOTES:
1. V_{IN} = 20 V.
2. Test is conducted at T_A = 25°C without a heat sink for a minimum of 4 hours.
3. The 1.0 μF capacitor may be reduced or eliminated provided the device remains stable.
4. The control pin connection is required for device types 01 and 02 only.

Figure 11-6. Pre burn-in test circuit.

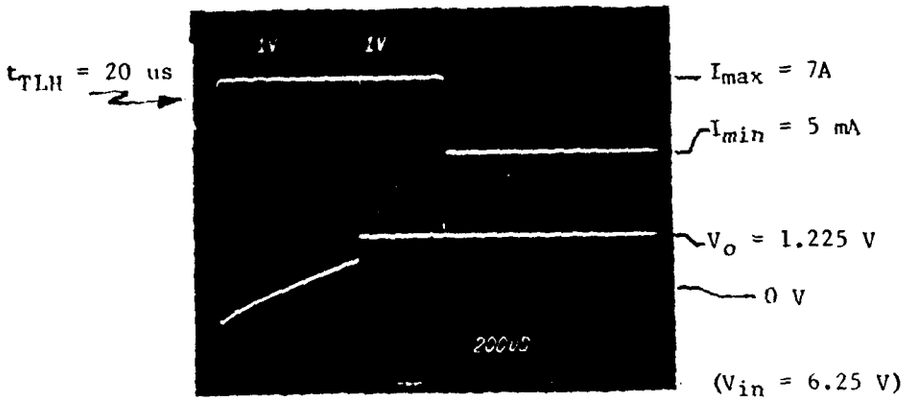


Device table

Device type	01	02	03	04
V_{IN}	20 V	20 V	36.5 V	36.5 V
R_L	887Ω	118Ω	250Ω	63.4Ω
C_i	0.33 μF	0.33 μF	1.0 μF	1.0 μF
C_L	0.1 μF	0.1 μF	1.0 μF	1.0 μF

NOTES:
1. Test is conducted without a heat sink.
2. The capacitors may be reduced or eliminated provided the device remains stable.
3. The control pin connection is required for device types 01 and 02 only.

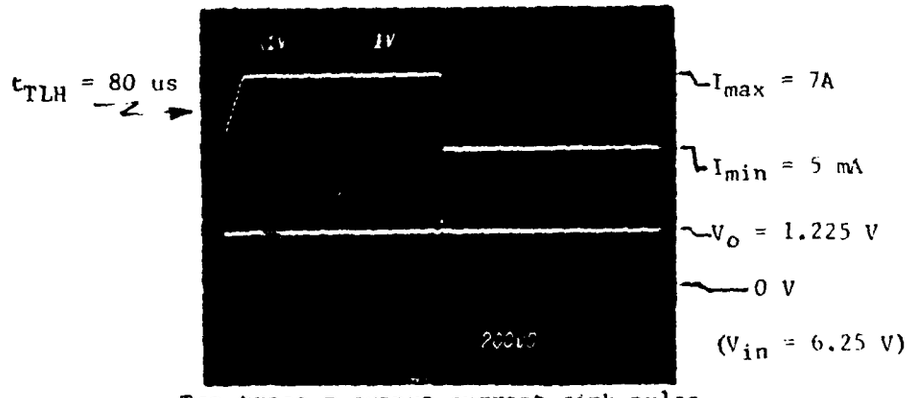
Figure 11-7. Burn-in and operating life test circuit.



Top trace = Output current sink pulse

Bottom trace = Voltage regulator output voltage

Figure 11-8. Output voltage versus load current.



Top trace = output current sink pulse

Bottom trace = voltage regulator output voltage

Figure 11-9. Output voltage versus load current.

Table 11-4. LM150K Data Distribution & Parameter Limits.

PARAMETER ($-55^{o}C \leq TA \leq 125^{o}C$)	* [///DATA////] * LL<-------LIMIT------->HL	UNIT
Output Voltage	* [///////] * 1.20 . . . . . 1.30	V
Output Voltage ($TA = 150^{o}C$)	* [//////] * 1.20 . . . . . 1.30	V
Line Regulation 1 ($TA = 25^{o}C$)	* [/] * -4 . 0 . 4	mV
Line Regulation 1	* [] * -20 . . . 0 . . . 20	mV
Load Regulation 1 ($TA = 25^{o}C$)	* [/] * -3.5 0 3.5	mV
Load Regulation 1	* [/] * -12. . 0 . .12	mV
Load Regulation 2 ($TA = 25^{o}C$)	* [] * -3.5 0 3.5	mV
Load Regulation 2	* [/] * -12. . 0 . .12	mV
Thermal Regulation ($TA = 25^{o}C$)	* [/] * -5 . 0 . 5	mV
Adjust Pin Current	* [////] * -100. . . . . -15	uA
Delta Adjust Pin Current (Line & Load)	* [] * -5. . 0 . .5	uA
Minimum Load Current 1 & 2	* [////]* -3 . . . . -.5	mA
Minimum Load Current 3	* [/////////] * -5 . . . . . -1	mA
Output Short Circuit Current 1 and peak output current	* [//] * -5.2. . . . -1.5	A
Output Short Circuit Current 2	*[/] * -2 . .-.15	A

Table 11-5.

POS. ADJ. VOLTAGE REGULATORS-LM150K; TEMPERATURE: 25 DEG C ; 23 APR 80

PARAMETER	CONDITION VIN	IL(MA)t(ms)	LO-LIMIT	S/N 34	S/N 35	S/N 36	S/N 37	S/N 38	HI-LIMIT	UNITS
VOUT1	4.25	-5	1.200	1.260	1.264	1.265	1.267	1.253	1.300	V
VOUT2	4.25	-3000	1.200	1.269	1.264	1.264	1.267	1.253	1.300	V
VOUT3	36.25	-5	1.200	1.261	1.256	1.266	1.268	1.254	1.300	V
VOUT4	36.25	-150	1.200	1.261	1.256	1.267	1.268	1.255	1.300	V
VRLINE	4.25 36.25	-5	-4.000M	1.178M	1.202M	1.737M	1.270M	1.444M	4.000M	V
VRLOAD1	6.25	-5 -3000	-3.500M	-456.1U	-584.0U	-1.018M	-227.0U	-247.0U	3.500M	V
VRLOAD2	36.25	-5 -150	-3.500M	429.0U	305.0U	311.0U	-152.0U	-654.0U	3.500M	V
VRTH	11.25	-1000 20.5	-5.000M	563.0U	1.398M	2.448M	1.772M	1.904M	5.000M	V
IADJ1 (LINE)	4.25	-5	-100.0U	-43.06U	-42.72U	-47.17U	-45.50U	-43.24U	-15.00U	A
IADJ2 (LINE)	36.25	-5	-100.0U	-43.27U	-42.81U	-47.30U	-45.52U	-43.20U	-15.00U	A
DIADJ1 (LINE)	4.25 36.25	-5	-5.000U	-218.6N	-89.42N	-134.1N	-14.90N	39.74N	5.000U	A
DIADJ2 (LOAD)	11.25	-5 -3000	-5.000U	-586.2N	-576.3N	-571.3N	-496.8N	-432.2N	5.000U	A
IOS1	4.25	VF=0V 0.1	-5.200	-3.880	-3.950	-4.050	-4.130	-4.050	-3.000	A
(VOUT) RECOV.			1.190	1.259	1.254	1.264	1.266	1.252	1.290	V
IOS2	36.00	VF=0V 10.0	-2.000	-460.0M	-494.0M	-418.0M	-461.0M	-464.0M	-150.0M	A
(VOUT) RECOV.			1.200	1.261	1.256	1.267	1.269	1.255	1.300	V
IPEAK	4.25	VF=1V 10.0	-5.200	-4.194	-4.274	-4.294	-4.434	-4.374	-3.000	A
(VOUT) RECOV.			1.200	1.260	1.255	1.265	1.267	1.254	1.300	V
IQ1	4.25	VF=1.4V	-3.000M	-918.5U	-952.2U	-40.32U*	-1.120M	-879.6U	-500.0U	A
IQ2	14.25	VF=1.4V	-3.000M	-1.284M	-1.326M	-1.273M	-1.556M	-1.349M	-500.0U	A
IQ3	36.25	VF=1.4V	-6.000M	-2.726M	-2.791M	-2.869M	-3.225M	-2.914M	-500.0U	A
VSTART	4.25	-3000	1.200	1.269	1.254	1.263	1.266	1.252	1.300	V

NOTE *1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 11-6. LM138K Data Distribution & Parameter Limits.

PARAMETER ($-55^{o}C \leq TA \leq 125^{o}C$)	* [///DATA////] * LL<-------LIMIT------->HL	UNIT
Output Voltage	* [////////////] * 1.19 . . . . . 1.29	V
Output Voltage ($TA = 150^{o}C$)	* [//////] * 1.19 . . . . . 1.29	V
Line Regulation 1 ($TA = 25^{o}C$)	* [/]* -4 . 0 . 4	mV
Line Regulation 1	* [/] * -17. . . 0 . . .17	mV
Load Regulation 1 ($TA = 25^{o}C$)	* [/] * -3.8 0 3.8	mV
Load Regulation 1	* [] * -8 . 0 . 8	mV
Load Regulation 2 ($TA = 25^{o}C$)	* [] * -3.8 0 3.8	mV
Load Regulation 2	* [] * -8 . 0 . 8	mV
Thermal Regulation ($TA = 25^{o}C$)	* [//] * -2 . 0 . 2	mV
Adjust Pin Current	* [//] * -100. . . . . -15	uA
Delta Adjust Pin Current (Line & Load)	* [] * -5. . 0 . .5	uA
Minimum Load Current 1 & 2	* [//]* -3 . . . . -.5	mA
Minimum Load Current 3	* [////] * -5 . . . . . -1	mA
Output Short Circuit Current 1 t = .1 ms	* [///] * -16 . . . . . -7	A
Output Short Circuit Current t = .5 ms	* [////]* -16 . . . . . -7	A

Table 11-6. LM138K Data Distribution & Parameter Limits (Cont'd)

PARAMETER ($-55^{o}C \leq TA \leq 125^{o}C$)	* [///DATA////] * LL<-------LIMIT------->HL	UNIT
Output Short Circuit Current 1 t = 5.0 ms	* [/////] * -15 . . . . . .-5	A
Output Short Circuit Current 2 t = 10.0 ms	* [//////] * -3 . . . . . -.2	A

Table 11-7.

POS. ADJ. VOLTAGE REGULATORS-LM138K; TEMPERATURE: 25 DEG C ; 23 APR 80

PARAMETER	CONDITION VIN	IL(MA)t(ms)		LO-LIMIT	S/N 34	S/N 35	S/N 36	S/N 37	S/N 38	HI-LIMIT	UNITS
VOUT1	4.25	-5		1.190	1.238	1.248	1.237	1.250	1.253	1.290	V
VOUT2	4.25	-5000		1.190	1.238	1.248	1.237	1.240	1.263	1.290	V
VOUT3	36.25	-5		1.190	1.234	1.243	1.240	1.251	1.255	1.290	V
VOUT4	36.25	-150		1.190	1.234	1.243	1.240	1.251	1.254	1.290	V
VOUT5	6.25	-7000	0.5	1.190	1.832	1.242	1.836	1.249	1.263	1.290	V
VRLINE	4.25 36.25	-5		-4.000M	1.579M	1.161M	2.222M	1.393M	1.785M	4.000M	V
VRLOAD1	6.25	-5 -5000		-3.800M	-525.0U	-152.0U	-860.9U	-79.99U	-187.0U	3.800M	V
VRLOAD2	36.25	-5 -150		-3.800M	-193.0U	-143.0U	-695.0U	-414.0U	-516.0U	3.800M	V
VRTH	11.25	-1000	20.5	-2.000M	-666.0U	-443.0U	-777.0U	-206.0U	63.06U	2.000M	V
IADJ1 (LINE)	4.25	-5		-100.0U	-44.06U	-43.57U	-38.75U	-44.21U	-45.70U	-15.00U	A
IADJ2 (LINE)	36.25	-5		-100.0U	-44.01U	-43.57U	-38.85U	-44.51U	-45.90U	-15.00U	A
DIADJ1 (LINE)	4.25 36.25	-5		-5.000U	49.67N	0.000	-99.35N	-298.1N	-198.7N	5.000U	A
DIADJ2 (LOAD)	11.25	-5 -5000		-5.000U	-149.0N	99.36N	99.35N	-99.35N	-198.7N	5.000U	A
IOS1	4.25	VF=0V	0.1	-16.00	-8.885	-8.362	-9.700	-8.662	-8.753	-7.000	A
			0.5	-16.00	-8.861	-8.350	-9.684	-8.726	-8.250	-7.000	A
			5.0	-15.00	-8.829	-8.334	-9.449	-8.618	-8.130	-5.000	A
(VOUT) RECOV.				1.190	1.234	1.244	1.239	1.250	1.257	1.290	V
IOS2	36.00	VF=0V	10.0	-3.000	-1.153	-1.114	-1.103	-1.059	-1.016	-200.0M	A
(VOUT) RECOV.				1.190	1.234	1.243	1.240	1.251	1.254	1.290	V
IQ1	4.25	VF=1.4V		-3.000M	-938.2U	-831.6U	-682.3U	-859.0U	-843.0U	-500.0U	A
IQ2	14.25	VF=1.4V		-3.000M	-1.285M	-1.183M	-1.135M	-1.186M	-1.232M	-500.0U	A
IQ3	36.25	VF=1.4V		-5.000M	-2.718M	-2.484M	-2.691M	-2.571M	-2.691M	-500.0U	A
VSTART	4.25	-5000		1.190	1.831	1.241	1.836	1.249	1.253	1.290	V

NOTE #1 VF-FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 11-8. Comparison of 3-Terminal Device Data (25°C). (Average measured data)

Parameter	Condition VIN (V)	Condition IL (mA)	[Generic Device Type] LM117H	LM117K	LM150K	LM138K	Units
VOUT1	4.25	5	+1.240	+1.246	+1.257	+1.241	V
VOUT2	4.25	IMAX	+1.233	+1.245	+1.257	+1.241	V
VOUT3	VIN MAX	5	+1.247	+1.251	+1.259	+1.243	V
VOUT4	VIN MAX	I1	+1.245	+1.248	+1.259	+1.241	V
VOUT5	6.25	7000	-	-	-	+1.241	
VRLINE	4.25	5	+5.771	+4.235	+1.223	+1.651	mV
	VIN MAX						
VRLOAD1	6.25	5	-5.237	-.050	-.449	-.357	mV
		IMAX					
VRLOAD2	VIN MAX	5	-1.663	-2.174	-.062	-.308	mV
		I1					
VRTH	V1	I2	+2.941	+3.142	+1.483	-.338	mV
IADJ1 (LINE)	4.25	5	-50.11	-55.761	-44.87	-44.00	uA
IADJ2 (LINE)	VIN MAX	5	-50.74	-56.127	-44.93	-44.19	uA
D-IADJ (LINE)	4.25	5	-.635	-.365	-.065	-.190	uA
	VIN MAX						
D-IADJ (LOAD)	6.25	5	-.682	-.155	-.532	-.012	uA
		IMAX					
IOS1	4.25	(t = .1 ms)	-1.240	-2.711	-3.953	-8.862	A
		(t = .5 ms)	-	-	-	-8.818	A
		(t = 5.0ms)	-	-	-	-8.748	A
VOUT RECOV			+1.236	+1.247	+1.256	+1.241	V
IOS2	V2	(t = 10 ms)	- .226	- .471	-.455	-1.156	A
VOUT RECOV			+1.249	+1.251	+1.259	+1.243	V
IPEAK	4.25	D-VOUT=-1.0V	-1.241	-2.409	-4.264	-	A
VOUT RECOV			+1.236	+1.247	+1.258	-	V
IQ1	4.25	VOUT =1.4V	-1.293	-1.318	-1.023	- .888	mA
IQ2	14.25	VOUT =1.4V	-1.443	-1.670	-1.416	-1.027	mA
IQ3	VIN MAX	VOUT =1.4V	-3.487	-3.729	-2.977	-2.728	mA
VSTART	4.25	IMAX	+1.234	+1.246	+1.256	+1.241	V
IMAX =			-500	-1500	-3000	-5000	mA
I1 =			- 50	- 200	-150	-150	mA
I2 =			-750	-1500	-1000	-1000	mA

Table 11-8. Comparison of 3-Terminal Device Data (25°C) (Cont'd)
(Average measured data)

Parameter	Condition VIN (V)	Condition IL (mA)	[Generic Device Type] LM117H	LM117K	LM150K	LM138K	Units
VIN MAX =			41.25	41.25	36.25	36.25	V
V1 =			14.60	14.60	11.25	11.25	V
V2 =			40.00	40.00	35.00	35.00	V

Table 11-9. Comparison of 3-Terminal Device Data (-55°C). (Average measured data)

Parameter	Condition VIN (V)	Condition IL (mA)	[Generic Device Type] LM117H	LM117K	LM150K	LM138K	Units
VOUT1	4.25	5	+1.240	+1.246	+1.250	+1.229	V
VOUT2	4.25	IMAX	+1.234	+1.245	+1.249	+1.228	V
VOUT3	VIN MAX	5	+1.245	+1.249	+1.251	+1.230	V
VOUT4	VIN MAX	I1	+1.244	+1.247	+1.251	+1.230	V
VOUT5	6.25	7000	-	-	-	+1.227	V
VRLINE	4.25 VIN MAX	5	+4.830	+3.192	+1.508	+1.907	mV
VRLOAD1	6.25	5 IMAX	+.328	+.842	+.477	-.334	mV
VRLOAD2	VIN MAX	5 I1	-.927	+.943	-.284	-.563	mV
VRTH	VIN MAX	I2	+4.083	+3.657	+.627	-.306	mV
	V1		-	-	-	-	mV
IDAJ1 (LINE)	4.25	5	-40.57	-46.51	-37.63	-35.90	uA
IADJ2 (LINE)	VIN MAX	5	-42.30	-46.76	-37.76	-36.06	uA
D-IADJ (LINE)	4.25 VIN MAX	5	-1.729	-.249	-.129	-.153	uA
D-IADJ (LOAD)	6.25	5 IMAX	-1.435	-.382	-1.354	-.017	uA
IOS1	4.25	(t = 1 ms)	-1.258	-2.751	-4.142	-8.626	A
		(t =.5 ms)	-	-	-	-8.641	A
		(t = 5 ms)	-	-	-	-8.844	A
VOUT RECOV		(t =10 ms)	+1.238	+1.246	1.250	1.226	V
IOS2	V2		-.329	-.698	- .689	-1.669	A
VOUT RECOV			+1.248	+1.249	1.252	1.231	V
IPEAK	4.25	D-VOUT=-1.0V	-1.262	-2.315	-4.350	-	A
VOUT RECOV			+1.237	+1.245	1.250	-	V
IQ1	4.25	VOUT =1.4V	-1.023	-1.052	-1.082	-.741	mA
IQ2	14.25	VOUT =1.4V	-1.380	-1.461	-1.742	-1.209	mA
IQ3	IN MAX	VOUT =1.4V	-3.377	-3.632	-3.653	-2.809	mA
VSTART	4.25	IMAX	+1.235	+1.245	-1.249	+1.229	V
IMAX =			-500	-1500	-3000	-7000	mA
I1 =			-50	-200	-150	-150	mA
I2 =			-125	-500	-1000	-1000	mA
VIN MAX=			41.25	41.25	36.25	36.25	V
V1 =			14.60	14.60	11.25	11.25	V
V2 =			40.00	40.00	35.00	35.00	V

Table 11-10. Comparison of 3-Terminal Device Data (125°C). (Average measured data)

Parameter	Condition VIN (V)	Condition I2 (mA)	[Generic Device Type LM117H	LM117K	LM150K	LM138K]	Units
VOUT1	4.25	5	+1.235	+1.238	+1.263	+1.250	V
VOUT2	4.25	IMAX	+1.225	+1.235	+1.268	+1.248	V
VOUT3	VIN MAX	5	+1.242	+1.243	+1.265	+1.251	V
VOUT4	VIN MAX	I1	+1.240	+1.239	+1.265	+1.251	V
VOUT5	6.25	7000	-	-	-	+1.245	
VRLINE	4.25 VIN MAX	5	+7.250	+5.077	+1.467	+1.990	mV
VRLOAD1	6.25	5 IMAX	-5.101	-1.269	-1.116	-.896	mV
VRLOAD2	VIN MAX	5 I1	-2.500	-3.519	+.043	-.297	mV
VRTH	V1	I2	+2.104	+2.702	+2.257	-.180	mV
IADJ (LINE)	4.25	5	-55.36	-60.63	-50.22	-48.57	uA
IADJ2 (LINE)	VIN MAX	5	-55.95	-61.03	-50.36	-48.76	uA
D-IADJ (LINE)	4.25	5	-.585	- .408	-.142	-.186	uA
D-IADJ (LOAD)	6.25	5 IMAX	-.235	+ .022	-.048	-.054	uA
IOS1	4.25	(t =.1 ms)	-1.187	-2.354	-3.678	-8.174	A
		(t =.5 ms)	-	-	-	-8.096	A
		(t = 5 ms)	-	-	-	-7.909	A
VOUT RECOV			+1.228	+1.237	+1.261	+1.245	V
IOS2	35.00	(t =10 ms)	- .235	- .431	- .389	-.848	A
VOUT RECOV			+1.244	+1.243	+1.265	+1.251	V
IPEAK	4.25	D-VOUT =-1V	-1.186	-1.990	-3.955	-	A
VOUT RECOV			+1.227	+1.236	+1.264	-	V
IQ1	4.25	VOUT = 1.4V	-1.450	-1.478	-.986	-.930	mA
IQ2	14.25	VOUT = 1.4V	-1.714	-1.771	-1.322	-1.208	mA
IQ3	41.25	VOUT = 1.4V	-3.396	-3.591	-2.561	-2.485	mA
VSTART	4.25	IMAX	+1.225	+1.236	+1.261	+1.248	V
IMAX =			-500	-1500	-3000	-5000	mA
I1 =			-50	- 200	-150	-150	mA
I2 =			-125	- 500	-1000	-1000	mA
VIN MAX =			41.25	41.25	36.25	36.25	V
V1 =			14.60	14.60	11.25	11.25	V
V2 =			40.00	40.00	35.00	35.00	V

Table 11-11. Electrical performance characteristics.
($-55^{o}C \leq TA \leq 125^{o}C$ unless otherwise stated)

Characteristic	Symbol	Test Conditions	Device Types	Limits Min	Limits Max	Units
Output voltage	VOUT	VIN=4.25V				
		IL=-5mA,-3.0A	05	1.20	1.30	V
		IL=-5mA,-5.0A	06	1.19	1.29	V
		VIN=36.25V				
		IL=-5mA,-150mA	05	1.20	1.30	V
		IL=-5mA,-150mA	06	1.19	1.29	V
		VIN=6.25V				
		IL=-7.0A	06	1.19	1.29	V
		IL=-5mA ; TA=150°C	05	1.20	1.30	V
		IL=-5mA ; TA=150°C	06	1.19	1.29	V
Line Regulation	VRLINE	$4.25 \leq VIN \leq 36.25V$				
		IL=-5mA ; TA=25°C	05,06	-4	4	mV
		IL=-5mA	05	-20	20	mV
		IL=-5mA	06	-17	17	mV
Load Regulation	VRLOAD	VIN=6.25V				
		$-3.0A \leq IL \leq -5mA$ TA=25°C	05	-3.5	3.5	mV
		$-5.0A \leq IL \leq -5mA$ TA=25°C	06	-3.5	3.5	mV
		$-3.0A \leq IL \leq -5mA$	05	-12	12	mV
		$-5.0A \leq IL \leq -5mA$	06	-12	12	mV
		VIN=36.25V				
		$-150mA \leq IL \leq -5mA$ TA=25°C	05	-3.5	3.5	mV
		$-150mA \leq IL \leq -5mA$ TA=25°C	06	-3.5	3.5	mV
		$-150mA \leq IL \leq -5mA$	05	-12	12	mV
		$-150mA \leq IL \leq -5mA$	06	-8	8	mV
Thermal Regulation	VRTH	VIN=11.25				
		IL=-1.0A ; TA=25°C	05	-5	5	mV
		IL=-1.0A ; TA=25°C	06	-2	2	mV
Adjust pin current	IADJ	VIN=4.25V				
		IL=-5mA	05,06	-100	-15	uA
		VIN=36.25V				
		IL=-5mA	05,06	-100	-15	uA

Table 11-11. Electrical performance characteriscs (Cont'd)
($-55^{o}C \leq TA \leq 125^{o}C$ unless otherwise stated)

Characteristic	Symbol	Test Conditions	Device Types	Limits Min	Limits Max	Units
Adjust pin current change versus line voltage	D-IADJ (LINE)	4.25 ≤VIN ≤36.25V IL=-5mA	05,06	-5	5	uA
Adjust pin current change versus load voltage	D-IADJ (LOAD)	VIN=6.25V -3.0A ≤IL ≤-5mA	05	-5	5	uA
		-5.0A ≤IL ≤-5mA	06	-5	5	uA
Minimum load current	IQ	4.25V ≤VIN ≤14.25V (forced VOUT=1.4V)	05,06	-3.0	-.5	mA
		VIN=36.25V (forced VOUT=1.4V)	05,06	-5.0	-.5	mA
Output short circuit current	IOS1	VIN=4.25V; t=10 ms	05	-5.2	-.5	A
	IOS2	VIN=35V ; t=10 ms	05	-2.0	-.15	A
	IOS1	VIN=4.25V; t=0.1ms	06	-16.0	-7.0	A
	IOS2	VIN=4.25V; t=0.5ms	06	-16.5	-7.0	A
	IOS3	VIN=4.25V; t=5.0ms	06	-15.0	-5.0	A
	IOS4	VIN=35V ; t=10 ms	06	-3.0	-.2	A
Output voltage recovery after output short circuit current	VOUT (RECOV)	VIN=4.25V (after IOS1) RL=0.416 ohms ; CL=20uF (after IOS3)	05	1.20	1.30	V
		RL=0.25 ohms ; CL=20uF	06	1.19	1.29	V
		VIN=35V RL=250 ohms (after IOS2	05	1.20	1.30	V
		RL=250 ohms (after IOS4	06	1.19	1.29	V
Voltage start-up	VSTART	VIN=4.25V RL=0.416 ohms ; CL=20uF	05	1.20	1.30	V
		RL=0.25 ohms ; CL=20uF	06	1.19	1.29	V
Ripple rejection	D-VIN /D-VOUT	VIN=6.25V Ei=1VRMS ; fo=2400 Hz IL=-500mA	05,06	65	-	dB
Output noise Voltage	NO	VIN=6.25V TA=25°C IL=-100mA	05,06	-	120	uV

Table 11-11. Electrical performance characteristics (Cont'd)
($-55^{o}C \leq TA \leq 125^{o}C$ unless otherwise stated)

Characteristic	Symbol	Test Conditions	Device Types	Limits Min	Limits Max	Units
Line transient response	D-VOUT /D-VIN	VIN=6.25V D-VIN=3.0V TA=25°C IL=-10mA	05,06	-	6	mV/V
Load transient response	D-VOUT /D-IL	VIN=6.25 TA=25°C IL=-100mA D-IL=-400mA	05,06	-	.3	mV/mA

SECTION XII

ADJUSTABLE NEGATIVE VOLTAGE REGULATORS

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SECTION XII

ADJUSTABLE NEGATIVE VOLTAGE REGULATORS

MIL-M-38510/118

(Highlights of and extension to Technical Report RADC-TR-80-49 Section III)

12.1 Introduction

Prior characterization efforts for RADC resulted in the development of slash sheet MIL-M-38510/115 for 3-terminal Fixed Negative Voltage Regulators. That slash sheet specifies regulators with -5 Volts, -12 Volts,-15 Volts and -24 Volts which complement the fixed positive voltage regulators specified in MIL-M-38510/107.

Adjustable voltage regulators are available in several case sizes and current outputs. Device types 79G and 79MG were considered for this characterization because of their similarity to the 79xx and 79Mxx families. Device type LM137H and LM137K were considered for this characterization because they compliment the LM117H and LM117K devices described in Section X and because of their user acceptance. All device types were selected by a joint decision of RADC, the JC-41 Committee and the Circuit Design Engineering activity of GEOS.

Table 12-1 lists the device types specified for this characterization.

Table 12-1. Device Types Specified.

Device Type	Generic Type	Manufacturer	Output Voltage Range	Output Current	Case Type	No. of Terminals
11801	79MG	Fairchild	$-30V \leq VO \leq -5V$	0.5A	TO-5	4
11802	79G	Fairchild	$-30V \leq VO \leq -5V$	1.0A	TO-5	4
11803	LM137H	NSC	$-37V \leq VO \leq -1.25V$	0.5A	TO-5	3
11804	LM137K	NSC	$-37V \leq VO \leq -1.25V$	1.5A	TO-3	3

12.2 Description of Device Types

The major physical distinctions between the various voltage regulators characterized for this slash sheet are the same as those described for the adjustable positive voltage regulators in Section X and are shown in Table 12-1. These features are: 1) voltage range, 2) maximum output current, 3) number of terminals and 4) case size.

All of these devices contain protective circuitry common to all IC voltage regulators characterized by GEOS on this contract. These circuits include a) output current limiting, b) short circuit protection, c) safe operating area protection and d) thermal shut down.

General block diagrams for the 4-terminal adjustable negative voltage regulator and the 3-terminal adjustable negative voltage regulator are shown in Figures 12-1 and 12-2, respectively.

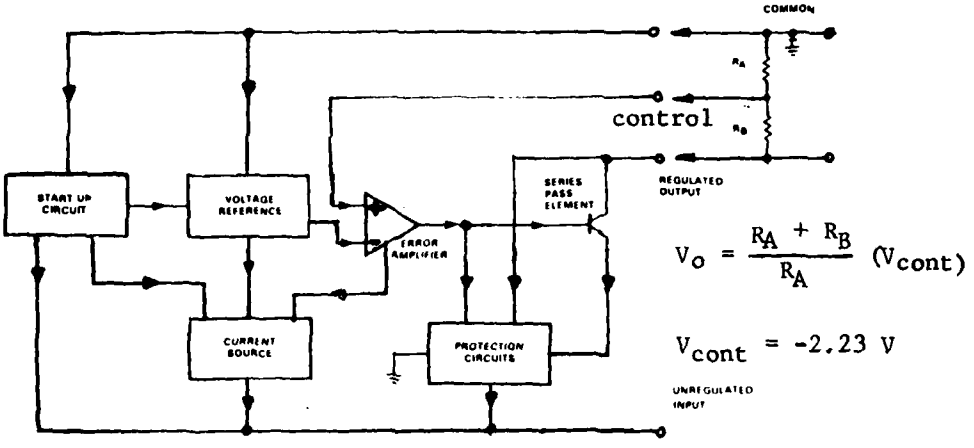


Figure 12-1. Block Diagram
of 4-Terminal Adjustable Negative Voltage Regulators.

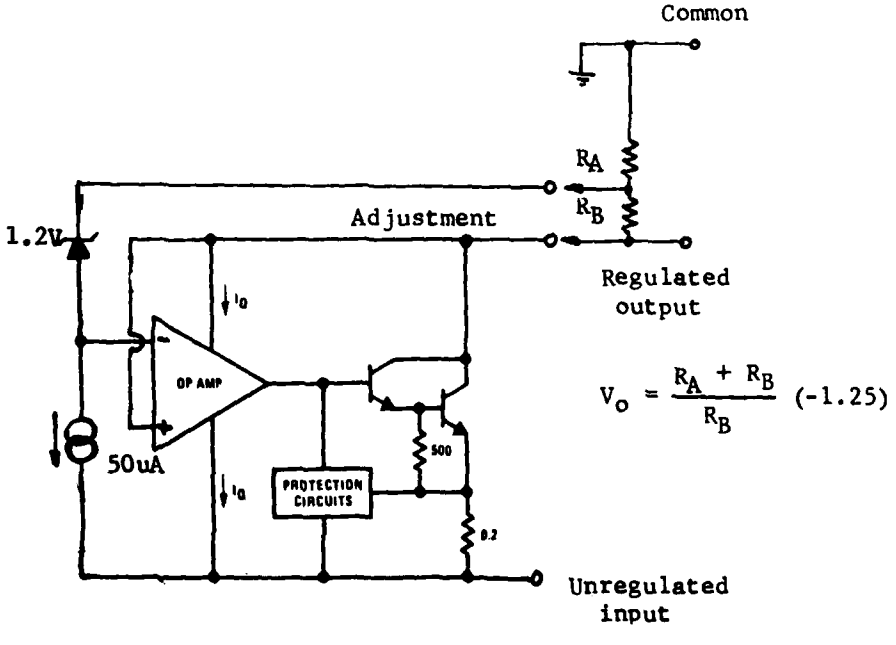


Figure 12-2. Block Diagram
of 3-Terminal Adjustable Negative Voltage Regulators.

The block diagrams of these devices are similar to their adjustable positive voltage regulator counterparts. Functionally, the positive and negative voltage regulators contain the same operating circuits. However, because the substrates for the negative regulators are referenced to the negative input supply, major changes to the circuitry are required to yield performance similar to that of the positive voltage regulators. Also, because the circuit reference (ie input supply voltage) is less stable than a reference ground, additional forward gain is required for the error amplifier to maintain a low line regulation specification. However, this results in a less stable device and additional input and output shunt capacitance is required to stabilize the negative regulators.

12.3 Test Development

Devices used in these characterizations were selected by a joint decision of RADC, the JC-41 Committee and the Circuit Design Engineering activity of GEOS. The devices were obtained from two manufacturers on the JC-41 Committee and from their distributors. Table 12-2 lists the device types characterized.

Table 12-2. Device Types Characterized.

Device Type	S/N	Manufacturer	Date Codes
11801	1-5	Fairchild	7906
11802	1-5	Fairchild	7639, 7916
11803	1-10	NSC	7902
11804	1-10	NSC	7836

Test Parameter Development

Test parameters for the adjustable positive voltage regulators and the adjustable negative voltage regulators were developed concurrently. A list of the electrical parameters tested during characterization is repeated from Section X, Table 10-3, and is presented in Table 12-3 Test Parameters for Characterization.

Table 12-3. Test Parameters for Characterization.

Test No	Symbol	Parameter
1	V_{OUT}	Output Voltage
2	V_{RLINE}	Line Regulation
3	V_{LOAD}	Load Regulation
4	V_{RTH}	Thermal Regulation
5	I_{ADJ}	Adjustment Pin Current
6	I_{ADJ} (Line)	Adjustment Pin Current Line Regulation
7	I_{ADJ} (Load)	Adjustment Pin Current Load Regulation
8	I_{OS}	Output Short Circuit Current
9	I_{peak}	Output Current with Forced Output Voltage of +1.0 Volts
10	V_{OUT} (RECOV)	Output Voltage Recovery After Output Short Circuit
11	V_{START}	Output Voltage Start-up with Maximum Load
12	I_Q	Quiescent Current
13	V_{IN}/V_{OUT}	Ripple Rejection
14	N_O	Output Noise
15	V_{OUT}/V_{IN}	Line Transient Response
16	V_{OUT}/I_L	Load Transient Response

Test Adapter Development

The test adapter used for these characterizations is the same as the test adapter used to characterize the adjustable positive voltage regulators. The schematic of the static test circuit is shown in Figure 12-3. The test adapter is shown in Section X, Figures 10-4 and 10-5. A complete description of this test adapter is presented in Section X, paragraph 10.3.

In order to acheive this versatility, the tester protection diodes and the transistors are mounted on DIP carriers, and the Darlington transistors are plugged into a transistor socket. The test adapter is readily changed to test negative voltage regulators by changing the DIP carrier with reverse mounted diodes and by changing the NPN transistors for PNP transistors. In addition, special load resistors are mounted on DIP carriers and each device type mounts into an interim adapter.

Dynamic tests for the voltage regulators include a) ripple rejection, b) line transient response, c) load transient response and d) output noise. No dynamic tests were run on the 79MG or 79G because of their similarity to the 79MXX and 79XX voltage regulator families which were characterized on a previous contract. Dynamic tests were performed on the LM137H and LM137K devices and the bench test circuit schematics are shown in Figures 12-4 thru 12-7. The noise test circuit schematic is shown in Figure 12-4. The test is performed using an oscilloscope with

a differential preamplifier with bandwidth control. The bandwidth is set to have a pass band from 10 Hz to 10 kHz and the peak-to-peak measurement of the noise was made. The ripple rejection test circuit schematic is shown in Figure 12-5. The test is performed using the above oscilloscope. The bandwidth is adjusted to reduce the high frequency noise without affecting the 2400 Hz ripple frequency. The 2400 Hz ripple at the regulator output is measured on the oscilloscope as a peak-to-peak voltage. Line transient response and load transient response test circuit schematics are shown in Figures 12-6 and 12-7. The peak measurements are made on an oscilloscope with a wide bandwidth pre-amp.

4 Test Results and Data

79MG and 79G Test Results

The 79G Adjustable Negative Voltage Regulators originally failed the output voltage tests at 125°C with maximum load current. Bench testing of these units revealed that the device shut down with steady state case temperatures above 60°C and with pulsed 1.0 amp load currents applied to the regulator. The date code for these devices was 7639. The vendor was contacted concerning this problem. Additional units were supplied with date code 7916 for characterization. These units were tested on both the S3260/70 and the bench and no anomalies were observed. The units met all of the tested electrical specifications in the slash sheet. The measurement data is, typically, in the middle of the specified tolerance band and the band spread appears to be reasonable for several parameters. However, the bandspread for some parameters - notably load and line regulation - is much greater than is necessary for even 100% yield. The 79MG Adjustable Negative Voltage Regulators met all of the tested electrical specifications in the slash sheet. No anomalies were detected during the test of these devices. Typical data sheets for these two devices are presented in Tables 12-4 and 12-5.

137H and LM137K Test Results

Typical data sheets for the LM137H and LM137K devices are shown in Tables 12-6 and 12-7. All of the LM137K devices met the specifications on the slash sheet. All of the LM137H devices failed the originally defined load regulation requirement for Vin = 6.25 volts at 25°C. Discussions with the vendor resulted in a change to the specification a) to test with a reduced load range, (5 mA $\leq$ IL $\leq$ 200 mA) and maintain the same limit ($\pm$ 6 mV) and b) to test to the same limit (5 mA $\leq$ IL $\leq$ 500 mA) and relax the limit ($\pm$ 12 mA).

Tabulation of dynamic test data taken in a bench test set up for the LM137H Adjustable Negative Voltage Regulators is shown in Table 12-8. The tests were performed at 25°C. All of the bench measurements made on these devices were stable and data showed reasonably safe margins for the recommended tolerances. Oscillographs of the line and load

transient responses are shown in Figures 12-9 and 12-10. Dynamic test data and oscillographs were also obtained for the LM137K Adjustable Negative Voltage Regulators. Oscillographs for line and load regulation for these devices are presented in Figures 12-11 and 12-12.

12.5 Discussion of Results

All of the test data taken on the 79MG voltage regulators was within the tolerances recommended by the manufacturer and the JC-41 Committee. The most serious problem detected with the 79G voltage regulator was a failure of the output voltage for 1.0 amp load currents as the case temperature is increased beyond 60°C. This problem was discussed with the vendor. The original parts received from a distributor had date code 7639 and were not typical of the devices currently being manufactured. Since this problem presented observations similar to those observed during the characterization of the 79xx Fixed Negative Voltage Regulators, some of the 7905 Fixed Voltage Regulators were retested in the same test circuit. The same failure mode was observed for the 7905 and the 79G Negative Voltage Regulators. Since only the devices manufactured with the most recent date codes are to be certified in accordance with the slash sheet, certified parts will not exhibit the problems observed with the older devices.

As with the adjustable positive voltage regulators, line and load regulation test parameter tolerances were excessively conservative in light of the measured data. Again, GEOS was unsuccessful in negotiating tighter test limits for these parameters.

Testing of the LM137H and LM137K voltage regulators was performed on the same test adapter used for the 79MG and 79G voltage. Except for the load regulation test described in 12.4, all devices met the original parameter tolerances specified by the manufacturer and approved by the JC-41 Committee. The device failure was shown to be an actual device anomaly. The anomaly was not detrimental to device performance; so, modifications to the specification were considered appropriate.

12.6 Slash Sheet Development

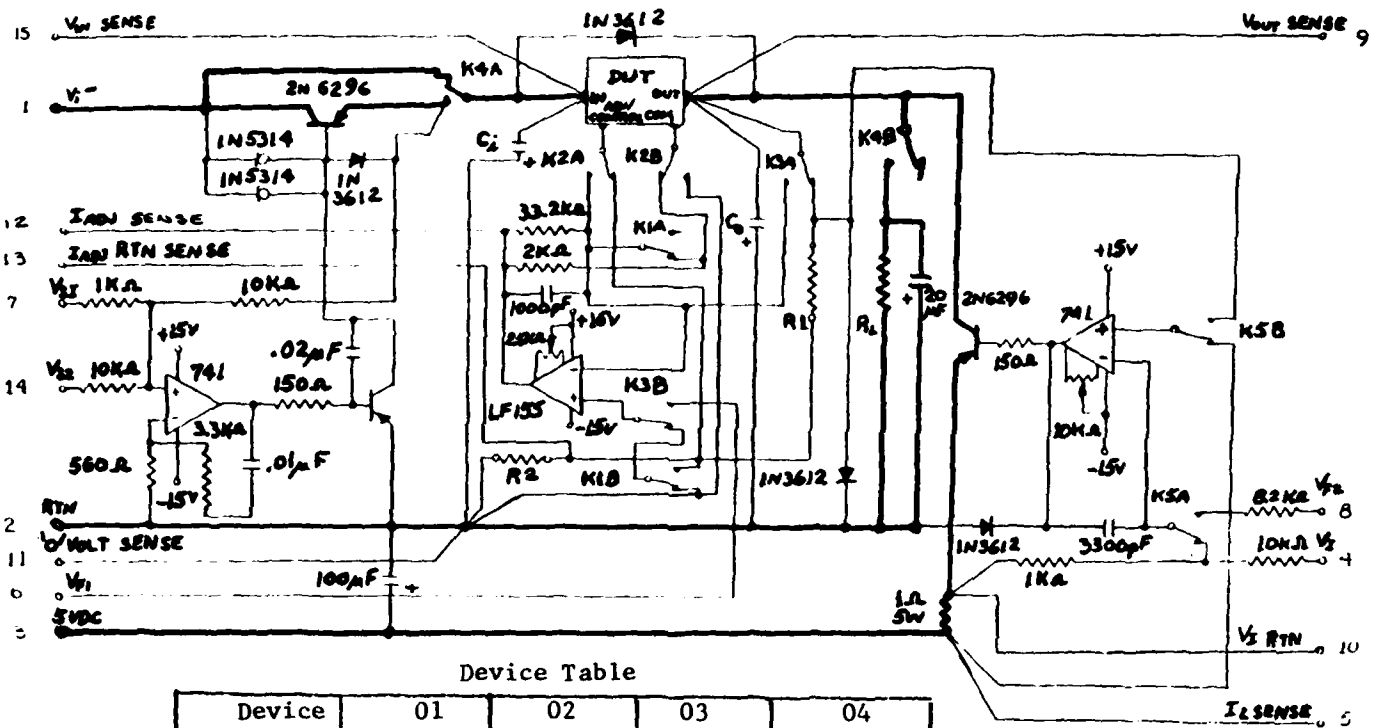
A modified Table I was received from each of two manufacturer committee members supplying parts for the characterization. The parameters were modified to include a) a voltage recovery measurement after the output short circuit current, b) a start-up test with an R-C load and c) additional and modified load regulation tests for the LM137H. In general, the parameters and test circuits are the same as those required in MIL-M-38510/115 to test fixed negative voltage regulators.

12.7 Conclusions and Recommendations

The test circuits used in these characterizations were developed for use either by an automatic tester or in a bench type set-up. Measurements

were taken in both test set-ups and excellent tester correlation was observed. The test circuits were easily constructed; however, because of the high currents involved at the input and output of the DUT, a difference of several millivolts can be observed across a connector terminal. Extreme care must be made to connect the voltmeter sense leads to the proper points in the test circuit.

When the above procedures were properly observed, all of the devices performed well in their individual test circuits. The regulation tests have very conservative tolerances and could be easily reduced from their present $\pm$ 150 mV limits. These limits could be reduced to $\pm$ 50 mV.



Device Table

Device Type	01 79MG	02 79G	03 LM137H	04 LM137K
R_1	2.74KΩ	2.74KΩ	249Ω	249Ω
R_2	2.21KΩ	2.21KΩ	0	0
R_L	10Ω	5Ω	2.5Ω	.833Ω
C_i	2.0uF	2.0uF	1.0uF	1.0uF
C_o	2.0uF	2.0uF	1.0uF	1.0uF

Figure 12-3. Negative voltage regulator test circuit for static tests.

Notes:

1. Heavy current paths ($I \geq 1.0A$) are indicated by bold lines.

2. Kelvin connections must be used for all output current and voltage measurements.

3. Op amp stabilization networks may vary with test adapter construction. Alternate drive circuits for the power transistor may be used to develop the proper load current and input voltage pulses.

4. Relay switch positions are defined in the appropriate Table III of the slash sheet.

5. Load currents of 5 mA are established via the load resistors R_1 and R_2. All other load currents shall be established via the pulse load circuit.

6. The pulse generator for the pulse load circuit shall have the following characteristics.

   a. Pulse amplitude = $-10(I_L - V_o/(R_1 + R_2))$ volts

   b. Pulse width = 1.0mS (unless otherwise stated)

   c. Duty cycle = 2% (maximum)

7. Load circuits shall be determined by the voltage measured across the 1 ohm resistor. Measurements shall be made 0.5 ms after the start of the pulse.

8. V_{in} (LOW) and V_{in} (HIGH) per the appropriate Table III of the slash sheet.

9. $V_{RLINE} + V_B - V_A$.

10. The output voltage is samples at specified intervals. Stobe pulse width is 100 us maximum.

11. I_L (minimum) and I_L (maximum) per the appropriate Table III of the slash sheet.

12. $V_{RLOAD} = V_D - V_C$.

13. $V_{RTH} = V_D - V_E$.

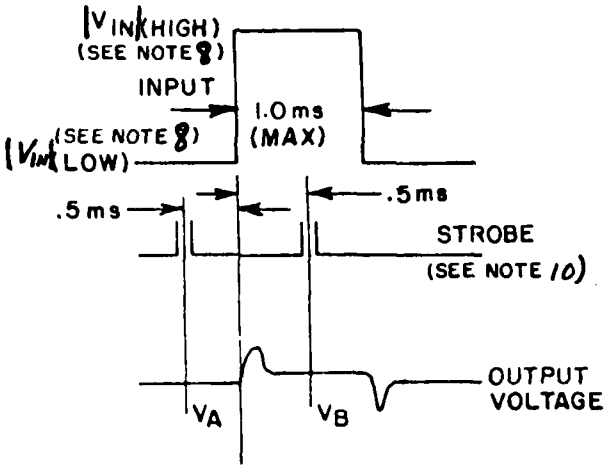
14. Force voltage, $V_I = -15$ volts; Relay K4 is energized.

15. $I_{OS} = (I_L)$ Amps.

16. $I_{pk} = (I_L + V_o/R_L + V_o/(R_1 + R_2)$ Amps.

17. For device types 01 & 02, t = 10.5 msec.
For device types 03 & 04, t + 20.5 msec.

LINE REGULATION WAVEFORMS



LOAD REGULATION WAVEFORMS

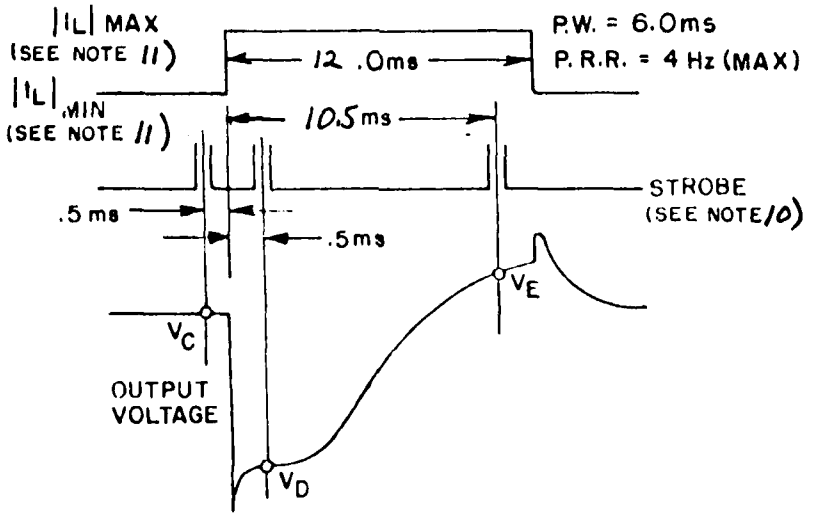
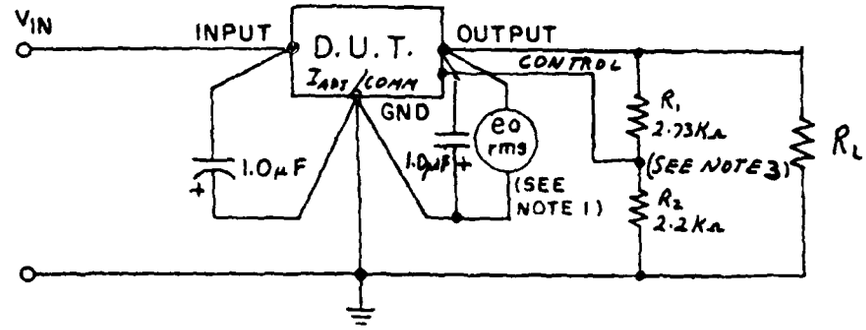


Figure 12-3. Negative voltage regulator test circuit for static tests (cont'd).



Device Table

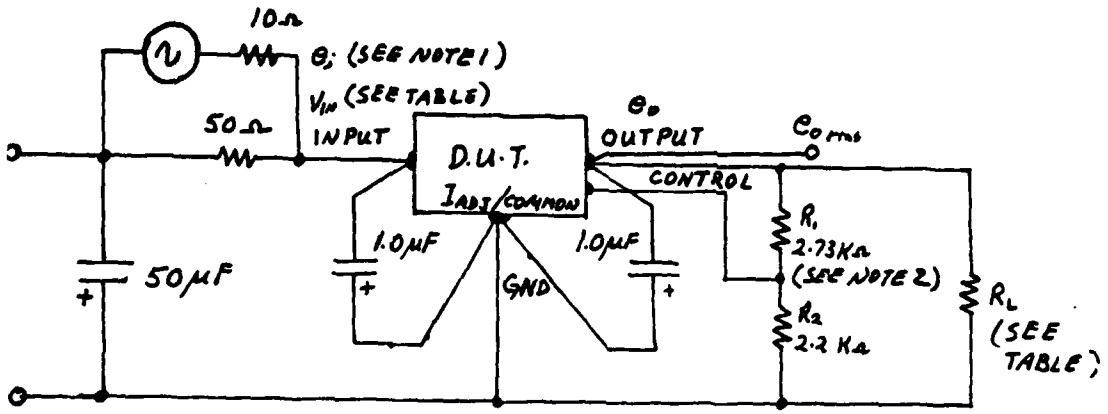
Device Type	01 79 MG	02 79 G	03 LM137H	04 LM137G
V_{IN}	-10 V	-10 V	-6.25V	-6.25 V
R_L	100Ω	50Ω	25Ω	12.5Ω

R_L shall be type RER 70 or equivalent.

Notes:

1. The meter for measuring e_{orms} shall have a minimum bandwidth from 10 Hz to 10 kHz and shall measure true rms voltages.
2. $N_o = e_o$ rms.
3. The control pin connections and resistors (R_1 and R_2) are required for device types 01 and 02 only.

Figure 12-4. Noise test circuit for negative voltage regulators.



Device Table

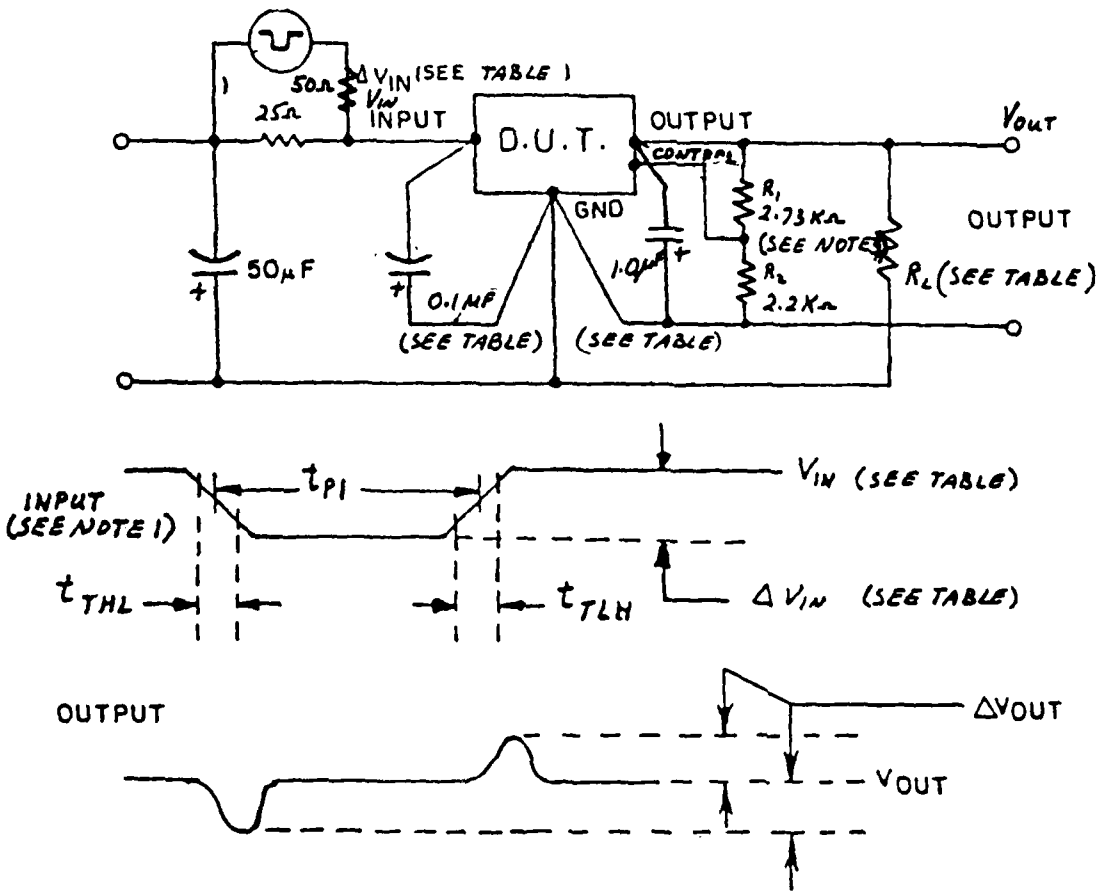
Device Type	01 79 MG	02 79 G	03 LM137H	04 LM137K
V_{IN}	-10 V	-10 V	-6.25 V	-6.25 V
R_L	40.2Ω	14.3Ω	10Ω	2.5Ω

The input 50Ω resistor and R_L shall be type RER 70 or equivalent.

Notes:

1. e_i = 1 V_{rms} @ f = 2400 Hz (measured at the input terminals of the DUT)
   ripple rejection = 20 log $\frac{e_{irms}}{e_{orms}}$
2. The control pin connection and resistors (R_1 and R_2) are required for device types 01 and 02 only.

Figure 12-5. Ripple rejection test circuit for negative voltage regulators.



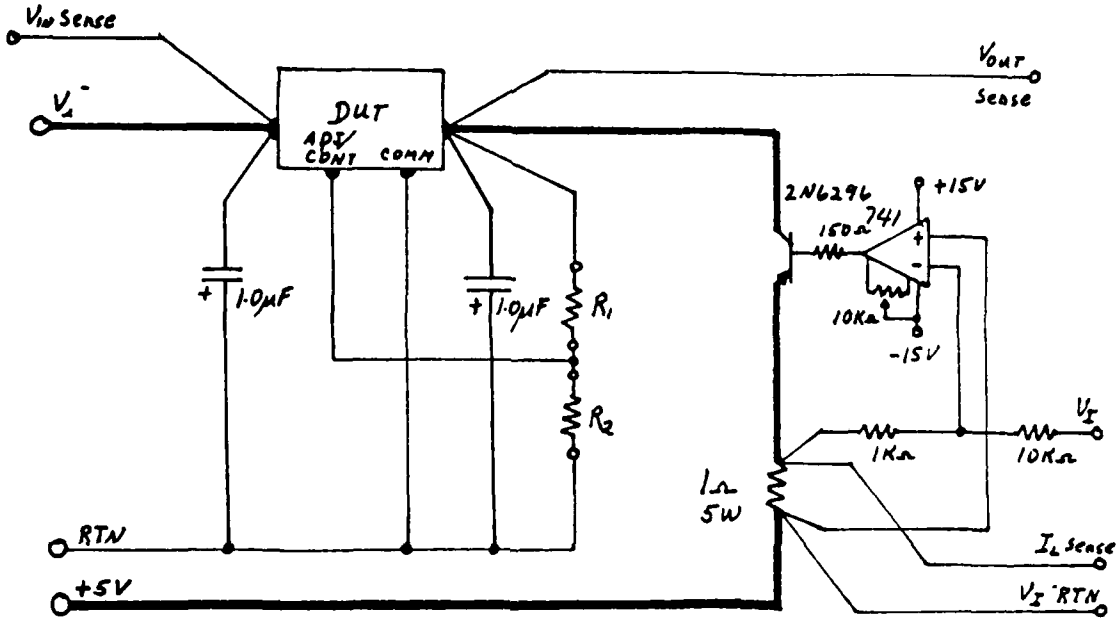
Device Table

Device Type	01 79MG	02 79G	03 LM137H	04 LM137K	NOTES
V_{IN}	-10V	-10V	-6.25V	-6.25V	1
V_{IN}	- 3V	- 3V	- 1V	- 1V	1
R_L	1.25KΩ	1.25KΩ	120Ω	120Ω	
$t_{THL}=t_{TLH}$	5.0us	5.0us	5.0us	5.0us	1

Notes:

1. Measured at device input.
2. Pulse width t_{p1} = 25 us; duty cycle = 3 % (maximum)
3. Oscilloscope bandwidth = 5 MHz to 15 MHz.
4. The control pin connection and resistors (R_1 and R_2) are required for device types 01 and 02.

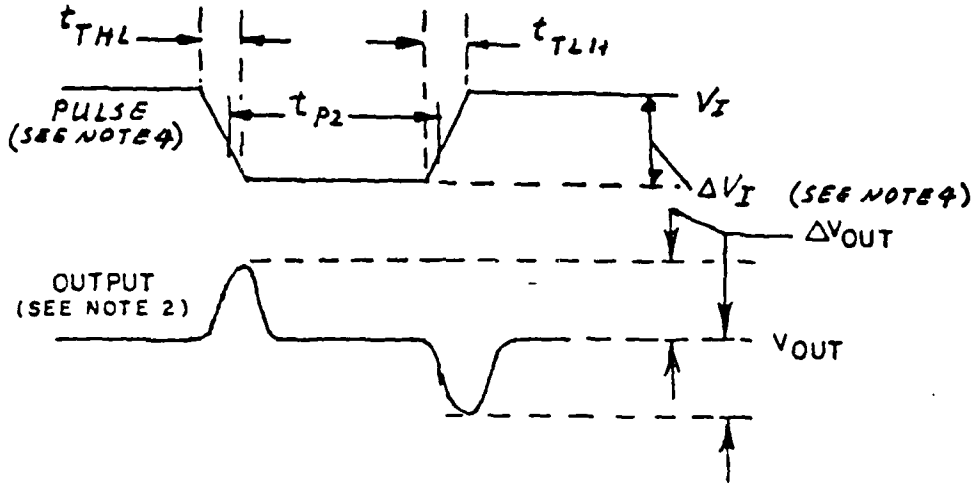
Figure 12-6. Line transient response test circuit for negative voltage regulators.



Device Table

Device Type	01 79MG	02 79G	03 LM137H	04 LM137K
R1	2.21KΩ	2.21KΩ	249Ω	249Ω
R2	2.74KΩ	2.74KΩ	0	0
I_L	50mA	100mA	50mA	100mA
I_L	200mA	400mA	200mA	400mA
V_I	0.49V	0.99V	0.45V	0.95V
V_I	2.0V	4.0V	2.0V	4.0V

Figure 12-7. Load transient response test circuit for negative voltage regulators.



Notes:

1. Heavy current path ($I \geq 1.0A$) are indicated by bold lines.

2. Kelvin connections must be used for all output current and voltage measurements.

3. Op amp stabilization networks may vary with test adapter construction. Alternate drive circuits for the 2N6296 may be used to develop the proper load current and input voltage pulses.

4. The pulse generator for the pulse load circuit shall have the following characteristics. (see device table)

   a. Voltage level (V_I) = 10 (I_L - Vo/(R_1 + R_2) volts
   b. Pulse width (t_{p2}) = 25 u sec
   c. Duty cycle = 3% (maximum)
   d. $t_{THL} = t_{TLH}$ = 1.0 u sec for device types 01 and 02
   e. $t_{THL} = t_{TLH}$ = 5.0 u sec for device types 03 and 04
   f. Difference voltage level ($\triangle V_I$) = 10 (I_L) volts

5. a. $\triangle V_{out}$ = 500 mV maximum for device type 01
   b. $\triangle V_{out}$ = 1000 mV maximum for device type 02
   c. $\triangle V_{out}$ = 60 mV maximum for devices type 03 and 04
   (These values guarantee the specified limits for load transient response.)

6. Oscilloscope minimum bandwidth shall be 9 MHz to 15 MHz.

Figure 12-7. Load transient response test circuit for negative voltage regulators (cont'd).

LM137H Line Transient Response

V/cm = .020 Unit #1
Time/cm = 5 us

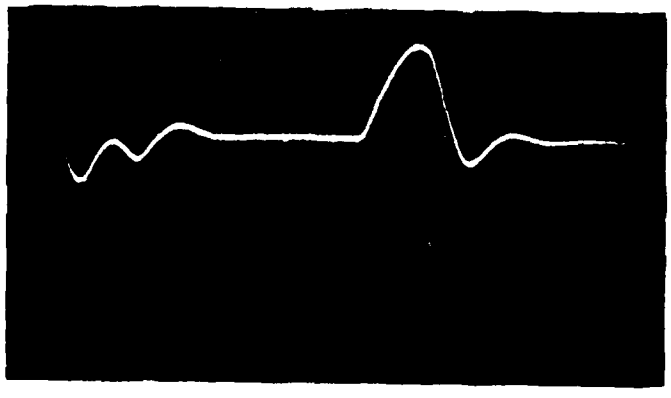


Figure 12-8 Oscillograph of LM137H Line Transient Response Test

LM137H Load Transient Response

V/cm = .01
Time/cm = 5 us

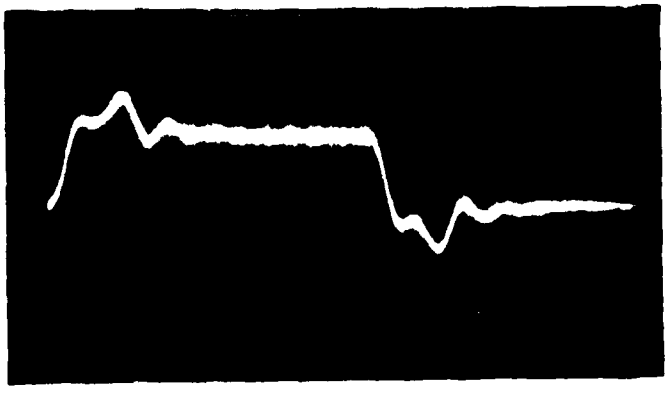


Figure 12-9 Oscillograph of LM137H Load Transient Response Test

Table 12-4.

NEG. ADJ. VOLTAGE REGULATORS-79MG ; TEMPERATURE: 25 DEG C ; 27 NOV 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI-LIMIT	UNITS
VOUT1	-8.00	5	-5.250	-5.037	-5.015	-5.028	-5.017	-5.013	-4.750	V
VOUT2	-10.00	500	-5.250	-5.040	-5.017	-5.030	-5.019	-5.015	-4.750	V
VOUT3	-20.00	5	-5.250	-5.046	-5.024	-5.037	-5.025	-5.021	-4.750	V
VOUT4	-20.00	500	-5.250	-5.047	-5.025	-5.038	-5.026	-5.022	-4.750	V
VOUT5	-30.00	5	-5.250	-5.051	-5.030	-5.042	-5.031	-5.026	-4.750	V
VOUT6	-30.00	500	-5.250	-5.051	-5.030	-5.060	-5.031	-5.026	-4.750	V
VRLINE1	-8.00 to -30.00	50	-150.0M	-8.250M	-7.780M	-10.15M	-9.190M	-8.480M	150.0M	V
VRLINE2	-8.00 to -20.00	350	-50.00M	-7.470M	-7.040M	-8.930M	-8.090M	-7.540M	50.00M	V
VRLOAD1	-10.00	5 to 500	-100.0M	60.08U	-280.4U	-350.0U	150.2U	-40.05U	100.0M	V
VRLOAD2	-30.00	5 to 500	-150.0M	-190.3U	-200.3U	-70.10U	-199.8U	-190.3U	150.0M	V
VRTH (IL APPLIED FOR 10.5msec.)	-15.00	500	-50.00M	26.89M	0.000	26.89M	0.000	26.89M	50.00M	V
ISCD1 (LINE)	-10.00	5	100.0U	566.6U	588.5U	593.8U	594.6U	564.3U	3.000M	A
ISCD2 (LINE)	-30.00	5	100.0U	969.6U	1.004M	1.014M	1.010M	957.1U	4.000M	A
DISCD1 (LINE)	-8.00 to -30.00	5	-1.000M	-406.2U	-419.3U	-426.8U	-427.2U	-402.4U	1.000M	A
DISCD2 (LOAD)	-10.00	5 to 500	-500.0U	74.51N	-288.1N	-347.7N	4.948N	0.000	500.0U	A
ICTL	-10.00	350	10.00N	147.8N	136.7N	186.8N	57.52N	171.6N	8.000U	A
IOS1 (VOUT)	-8.00 RECOV.	UF-0V	2.000M -5.250	740.0M -5.135	770.0M -5.108	685.0M -5.135	795.0M -5.108	740.0M -5.108	2.000 -4.750	A V
IOS2 (VOUT)	-10.00 RECOV.	UF-0V	2.000M -5.250	730.0M -5.135	740.0M -5.108	695.0M -5.135	760.0M -5.108	710.0M -5.108	2.000 -4.750	A V
IOS3 (VOUT)	-20.00 RECOV.	UF-0V	1.500M -5.250	397.5M -5.135	399.0M -5.135	370.5M -5.162	421.5M -5.135	385.0M -5.135	1.500 -4.750	A V
IOS4 (VOUT)	-30.00 RECOV.	UF-0V	1.000M -5.250	268.5M -5.162	264.5M -5.135	196.5M -5.162	282.5M -5.135	266.5M -5.135	1.000 -4.750	A V
IPEAK (VOUT)	-8.00 RECOV.	UF-VOUT-.48	500.0M -5.250	760.0M -5.135	790.0M -5.108	705.0M -5.135	815.0M -5.108	760.0M -5.108	8.000 -4.750	A V
VSTART	-20.00	500	-5.250	-5.135	-5.108	-5.108	-5.108	-5.081	-4.750	V

NOTE #1 UF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 12-5.

NEG. ADJ. VOLTAGE REGULATORS-79Q ; TEMPERATURE: 25 DEG C ; 27 NOV 79

PARAMETER	CONDITION VIN	CONDITION IL(mA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	HI-LIMIT	UNITS
VOUT1	-8.00	5	-5.250	-4.980	-4.968	-4.976	-4.947	-4.750	V
VOUT2	-8.00	1000	-5.250	-4.981	-4.965	-4.981	-4.948	-4.750	V
VOUT3	-20.00	5	-5.250	-4.987	-4.971	-4.989	-4.963	-4.750	V
VOUT4	-20.00	1000	-5.250	-4.987	-4.978	-4.991	-4.964	-4.750	V
VOUT5	-30.00	5	-5.250	-4.980	-4.976	-4.986	-4.957	-4.750	V
VOUT6	-30.00	100	-5.250	-5.000	-4.977	-4.988	-4.958	-4.750	V
VRLINE1	-8.00	100	-150.0M	-8.610M	-8.190M	-10.33M	-7.980M	150.0M	V
	-30.00								
VRLINE2	-8.00	500	-75.00M	-7.230M	-6.860M	-8.740M	-6.790M	75.00M	V
	-85.00								
VRLOAD1	-10.00	5	-100.0M	-50.07U	-70.10U	50.07U	-330.0U	100.0M	V
		1000							
VRLOAD2	-30.00	5	-150.0M	-110.1U	-100.1U	-209.8U	90.12U	150.0M	V
		100							
VRTH	-15.00	1000	-50.00M	26.89M	26.89M	26.89M	26.89M	50.00M	V
(IL APPLIED FOR 10.5msec.)									
ISCD1 (LINE)	-10.00	5	500.0U	615.1U	523.1U	615.6U	586.5U	3.000M	A
ISCD2 (LINE)	-30.00	5	500.0U	598.0U	508.2U	593.6U	570.8U	4.000M	A
DISCD1 (LINE)	-8.00	5	-1.000M	13.29U	7.755U	13.97U	11.28U	1.000M	A
	-30.00								
DISCD2 (LOAD)	-10.00	5	-500.0U	248.4N	-168.9N	34.81N	-327.8N	500.0U	A
		1000							
ICTL	-10.00	500	10.00N	412.8N	167.9N	381.3N	315.1N	2.000U	A
IOS1	-8.00	VF=0V	2.000M	2.475	2.210	2.240	2.375	4.500	A
(VOUT) RECOV.			-5.250	-5.081	-5.055	-5.081	-5.028	-4.750	V
IOS2	-10.00	VF=0V	2.000M	2.345	2.135	2.160	2.270	4.500	A
(VOUT) RECOV.			-5.250	-5.081	-5.055	-5.055	-5.028	-4.750	V
IOS3	-25.00	VF=0V	2.000M	1.165	1.070	1.155	1.195	3.500	A
(VOUT) RECOV.			-5.250	-5.081	-5.081	-5.108	-5.055	-4.750	V
IOS4	-30.00	VF=0V	2.000M	825.0M	765.0M	860.0M	870.0M	2.000	A
(VOUT) RECOV.			-5.250	-5.081	-5.081	-5.108	-5.055	-4.750	V
IPEAK	-8.00	VF=VOUT-.4V	4.000	4.496	4.234	4.260	4.306	4.500	A
(VOUT) RECOV.			-5.250	-5.081	-5.055	-5.081	-5.028	-4.750	V
VSTART	-80.00	1000	-5.250	-5.055	-5.055	-5.055	-5.028	-4.750	V

NOTE :1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table. 12-6.

NEG. ADJ. VOLTAGE REGULATORS-LM137H; TEMPERATURE: 25 DEG C ; 01 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI-LIMIT	UNITS
VOUT1	-4.25	5	-1.275	-1.252	-1.253	-1.252	-1.244	-1.249	-1.225	V
VOUT2	-4.25	500	-1.275	-1.240	-1.242	-1.242	-1.233	-1.238	-1.225	V
VOUT3	-41.25	5	-1.275	-1.255	-1.256	-1.255	-1.247	-1.252	-1.225	V
VOUT4	-41.25	50	-1.275	-1.255	-1.253	-1.254	-1.247	-1.250	-1.225	V
VRLINE	-4.25 -41.25	5	-9.000M	-2.715M	-2.262M	-2.262M	-2.375M	-2.375M	9.000M	V
VRLOAD1	-6.25	5 500	-6.000M	12.33MΩ	10.63MΩ	10.18MΩ	12.78MΩ	11.65MΩ	6.000M	V
VRLOAD2	-41.25	5 50	-6.000M	1.244M	1.018M	1.131M	1.018M	904.9U	6.000M	V
VRTH (IL APPLIED FOR 10.5Msec.)	-14.60	750	-5.000M	452.5U	339.3U	565.5U	339.3U	678.5U	5.000M	V
IADJ1 (LINE)	-4.25	5	25.00U	71.94U	64.68U	64.72U	74.77U	70.91U	100.0U	A
IADJ2 (LINE)	-41.25	5	25.00U	75.33U	67.38U	67.43U	78.07U	74.28U	100.0U	A
DIADJ1 (LINE)	-4.25 -41.25	5	-5.000U	3.396U	2.697U	2.709U	3.301U	3.369U	5.000U	A
DIADJ2 (LOAD)	-6.25	5 500	-5.000U	-1.256U	-937.0N	-1.017U	-1.153U	-1.103U	5.000U	A
IOS1	-4.25	VF=0V	500.0M	1.150	1.235	1.235	1.215	1.185	1.800	A
(VOUT) RECOV.			-1.275	-1.240	-1.242	-1.243	-1.232	-1.237	-1.225	V
IOS2	-40.00	VF=0V	50.00M	250.0M	365.0M	365.0M	310.0M	325.0M	500.0M	A
(VOUT) RECOV.			-1.275	-1.254	-1.254	-1.255	-1.247	-1.250	-1.225	V
IPEAK	-4.25	VF=-1.0V	500.0M	1.155	1.240	1.240	1.220	1.190	1.800	A
(VOUT) RECOV.			-1.275	-1.241	-1.243	-1.243	-1.232	-1.238	-1.225	V
IQ1	-4.25	VF=-1.4V	200.0U	400.0U	400.0U	400.0U	448.0U	432.0U	3.000M	A
IQ2	-14.25	VF=-1.4V	200.0U	480.0U	448.0U	464.0U	510.0U	508.0U	3.000M	A
IQ3	-41.25	VF=-1.4V	1.000M	1.980M	1.800M	1.800M	2.090M	2.020M	5.000M	A
VSTART	-4.25	500	-1.275	-1.241	-1.242	-1.243	-1.233	-1.238	-1.200	V

NOTE :1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 12.7.

NEG. ADJ. VOLTAGE REGULATORS-LM137K; TEMPERATURE: 25 DEG C ; 30 APR 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 4	S/N 5	S/N 6	HI-LIMIT	UNITS
VOUT1	-4.25	5	-1.275	-1.254	-1.259	-1.267	-1.257	-1.256	-1.225	V
VOUT2	-4.25	1500	-1.275	-1.249	-1.254	-1.261	-1.252	-1.252	-1.225	V
VOUT3	-41.25	5	-1.275	-1.257	-1.261	-1.268	-1.259	-1.258	-1.225	V
VOUT4	-41.25	250	-1.275	-1.256	-1.260	-1.268	-1.258	-1.258	-1.225	V
VRLINE	-4.25 -41.25	5	-9.000M	-3.506M	-2.149M	-1.923M	-2.149M	-2.715M	9.000M	V
VRLOAD1	-6.25	5 1500	-6.000M	4.524M	4.864M	4.977M	5.090M	4.185M	6.000M	V
VRLOAD2	-41.25	5 250	-6.000M	1.018M	339.4U	791.8U	1.131M	452.4U	6.000M	V
VRTH (IL APPLIED FOR 10.5Msec.)	-14.60	1500	-5.000M	565.5U	1.131M	1.018M	1.470M	791.7U	5.000M	V
IADJ1 (LINE)	-4.25	5	25.00U	73.08U	67.70U	64.52U	62.90U	60.14U	100.0U	A
IADJ2 (LINE)	-41.25	5	25.00U	76.62U	70.51U	67.09U	65.47U	63.50U	100.0U	A
DIADJ1 (LINE)	-4.25 -41.25	5	-5.000U	3.541U	2.814U	2.572U	2.570U	3.358U	5.000U	A
DIADJ2 (LOAD)	-6.25	5 1500	-5.000U	-669.5N	-508.0N	-272.0N	-538.5N	-510.0N	5.000U	A
IOS1	-4.25	VF=0V	1.500	2.190	2.255	2.500	2.320	2.230	3.500	A
(VOUT) RECOV.			-1.275	-1.250	-1.253	-1.260	-1.253	-1.253	-1.225	V
IOS2	-40.00	VF=0V	200.0M	560.0M	570.0M	730.0M	590.0M	625.0M	800.0M	A
(VOUT) RECOV.			-1.275	-1.256	-1.260	-1.268	-1.258	-1.258	-1.225	V
IPEAK	-4.25	VF=-1.0V	1.500	2.245	2.300	2.530	2.365	2.285	3.500	A
(VOUT) RECOV.			-1.275	-1.250	-1.253	-1.260	-1.251	-1.253	-1.225	V
IQ1	-4.25	VF=-1.4V	200.0U	540.0U	400.0U	416.0U	352.0U	400.0U	3.000M	A
IQ2	-14.25	VF=-1.4V	200.0U	960.0U	480.0U	480.0U	448.0U	560.0U	3.000M	A
IQ3	-41.25	VF=-1.4V	1.000M	2.882M	1.920M	1.800M	1.720M	2.080M	5.000M	A
VSTART	-4.25	1500	-1.275	-1.250	-1.253	-1.260	-1.252	-1.253	-1.200	V

NOTE #1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

TABLE 12-8. NEG. ADJ. VOLTAGE REGULATOR - LM137H T_A = 25°C 6-16-79

PARAMETER	CONDITONS	LO - LIMIT	S/N1	S/N2	S/N3	S/N4	S/N5	HI - LIMIT	UNITS
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = -6.25V e_i = 1 V_{RMS} @ 2400 Hz I_L = 125 mA	48	60.0	57.7	60	59.2	57.7	-	dB
V_{NO}	V_{IN} = -6.25V I_L = 50 mA	-	70	70	70	70	70	120	uV_{RMS}
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = -6.25V ΔV_{IN} = -1.0V I_L = 10 mA	-	30	36	35	30	38	80	mV/V
$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = -6.25V I_L = 50 mA ΔI_L = 200 mA	-	.05	.05	.04	.045	.05	0.3	mV/mA

Table 12-9. Electrical performance characteristics for device type 01 (79MG) (See 3.4 unless otherwise specified)

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		
		Input Voltage	Load Current	Other	Min.	Max.	Units
Output Voltage	V_{OUT}	V_{IN}=-8V	I_L=5mA, 500mA	3/	-5.25	-4.75	V
		V_{IN}=-30V	I_L=5mA, 50mA				
		V_{IN}=-10V	I_L=5mA	T_A=150°C 1/			
		V_{IN}=-38V	I_L=500mA	R_1=27.4kΩ R_2=2.21kΩ	-31.5	-28.5	
Line regulation	V_{RLINE}	-30V≤V_{IN}≤-8V	I_L=50mA	Figure 12	-150	150	mV
		-25V≤V_{IN}≤-8V	I_L=350mA	Waveforms	- 50	50	
Load regulation	V_{RLOAD}	V_{IN}=-10V	5mA≤I_L≤500mA	Figure 12	-100	100	
		V_{IN}=-30V	5mA≤I_L≤50mA	Waveforms	-150	150	
Thermal regulation	$V_{RTH.}$	V_{IN}=-15V	I_L=500mA	T_A-25°C Figure 12 Waveforms	- 50	50	
Standby current drain	I_{SCD}	V_{IN}=-10V	I_L=5mA		0.1	3.0	mA
		V_{IN}=-30V	I_L=5mA		0.1	4.0	
Standby current drain change versus line voltage	ΔI_{SCD} (LINE)	-30V≤V_{IN}≤-8V	I_L=5mA		-1.0	1.0	
Standby current drain change versus load current	ΔI_{SCD} (LOAD)	V_{IN}=-10V	5mA≤I_L≤500mA		-0.5	0.5	
Control pin current	I_{CTL}	V_{IN}=-10V	I_L=350mA	T_A=25°C	0.001	2.00	μA
				-55°C≤T_A ≤125°C	0.001	3.00	μA
Output short circuit current	I_{OS1}	V_{IN}=-10V		Figure 12	0.002	2.0	A
	I_{OS2}	V_{IN}=-30V		Waveforms	0.002	1.0	
Output voltage recovery after output short circuit current	V_{OUT} (RECOV)	V_{IN}=-10V	R_L=10Ω; CL =20μf	After I_{OS1} 2/	-5.25	-4.75	V
		V_{IN}=-30V	R_L=5kΩ	After I_{OS2}			
Voltage Start-up	V_{START}	V_{IN}=-20V	R_L=10Ω; CL =20μF		-5.25	-4.75	
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN}=-10V Ci=1Vrms @f=2400 Hz	I_L=125mA	Figure 13 T_A=25°C	45	--	dB
Output noise voltage	V_{NO}	V_{IN}=-10V	I_L=50mA	Figure 14 T_A=25°C BW=10Hz to 10kHz	--	250	μVrms
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN}=-10V V_{PULSE}=-3.0V	I_L=5mA	Figure 15 T_A=25°C	--	30	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN}=-10V	I_L=50mA ΔI_L=200mA	Figure 16 T_A=25°C	--	2.5	mV/mA

Table 12-9. (Cont'd)

NOTES:
1. All tests performed at T_A=125°C may, at the manufacturer's option, be performed at T_A=150°C. Specifications for T_A=125°C shall then apply at TA-150°C.

2. Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the I_{OS} test forced output voltage condition. Voltage recovery for conditions other than those specified is not guaranteed.

3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

Table 12-10. Electrical performance characteristics for device type 02 (79G)
(See 3.4 unless otherwise specified)

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		Units
		Input Voltage	Load Current	Other	Min.	Max.	
Output Voltage	V_{OUT}	V_{IN}=-8V V_{IN}=-30V V_{IN}=-10V	I_L=5ma, 1000mA I_L=5mA, 100mA I_L=5mA	3/ T_A=150°C 1/	-5.25	-4.75	V
		V_{IN}=-38V	I_L=1000mA	R_1=27.4kΩ R_2=2.21kΩ	-31.5	-28.5	
Line regulation	VRLINE	-30V≤V_{IN}≤-8V -25V≤V_{IN}≤-8V	I_L=100mA I_L= 500mA	Figure 12 Waveforms	-150 - 75	150 75	mV
Load regulation	VRLOAD	V_{IN}=-10V V_{IN}=-30V	5mA≤I_L≤1000mA 5mA≤I_L≤100mA	Figure 12 Waveforms	-100 -150	100 150	
Thermal regulation	VRTH.	V_{IN}=-15V	I_L=1000mA	T_A=25°C Figure 12 Waveforms	- 50	50	
Standby current drain	I_{SCD}	V_{IN}=-10V V_{IN}=-30V	I_L=5mA I_L=5mA		0.5 0.5	3.0 4.0	mA
Standby current drain change versus line voltage	ΔISCD (LINE)	-30V≤V_{IN}≤-8V	I_L=5mA		-1.0	1.0	
Standby current drain change versus load current	ΔISCD (LOAD)	V_{IN}=-10V	5mA≤I_L≤1000mA		-0.5	0.5	
Control pin current	I_{CTL}	V_{IN}=-10V	I_L=500mA	T_A=25°C -55°C≤T_A ≤125°C	0.01 0.001	2.00 3.00	μA μA
Output short circuit current	I_{OS1} I_{OS2}	V_{IN}=-10V V_{IN}=-30V		Figure 12 Waveform	0.002 0.002	4.5 2.0	A
Output voltage recovery after output short circuit current	V_{OUT} (RECOV)	V_{IN}=-10V V_{IN}=-30V	R_L=5Ω; C_L=20μF R_L=5kΩ	After I_{OS1} 2/ After I_{OS2}	-5.25	-4.75	V
Voltage start-up	V_{START}	V_{IN}=-20V	R_L=5Ω; C_L=20uF		-5.25	-4.75	
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN}=-10V C_1=1Vrms @f=2400Hz	I_L=350mA	Figure 13 T_A=25°C	45	--	dB
Output noise voltage	V_{NO}	V_{IN}=-10V	I_L=100mA	Figure 14 T_A=25°C BW=10Hz to 10kHz	--	250	μVrms
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN}=-10V V_{PULSE}=-3.0V	I_L=5mA	Figure 15 T_A=25°C	--	30	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN}=-10V	I_L=100mA ΔI_L=400mA	Figure 16 T_A=25°C	--	2.5	mV/mA

Table 12-10. (Cont'd)

NOTES: 1. All tests performed at T_A=125°C may, at the manufacturer's option, be performed at T_A=150°C. Specifications for T_A=125°C shall then apply at T_A=150°C.

2. Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the I_{OS} test forced output condition. Voltage recovery for conditions other than those specified is not guaranteed.

3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

Table 12-11 Electrical performance characteristics for device type 03 (LM137H)
(See 3.4 unless otherwise specified)

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		Units
		Input Voltage	Load Current	Other	Min.	Max.	
Output Voltage	V_{OUT}	V_{IN}=-4.25V	I_L=5mA, 500mA	3/	-1.300	-1.200	V
		V_{IN}=-41.25V	I_L=5mA, 50mA				
		V_{IN}=-6.25V	I_L=5mA	T_A=150°C 1/			
Line regulation	VRLINE	-41.25V≤V_{IN} ≤-4.25V	I_L=5mA	T_A=25°C	-9	9	mV
				-55°C T_A 125°C	-23	23	
Load regulation	VRLOAD	V_{IN}=-6.25V	5mA≤I_L≤200mA	T_A=25°C	-6	6	
				-55°C≤T_A ≤125°C	-12	12	
			5mA≤I_L≤500mA	T_A=25°C	-12	12	
				-55°C≤T_A ≤125°C	-24	24	
		V_{IN}=-41.25V	5mA≤I_L≤50mA	T_A=25°C	- 6	6	
				-55°C≤T_A ≤125°C	-12	12	
Thermal regulation	VRTH.	V_{IN}=-14.6V	I_L=750mA	T_A=25°C	- 5	5	
Adjust pin current	I_{ADJ}	V_{IN}=-4.25V	I_L=5mA		25	100	μA
		V_{IN}=-41.25V	I_L=5mA		25	100	
Adjust pin current change versus line voltage	ΔI_{ADJ} (LINE)	-41.25V≤I_L ≤-4.25V	I_L=5mA		- 5	5	
Adjust pin current change versus load current	ΔI_{ADJ} (LOAD)	V_{IN}=-6.25V	5mA≤I_L≤500mA		- 5	5	
Minimum load current	I_Q	-14.25V≤V_{IN} ≤-4.25V forced V_{OUT} =-1.4V			0.20	3.00	mA
		V_{IN}=41.25V forced V_{OUT} =-1.4V			1.00	5.00	
Output short circuit current	I_{OS1}	V_{IN}=-4.25V			0.5	1.8	A
	I_{OS2}	V_{IN}=-40V			0.05	0.5	A
Output voltage recovery after output short circuit current	V_{OUT} (RECOV)	V_{IN}=-4.25V	R_L=2.5Ω; C_L =20μF	After I_{OS1} 2/	-1.300	-1.200	V
		V_{IN}=-40V	R_L=250Ω	After I_{OS2}			
Voltage start-up	V_{START}	V_{IN}=-4.25V	R_L=2.5Ω; C_L =20μF		-1.300	-1.200	
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN}=-6.25V C_f=1Vrms dfo=2400 Hz	I_L=125mA	Figure 13 T_A=25°C	48	--	dB

Table 12-11. Electrical performance characteristics for device type 03 (LM137H) (Cont'd) (See 3.4 unless otherwise specified)

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		
		Input Voltage	Load Current	Other	Min.	Max.	Units
Output noise voltage	V_{NO}	V_{IN}=-6.25V	I_L=50mA	Figure 14 T_A=25°C BW=10 Hz to 10kHz	--	120	μVrms
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN}=-6.25V ΔV_{IN}=-1.0V	I_L=10mA	Figure 15 T_A=25°C	--	80	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN}=-6.25V	I_L=50mA ΔI_L=200mA	Figure 16 T_A=25°C	--	0.30	mV/mA

NOTES: 1. All tests performed at T_A=125°C may, at the manufacturer's option, be performed at T_A=150°C.

2. Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the I_{OS} test forced output voltage condition. Voltage recovery for conditions other than those specified is not guaranteed.

3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

Table 12-12. Electrical performance characteristics for device type 04 (LM137K) (See 3.4 unless otherwise specified)

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		Units
		Input Voltage	Load Current	Other	Min.	Max.	
Output Voltage	V_{OUT}	V_{IN}=-4.25V	I_L=5mA, 1500mA	3/	-1.300	-1.200	V
		V_{IN}=-41.25V	I_L=5mA, 200mA				
		V_{IN}=-6.25V	I_L=5mA	T_A=150°C 1/			
Line regulation	V_{RLINE}	-41.25V≤ V_{IN} ≤-4.25V	I_L=5mA	T_A=25°C	- 9	9	mV
				-55°C≤T_A ≤125°C	-23	23	
Load regulation	V_{RLOAD}	V_{IN}=-6.25V	5mA≤I_L≤1500mA	T_A=25°C	- 6	6	
				-55°C≤T_A ≤125°C	-12	12	
		V_{IN}=-41.25V	5mA≤I_L≤150mA	T_A=25°C	- 6	6	
				-55°C≤T_A ≤125°C	-12	12	
Thermal regulation	$V_{RTH.}$	V_{IN}=-14.6V	I_L=1500mA	T_A=25°C	- 5	5	
Adjust pin current	I_{ADJ}	V_{IN}=-4.25V	I_L=5mA		25	100	µA
		V_{IN}=-41.25V	I_L=5mA		25	100	
Adjust pin current change versus line voltage	ΔI_{ADJ} (LINE)	-41.25V≤I_L≤ 4.25V	I_L=5mA		- 5	5	
Adjust pin current change versus load current	ΔI_{ADJ} (LOAD)	V_{IN}=-6.25V	5mA≤I_L≤1500mA		- 5	5	
Minimum load current	I_Q	-14.25V≤V_{IN} ≤-4.25V forced V_{OUT} =-1.4			0.20	3.00	mA
					1.00	5.00	
		V_{IN}=-41.25V forced V_{OUT} =-1.4V			1.00	5.00	
Output short circuit current	I_{OS1}	V_{IN}=-4.25V			1.5	3.5	A
	I_{OS2}	V_{IN}=-40V			0.2	0.8	A
Output voltage recovery after output short circuit current	V_{OUT} (RECOV)	V_{IN}=-4.25V	R_L=.833Ω; C_L =20µF	After I_{OS1} 2/	-1.300	-1.200	V
		V_{IN}=-40V	R_L=250Ω	After I_{OS2}			
Voltage start-up	V_{START}	V_{IN}=-4.25V	R_L=.833Ω; C_L =20µF		-1.300	-1.200	
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN}=-6.25V C_i=1Vrms @fo=2400Hz	I_L=500mA	Figure 13 T_A=25°C	50	--	dB
Output noise voltage	V_{NO}	V_{IN}=-6.25V	I_L=100mA	Figure 14 T_A=25°C BW=10Hz to 10kHz	--	120	µVrms

Table 12-12. Electrical performance characteristics for device type 04 (LM137K) (Cont'd) (See 3.4 unless otherwise specified)

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		
		Input Voltage	Load Current	Other	Min.	Max.	Units
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN}=-6.25V ΔV_{IN}=-1.0V	I_L=10mA	Figure 15 T_A=25°C	--	40	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN}=-6.25V	I_L=100mA ΔI_L=400mA	Figure 16 T_A=25°C	--	0.15	mV/mA

NOTES:

1. All tests performed at T_A=125°C may, at the manufacturer's option, be performed at T_A=150°C. Specifications for T_A=125°C shall then apply at T_A=150°C.

2. Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the IOS test forced output voltage condition. Voltage recovery for conditions other than those specified is not guaranteed.

3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

SECTION XIII

PRECISION VOLTAGE REFERENCES
MIL-M-38510/124

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SECTION XIII

PRECISION VOLTAGE REFERENCES

MIL-M-38510/124

13.1 Introduction

As precision and accuracy of control systems increase, the need for a stable, precise voltage reference becomes apparent.

Precision voltage references are used in ratiometric measurement systems as a reference against which all signal voltages can be compared, and in high accuracy data converter circuits. The two precision voltage references characterized for this slash sheet are the LM129A and the LM199A. These devices were selected by RADC, GEOS and members of the JC-41 Committee for characterization. The LM129A's and LM199A's were tested in test circuits devised to check each parameter at all of the specified temperatures.

Table 13-1 lists the device types specified for this characterization.

Table 13-1. Device Types Specified.

Device Type	Generic Type	Manufacturer	Output Voltage	Heater Voltage	No. of Terminals
12401	LM199A	NSC	6.95V	$9V \leq V_H \leq 40V$	4
12402	LM129A	NSC	6.95V	N.A.	2

13.2 Description of Device Types

The LM129A and LM199A precision voltage references each incorporate precision temperature compensated 6.9 volt zener references. The design of the silicon chips uses a subsurface zener diode reference to reduce noise and long term stability. The voltage reference, additionally, contains circuitry to buffer the temperature compensated zener diode from current variations that accompany load current changes. The circuit for the LM199A precision voltage reference is shown in Figure 13-1.

The precision reference circuit in this figure is comprised of two circuits on a single monolithic silicon chip. One circuit is a temperature stabilizer. The other circuit is the voltage reference. The voltage reference consists of a reference diode, D3, a current shunt circuit, Q10-Q13 and a current mirror, Q14-Q16. The reference diode is

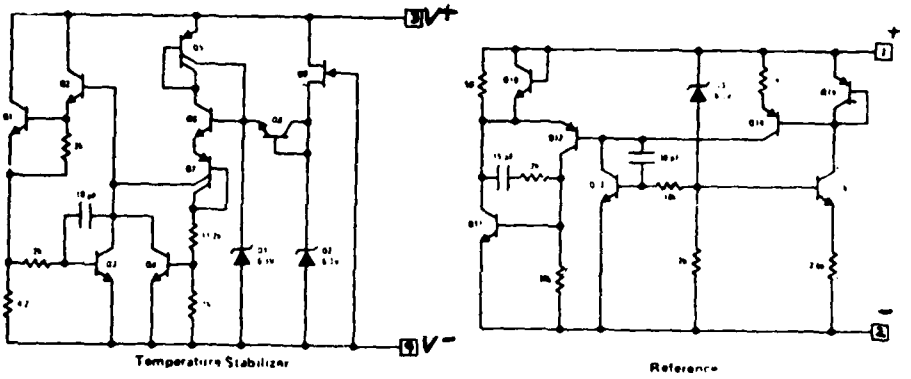

Figure 13-1. Schematic of LM199A voltage reference.

temperature compensated by adjusting the diode current for 0-T.C. This is accomplished by adjusting the 10 Kohm resistor in the base of transistor Q13. Transistor Q13 serves to buffer any reference circuit current variations from the reference diode. By adjusting the 30 Kohm resistor in the collector of Q12, the increase in shunt current can be made approximately equal to the decrease in current supplied to the load. The only current change to the reference diode is due to the small change in transistor Q13 base current. Transistors Q14-Q16 form a current mirror and serve as a constant current, active load for transistor Q13. Because the reference diode is temperature compensated and because the current shunt handles the main variations in current, the reference circuit maintains a stable output for large variations of both temperature and current. This stability is observed in both the LM129A and LM199A precision references.

The LM199A differs from the LM129A in that it also contains a temperature stabilizer circuit. The temperature stabilizer circuit operates from a separate supply voltage that may range from 9V to 40 V. The circuit draws current from this supply so as to maintain a constant chip temperature of approximately 85°C. As the chip ambient temperature decreases, the stabilizer draws more current from the supply and increases the power dissipation on the chip. Thus, the chip temperature tends to remain constant. For temperatures above 85°C, the temperature stabilizer is no longer effective and the LM199A precision reference performance is essentially degraded to that of the LM129A.

13.3 Test Development

The devices used in these characterizations were selected and approved by a joint decision of RADC, the JC-41 Committee and the Circuit Design Engineering activity of GEOS. The devices were obtained from National Semiconductor Corporation and from their distributors. Table 13.2 lists the device types characterized.

Table 13-2. Device Types Characterized.

Device Type	S/N	Manufacturer	Date Code
12401	1-21	NSC	7641, 7803
12402	1-23	NAC	7826, 7839

Test Parameter Development

Test parameters were recommended by the manufacturer and were approved by the JC-41 Committee. In addition, extra tests were added by GEOS to extend the characterization study beyond the recommended tests in Table I of the device slash sheet. Except for certain dynamic test parameters, tests were performed at -55°C, 25°C and 125°C, and additionally at 85°C for device type 12401. Noise, dynamic impedance and warm-up were performed at one current level at 25°C. A list of the electrical parameters tested during characterization is presented in Table 13-3.

Table 13-3. Test Parameters for Characterization.

Item No.	Symbol	Parameter
1	V_R	Reference voltage
2	delta V_R (current)	Reference voltage change with current
3	delta V_R/delta T	Reference voltage temperature coefficient
4	Z_D	Dynamic impedance
5	N_O	Output noise
6	delta V_R (temp cycle)	Reference voltage temperature cycling hysteresis
7	delta V_R/delta t	Reference voltage long term stability
8	I_S	Temperature stabilizer supply current
9	I_{SI}	Initial temperature stabilizer supply current

Test Circuit Development

All evaluation and characterization of the precision voltage reference was performed in bench test set-ups, and d.c. measurements were made on an HP3455 voltmeter using Kelvin connections to the DUT pins.

Figure 13-2 shows the test circuit used to measure breakdown voltage. The breakdown voltage measurements on the LM129A devices were made at current levels of 0.6 mA, 1.0 mA and 15 mA. For the LM199a, these measurements were made at current levels of 0.5 mA, 1.8 mA, 5 mA, 10.0 mA and 11.3 mA with the temperature stabilizer supply voltages set at 30 volts. Additional measurements were made with the temperature stabilizer supply voltages set at 9 volts and 40 volts.

The noise test circuit is also shown in Figure 13-2. Measurements were made on a Tektronix model 7904 oscilloscope with a model 7A22 differential input preamplifier. The bandwidth on the preamp was adjusted for 10 Hz $\leq$ BW $\leq$ 10 kHz and peak-to-peak measurements were made on the oscilloscope.

The dynamic impedance test circuit is shown in Figure 13-3. Measurements were made using a 400 Hz signal source and a voltmeter with a 400 Hz narrow band filter. AC signal levels were low in order to insure small signal impedance measurements. Kelvin connections were used and contact was made 1/8" below the reference case.

The initial temperature stabilizer supply current was measured using a Tektronix model storage oscilloscope with a current probe. The peak current was recorded from the oscilloscope.

13.4 Test Results and Data

A summary of the test data is presented in Tables 13-4 through 13-6. The summary presents the higher measured value, the lowest measured value, the calculated mean value and the standard deviation for each parameter and set of test conditions. Several measurements were made with test conditions that are not defined in the slash sheet. For example, data was obtained on the LM199A devices at five different currents, three different temperature stabilizer voltages and four different temperatures in order to characterize the reference voltage output, the temperature coefficient and the temperature stabilizer. In addition, dynamic impedance and output noise were measured at 25°C. Some of this data was strictly for characterization and provides data on conditions not specified by the vendor or recommended for the device slash sheet.

Table 13-4 tabulates the analyzed, measured data taken on the LM129A. Measurements were made on the devices with supply currents of .6 mA, 1.0 mA and 15 mA. The reference voltage measurements were all well within

the manufacturer's specified limits and a population hystogram of these voltages is shown in Figure 13-4.

Data for the evaluation of the temperature coefficient was obtained by measuring the output voltage at the various specified temperatures and calculating the measurement difference in PPM/°C. For this characterization effort similar data was obtained for device currents of .5 mA and 15 mA, and data was used in the analysis of temperature coefficient change with current.

Noise measurements were made of the peak-to-peak value of the noise. The mean value of these measurements was 69.8 uV. Since broad-band white noise (RMS value) = (peak-to-peak value)/6, the mean RMS value is 11.6 uVrms. Dynamic impedance measurements were made and the mean value of these measurements is .74 ohms.

Tables 13-5 and 13-6 summarize the analysis of the measured data for the LM199A. LM199A data for various reference voltage currents was taken with the thermal stabilizer supply voltage set to 30 volts. The reference voltage current values varied from .5 mA to 11.3 mA. A population hystogram of the reference voltage output is presented in Figure 13-6. The data was within the specified limits. Output reference voltage measurements were made with I_R = 11.3 mA and with V_S = 9 V and 40 V. For these two conditions, the output reference voltage is 6.96457 Vdc and 6.96488 Vdc. With I_R = 1.8 mA and with V_S = 9 V and 40 V, the two output voltage measurements are 6.95897 Vdc and 6.95949 Vdc. Since the thermal stabilizer temperature does not regulate to the maximum temperature of 125°C, two temperature coefficient specifications are required. One T.C. tolerance of .5PPM/°C covers the temperature range from -55°C to 85°C. The other tolerance of 10 PPM/°C covers the temperature range from 85°C to 125°C.

Table 13-5 tabulates the results of the analyzed data for dynamic impedance, noise and T.C. changes with current. Noise measurements were made of the peak-to-peak value of the noise. The mean value of these measurements was 73.5 uV p-p. Since broad-band white noise (RMS value) = (peak-to-peak value) /6, the mean RMS value is 12.25 uVrms.

Table 13-5 also tabulates the analysis of measured data for LM199A Reference Voltage Warm-up Stability and Reference Voltage Temperature Cycling Hysteresis. Data was also taken to determine the power dissipation of the thermal stabilizer versus temperature. The results of this data is tabulated in Table 13-6 and is graphed on Figure 13-5.

13.5 Discussion of Results

LM129A

A summary of the measured and calculated data is presented in Table 13-4. Reference voltage measurements were made on twenty-one devices.

The devices all had output voltage measurement that were slightly below the normal of 6.95 $\pm$ .25 volts. The mean value for I_R = 1 mA was 6.8724 with a standard deviation of .02 volts.

The temperature coefficient for these devices is determined by measuring the output reference voltage at -55°C, 25°C & 125°C. The mean temperature coefficient for these devices is -0.3 PPM/°C with a standard deviation of 3.1 PPM/°C for a temperature range from -55°C to 25°C. The mean temperature coefficient over the temperature range from 25°C to 125°C was + 3.8 PPM/°C with a standard deviation of 2.8 PPM/°C. These values are well within the specification of $\pm$ 10 PPM/°C.

Analysis of the calculated temperature coefficient versus current shows that the T.C. change with current, over the temperature range from -55°C to 25°C, has a mean value of 0.8 PPM/°C with a standard deviation of 0.8 PPM/°C. Over the temperature range from 25°C to 125°C, the mean value of the T.C. change with current is -1.9 PPM/°C with a mean value of 1.3 PPM/°C. This value is greater than the vendor's typical specification of 1 PPM/°C, however, the parts received by GEOS for characterization were not screened for this parameter.

LM199A

A summary of the measured and calculated data is presented in Table 13-5 and 13-6 for the reference voltage and the temperature stabilizer, respectively. Reference voltage measurements were made on thirteen devices. The output voltage was measured at several currents from 0.5 mA to 11.3 mA. The mean value of the output voltage with a current of I_R= 1.0 mA was interpolated from measured values. The mean value is 6.95863 volts.

The mean temperature coefficient for I_R = 1 mA was determined for temperature ranges from -55°C to 25°C, 25°C to 85°C and 85°C to 125°C. The mean value was obtained by interpolating measured data from I_R = 0.5 mA to I_R = 1.8 mA, and for the above temperature ranges, the mean values were - .075 PPM/°C, - .18 PPM/°C & - .82 PPM/°C, respectively. Data presented in Table 13-5 shows that the T.C. range increases as current through the reference voltage circuit increases. For currents of 5 mA and larger, the standard deviation of the temperature coefficients is larger than the 1 mA limit for a temperature range from 25°C to 85°C.

Peak to peak noise, dynamic impedance and temperature cycling hysteresis measurements were made. The measurements were all within the specified limits. Reference voltage warm-up stability measurements were made at t = 10 sec, t = 1 min & t = 5 min. The measured data indicated that the LM199A reference voltage device requires several minutes for warm-up.

Data taken to determine temperature stabilizer power dissipation was tabulated in Table 13-6 and plotted in Figure 13-5. The graph shows the linearity of the change in power dissipation versus temperature for zero current in the reference voltage circuit. From this information the average thermal resistance is calculated as

$$\theta = (538.7 - 78.0)/(85 + 55) = 3.29 \text{ mW/}^{o}\text{C}$$

The vendor was contacted on this matter and confirmed that the figure should be 2 - 5 mV/^{o}C. The vendor recommends that the thermal resistance should be nominally specified at 5 mV/^{o}C. The total device power dissipation is the sum of the thermal stabilizer circuit power and the reference voltage circuit power. (PT = PTS + PR). The graph, in Figure 13-5, shows how the thermal stabilizer power dissipation is affected by the added power dissipation of the voltage reference.

13-6. Slash Sheet Development

Table I of the slash sheet was developed from the manufacturer's data sheet. Additional test parameters were proposed for characterization and were added to the table. These test parameters were then negotiated with the manufacturer and the resultant table is shown in Table 13-7. Because some of the tests proposed for characterization are expensive to perform, they have been left off the slash sheet. The slash sheet was finalized and submitted to RADC & DESC. Additional negotiations between the vendor and RADC resulted at the time of the initial release of the slash sheet. At the time of this writing the results of these negotiations were being included in the slash sheet.

13.7 Conclusions and Recommendations.

The data obtained for these analyses showed that the reference voltage devices met the specifications published by the manufacturer. Other parameters, not one hundred percent guaranteed by the manufacturer but recommended by the JC-41 Committee, were measured and the data was analyzed. Data taken on the temperature coefficient change with current showed that some devices had values much greater than the published typical value. The manufacturer states that this parameter can be guaranteed but the additional tests will add extra cost to the parts. It was decided not to recommend specification of the parameter.

Additional tests, such as, power off/on repeatibility, warm-up stability, and temperature cycling hysteresis have been checked. These parameters require extreme care in order to obtain reliable test data. The power off/on data was obtained as a consequence of the warm-up test data at time = 5 min. These data are shown in Table 13-5. GEOS does not recommend that the power off/on and warm-up test be a part of the slash sheet. No major anomalies were uncovered during this characterization. A minor anomaly was observed in the measurement of temperature

coefficient change with current. As the voltage reference current and temperature were increased simultaneously to their maximum, the T.C. change increased until it was 2-3 times the value at low current and temperature.

Table 13-7 lists the recommended parameters for these devices.

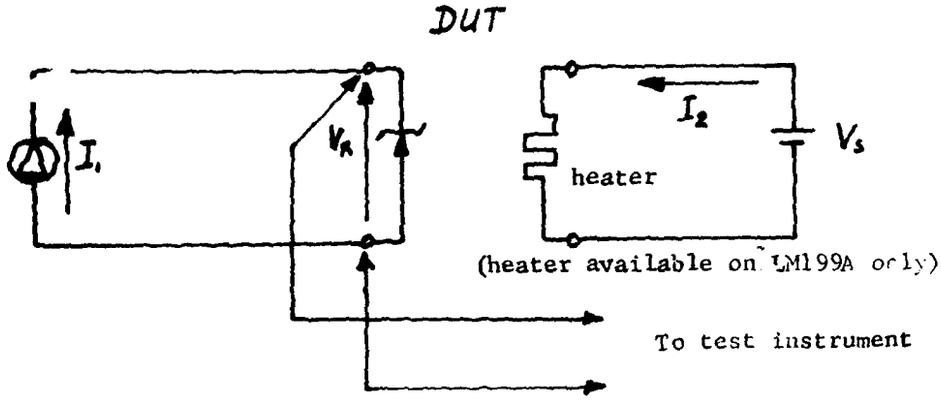

Figure 13-2. Reference voltage and noise test circuit.

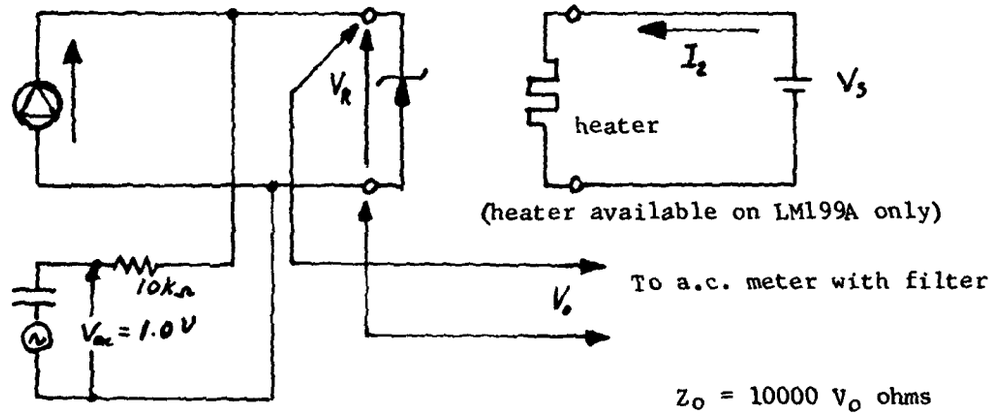

Figure 13-3. Dynamic impedance test circuit.

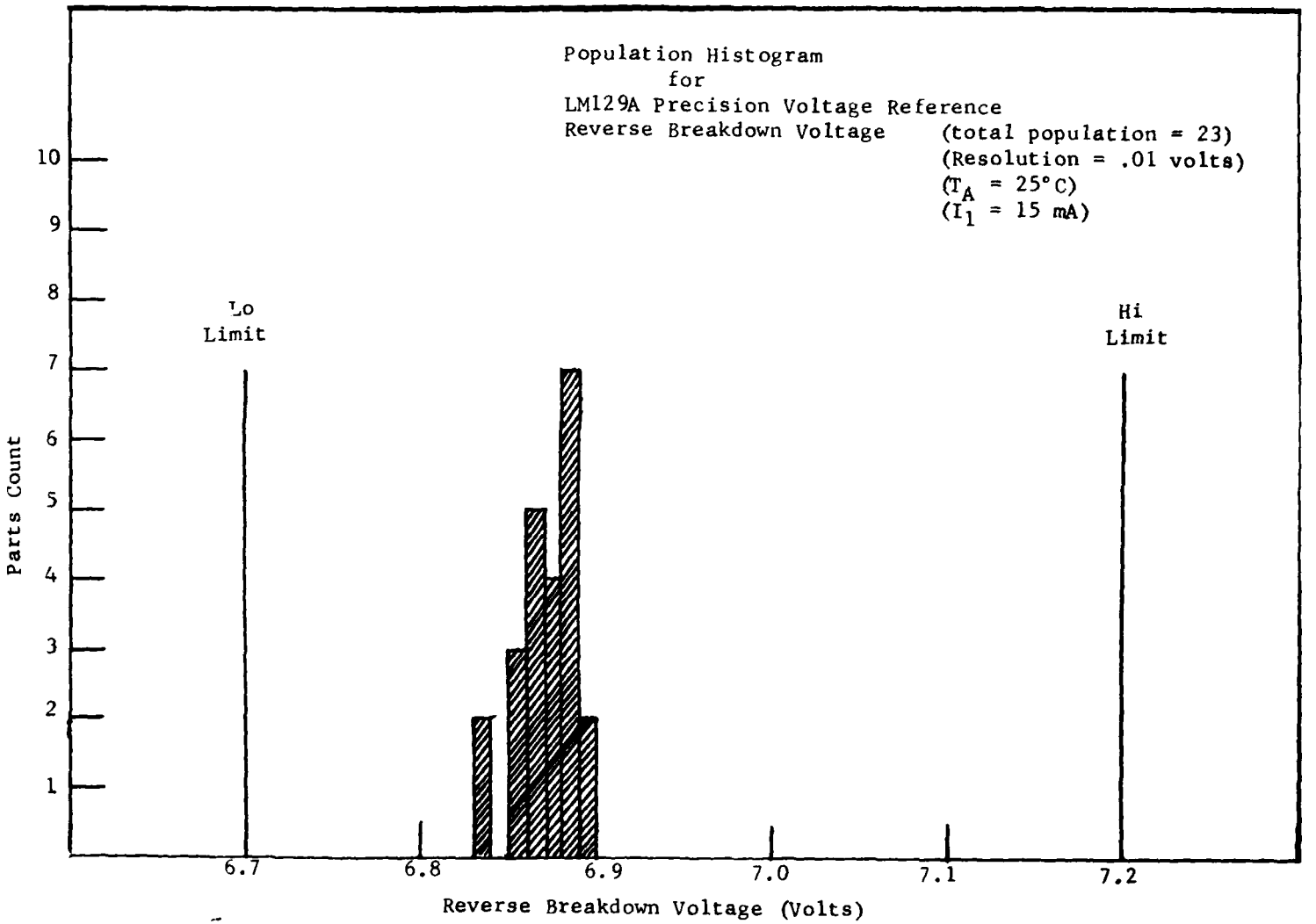

Figure 13-4. Population histogram for LM129A precision voltage reference.

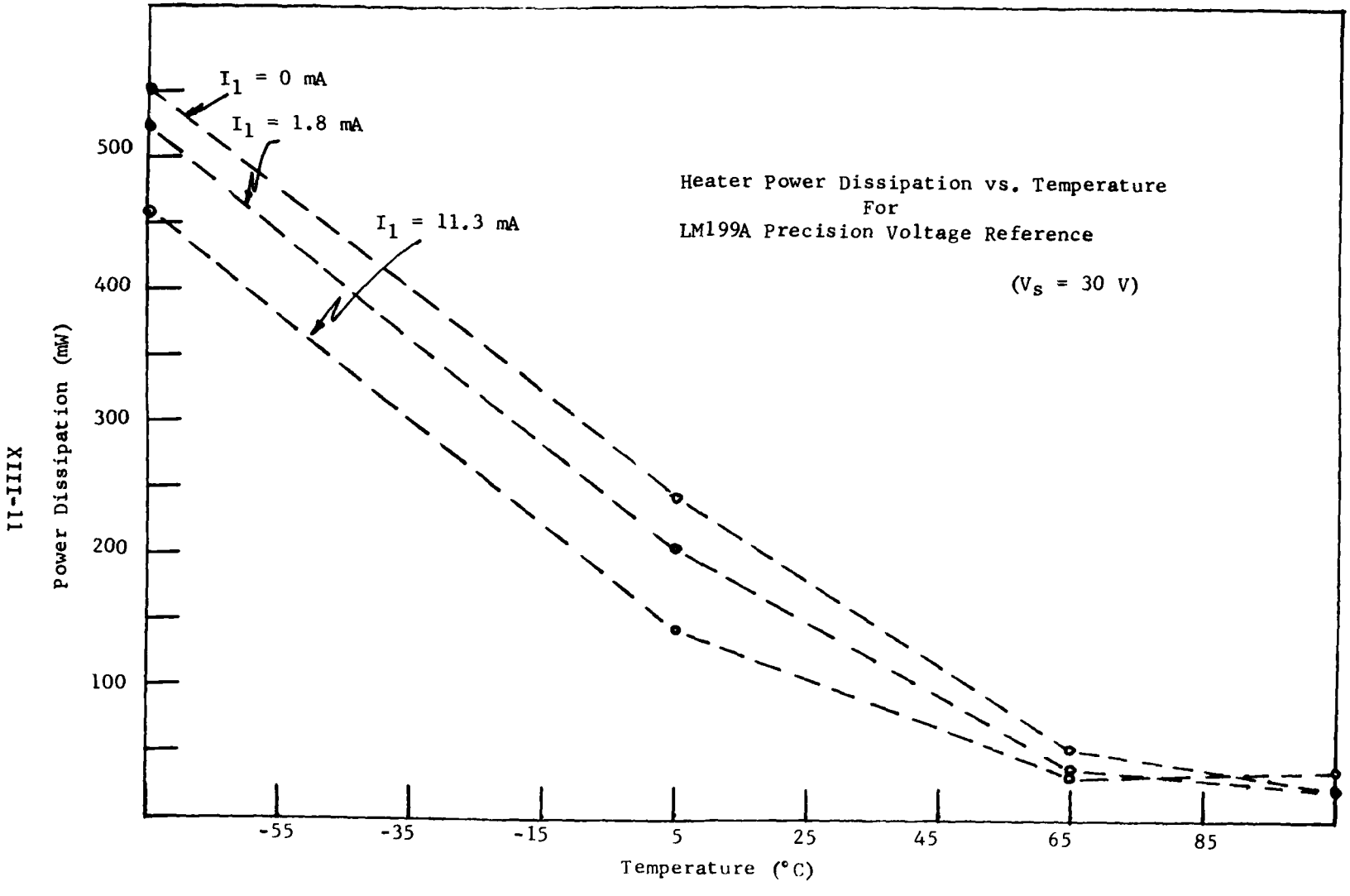

Figure 13-5. Heater power dissipation versus temperature for different reference currents.

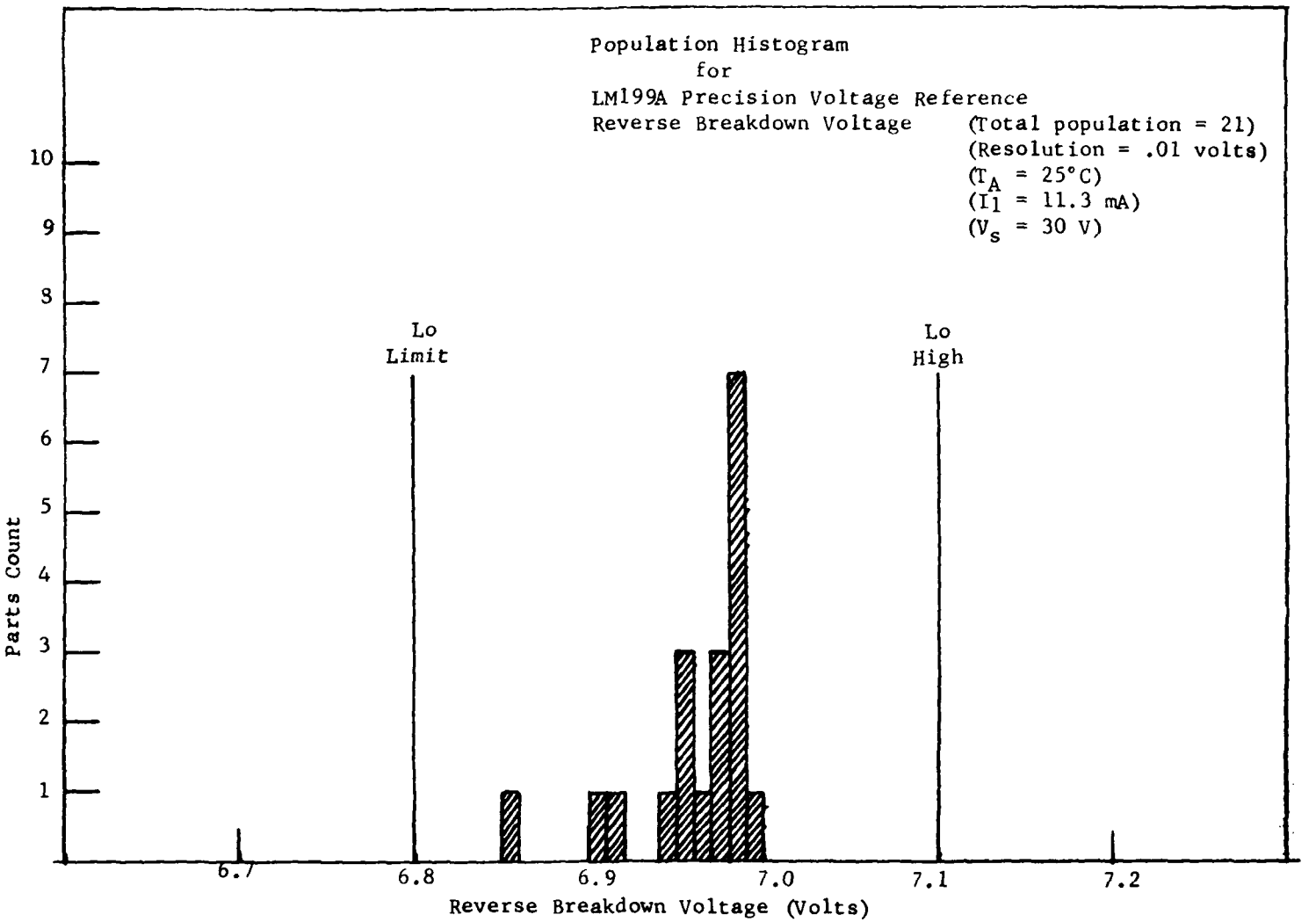

Figure 13-6. Population histogram for LM199A precision voltage reference.

Table 13-4. Summary of Measurements (LM129A).

Parameter	Conditions	Limits Min	Limits Max	Data (21 Units) Hi	Low	Mean	Std. Dev.
Reference Voltage 25° (volts)	I_R = 0.6 mA	6.70	7.20	6.8922	6.8360	6.82718	.02
	I_R = 1.0 mA			6.8927	6.8360	6.8724	.02
	I_R = 15 mA			6.9036	6.8455	6.8852	.02
Temperature coefficient $-55°C \leq T_A \leq 25°C$ (PPM/°C)	I_R = 0.6 mA	-10	10	4.2	-6.1	-0.5	3.0
	I_R = 1.0 mA	-10	10	4.2	-6.8	-0.3	3.1
	I_R = 15 mA	-10	10	2.3	-7.3	-1.8	2.8
Temperature coefficient $25°C \leq T_A \leq 125°C$ (PPM/°C)	I_R = 0.6 mA	-10	10	8.0	-7.7	3.8	3.6
	I_R = 1.0 mA	-10	10	7.2	-2.5	3.8	2.8
	I_R = 15 mA	-10	10	8.4	-1.2	4.5	2.7
Change in temperature coefficient with current	1 mA $\leq I_R \leq$ 15 mA						
$-55°C \leq T_A \leq 25°C$				2.1	-1.2	0.8	0.8
$25°C \leq T_A \leq 125°C$ (PPM/°C)				-0.6	-5.2	-1.9	1.3
Peak-to-peak noise (uV)	I_R = 1 mA	-	20uV (RMS)			69.8	4.9
Dynamic Impedance (ohms)	I_R = 1 mA	-	1			.74	.24

Table 13-5. Summary of Reference Voltage Measurements (LM199A)

Parameters	Conditions	Limits Min	Limits Max	Data (13 Units) High	Low	Mean	Std. Dev.
Reference voltage 25°C (volts).	I_R = .5 mA	6.800	7.100				
	V_S = 30 V			6.9899	6.9025	6.9582	.03
	I_R = 1.8 mA						
	V_S = 30 V			6.99376	6.84427	6.95932	.03
	I_R = 5 mA						
	V_S = 30 V			6.9929	6.9055	6.9613	.03
	I_R = 10 mA						
	V_S = 30 V			6.9955	6.9085	6.9640	.03
	I_R = 11.3 mA						
	V_S = 30 V			6.99934	6.85108	6.96484	.03
	I_R = 1.8 mA						
	V_S = 9V			6.99343	6.84392	6.95897	.03
	I_R = 11.3 mA						
	V_S = 9V			6.99912	6.85086	6.96457	.03
	I_R = 1.8 mA						
	V_S = 40 V			6.99383	6.84433	6.95949	.03
	I_R = 11.3 mA						
	V_S = 40 V			6.99938	6.85109	6.96488	.03
Temperature coefficient $-55°C \leq T_A \leq 25°C$ (PPM/°C)	I_R = .5 mA	-.5	.5				
	V_S = 30 V			0.0	-.54	-.31	.17
	I_R = 1.8 mA						
	V_S = 30 V			.72	0.0	.30	.20
	I_R = 5 mA						
	V_S = 30 V			.54	-.54	.03	.25
	I_R = 10 mA						
	V_S = 30 V			.72	-.18	.36	.23
	I_R = 11.3 mA						
	V_S = 30 V			1.6	-.36	.70	.40
	I_R = 1.8 mA						
	V_S = 9V			1.6	.72	1.2	.30
	I_R = 11.3 mA						
	V_S = 9V			1.8	.54	1.5	.30
	I_R = 1.8 mA						
	V_S = 40 V			.59	-.18	.23	.20
	I_R = 11.3 mA						
	V_S = 40 V			1.1	.18	.60	.30

Table 13-5. Summary of Reference Voltage Measurements (LM199A) (Cont'd)

Parameters	Conditions	Limits Min	Limits Max	Data (13 Units) High	Low	Mean	Std. Dev.
Temperature coefficient $25^{o}C \leq T_A \leq 85^{o}C$ (PPM/°C)	I_R = .5 mA, V_S = 30 V	-.5	.5	.24	-.95	-.50	.34
	I_R = 1.8 mA, V_S = 30 V			.70	0.0	.32	.30
	I_R = 5 mA, V_S = 30 V			1.9	-.72	.28	.80
	I_R = 10 mA, V_S = 30 V			1.9	-1.2	.91	.90
	I_R = 11.3 mA, V_S = 30 V			3.3	-.70	2.2	1.4
	I_R = 1.8 mA, V_S = 9 V			1.4	.50	1.1	.30
	I_R = 11.3 mA, V_S = 9 V			3.4	.50	2.3	1.0
	I_R = 1.8 mA, V_S = 40 V			.70	.20	.30	.30
	I_R = 11.3 mA, V_S = 40 V			3.8	-1.2	2.0	1.6
Temperature coefficient $85^{o}C \leq T_A \leq 125^{o}C$ (PPM/°C)	I_R = .5 mA, V_S = 30 V	-10	10	7.5	-9.4	-1.7	5.0
	I_R = 1.8 mA, V_S = 30 V			9.3	-11.3	.60	6.6
	I_R = 5 mA, V_S = 30 V			9.7	-8.7	3.0	5.5
	I_R = 10 mA, V_S = 30 V			10.0	-10.5	2.8	6.4
	I_R = 11.3 mA, V_S = 30 V			7.3	-7.6	.05	4.1
	I_R = 1.8 mA, V_S = 9 V			10.0	-9.4	2.4	5.6
	I_R = 11.3 mA, V_S = 9 V	-10	10	11.4	-13.7	.90	7.2
	I_R = 1.8 mA, V_S = 40 V			7.9	-9.8	1.4	5.3
	I_R = 11.3 mA, V_S = 40 V			13.9	-12.3	-.30	7.3

Table 13-5. Summary of Reference Voltage Measurements (LM199A) (Concluded)

Parameters	Conditions	Limits Min	Limits Max	Data (13 Units) High	Low	Mean	Std. Dev.
Change in temperature coefficient with current	$1.8mA \leq I_R \leq 11.3$ mA $V_S = 30V$						
$-55^oC \leq T_A \leq 25^oC$		-	-	1.1	-1.1	.30	.50
$25^oC \leq T_A \leq 85^oC$		-	-	3.6	-.70	2.0	1.3
$85^oC \leq T_A \leq 125^oC$ ($PPM/^oC$)		-	-	8.6	-4.5	-1.7	3.4
Peak to peak Noise (uV)	I_R = 1 MA V_S = 30 V	-	20uV (RMS)	80	50	73.5	6.9
Dynamic impedance (ohms)	I_R = 1 mA V_S = 30 V	-	1	8.3	.30	.66	.12
Reference voltage warm-up stability	I_R = 1 mA V_S = 30 V						
t = 10 sec		-	-	15.2	-5.6	7.05	5.4
t = 1 min		-	-	5.07	-9.74	.35	3.8
t = 5 min (PPM)		-	-	1.3	-9.74	-2.4	2.8
Temperature cycling hysteresis	I_R = 1 mA V_S = 30 V						
+ T_A cycle		-10	10	2.03	-2.4	-.57	1.29
- T_A cycle (PPM)		-10	10	1.3	-9.74	-2.4	2.8

Table 13-6. Summary of Temperature Stabilizer Measurements (LM199A).

Parameters	Conditions	Limits Min	Limits Max	Data (13 Units) High	Low	Mean	Std. Dev.
Temperature stabilizer power dissipation T_A = -55°C (mW)	I_R = 0 mA, V_S = 30 V	-	-	579.3	512.4	538.7	21.1
	I_R = 1.8 mA, V_S = 30 V	-	-	567.0	491.7	522.0	22.3
	I_R = 11.3 mA, V_S = 30 V	-	-	501.9	425.7	458.4	24.4
	I_R = 1.8 mA, V_S = 9 V	-	-	569.7	476.1	521.6	27.1
	I_R = 11.3 mA, V_S = 9 V	-	-	504.0	421.2	457.6	24.5
	I_R = 1.8 mA, V_S = 40 V	-	-	566.4	486.0	521.6	23.9
	I_R = 11.3 mA, V_S = 40 V	-	-	503.2	411.6	457.0	25.6
Temperature stabilizer power dissipation T_A = 25°C (mW)	I_R = 0 mA, V_S = 30 V	-	-	252.6	213.3	229.4	13.0
	I_R = 1.8 mA, V_S = 30 V	-	-	240.9	192.0	213.6	14.8
	I_R = 11.3 mA, V_S = 30 V	-	-	174.6	146.8	121.8	14.9
	I_R = 1.8 mA, V_S = 9 V	-	-	243.0	190.8	214.6	15.2
	I_R = 11.3 mA, V_S = 9 V	-	-	179.8	124.6	150.4	15.7
	I_R = 1.8 mA, V_S = 40 V	-	-	239.6	189.2	212.3	15.0
	I_R = 11.3 mA, V_S = 40 V	-	-	173.6	120.4	145.8	15.0

Table 13-6. Summary of Temperature Stabilizer Measurements (LM199A). (Cont'd)

Parameters	Conditions	Limits Min	Limits Max	Data (13 Units) High	Low	Mean	Std. Dev.
Temperature stabilizer power dissipation T_A = 85°C (mW)	I_R = 0 mA V_S = 30 V	-	-	78.0	28.5	52.8	18.1
	I_R = 1.8 mA V_S = 30 V	-	-	65.7	20.7	41.3	18.0
	I_R = 11.3 mA V_S = 30 V	-	-	42.9	23.4	32.8	6.2
	I_R = 1.8 mA V_S = 9 V	-	-	67.2	14.4	41.6	19.1
	I_R = 11.3 mA V_S = 9 V	-	-	12.1	6.9	9.0	1.9
	I_R = 1.8 mA V_S = 40 V	-	-	64.8	28.0	43.8	14.7
	I_R = 11.3 mA V_S = 40 V	-	-	61.6	34.8	45.5	8.5
Temperature stabilizer power dissipation T_A = 125°C (mW)	I_R = 0 mA V_S = 30 V	-	-	25.5	20.2	22.7	1.7
	I_R = 1.8 mA V_S = 30 V	-	-	25.2	20.0	22.5	1.7
	I_R = 11.3 mA V_S = 30 V	-	-	51.1	32.3	41.7	6.1
	I_R = 1.8 mA V_S = 9 V	-	-	7.2	5.5	6.4	0.6
	I_R = 11.3 mA V_S = 9 V	-	-	14.2	8.8	11.5	1.8
	I_R = 1.8 mA V_S = 40 V	-	-	33.9	26.9	30.5	2.2
	I_R = 11.3 mA V_S = 40 V	-	-	70.9	44.3	57.7	8.4
Initial heater current (mA)	I_R = 0 mA V_S = 40 V	-	200	120	95	108.5	9.0

Table 13-7. MIL-M-38510/121 TABLE I Electrical performance characteristics for device types 01 & 02

Characteristics	Symbol	Conditions		Device Type	Limits Min	Limits Max	Units
Reference voltage	V_R	$0.5mA \leq I_R \leq 10mA$ $V_S = 30\ V$	$T_A=25^oC$	01	6.800	7.100	V
		$0.6mA \leq I_R \leq 15mA$	$T_A=25^oC$	02	6.70	7.20	
Reference voltage change with current	ΔV_R (current)	$0.5mA \leq I_R \leq 10mA$ $V_S = 30V$	$T_A=25^oC$	01	-9	9	mV
			$-55^oC \leq T_A \leq 125^oC$	01	-12	12	
		$0.6mA \leq I_R \leq 15mA$	$T_A=25^oC$	02	-14	14	
			$-55^oC \leq T_A \leq 125^oC$	02	-18	18	
Reference voltage temperature coefficient	$\Delta V_R/\Delta T$	$I_R=1.0mA$ $V_S = 30V$	$-55^oC \leq T_A \leq 85^oC$	01	-.5	.5	PPM °C
			$85^oC \leq T_A \leq 125^oC$	01	-10	10	
		$I_R=1.0mA$	$-55^oC \leq T_A \leq 125^oC$	02	-10	10	
Dynamic impedance	Z_D	$I_R=1mA$	$V_S=30V$; $T_A=25^oC$	01	0	1	ohms
		$e_i=.3V; f=400HZ$	$T_A=25^oC$	02	0	1	
Noise	N_O	$I_R=1mA$	$V_S=30V$; $T_A=25^oC$	01	0	20	uVrms
		BW=10Hz to 10kHz	$T_A=25^oC$	02	0	20	
		$I_R=1mA$	$V_S=30V$; $T_A=25^oC$	01	0	7	Vp-p
		BW=0.1Hz to 10Hz	$T_A=25^oC$	02	0	7	
Temperature stabilizer supply current	I_S	$9V \leq V_S \leq 40V$ $I_R=0mA$	$T_A=25^oC$	01	2.5	14	mA
			$T_A=-55^oC$	01	6.6	28	
Initial temperature stabilizer supply current	I_{SI}	$9V \leq V_S \leq 40V$ $I_R=0mA$	$T_A=25^oC$	01	-	200	

Table 13-7. MIL-M-38510/121 TABLE I Electrical performance characteristics for device types 01 & 02 (Cont'd)

Characteristics	Symbol	Conditions		Device Type	Limits Min	Limits Max	Units
Reference voltage temperature cycling hysteresis	ΔV_R (TEMP CYCLE)	I_R=1mA $-55^oC \leq T_A$ 125°C	V_S=30V	01	-10	10	mV
				02	- 1	1	mV
Reference voltage long term stability	$\Delta V_R/\Delta t$	I_R=1mA Δt = 1000 hrs	V_S=30V; T_A=25°C	01	-20	20	PPM
			T_A=25°C	02	-20	20	PPM
			T_A=45°C	02	-20	20	PPM

SECTION XIV

MIL-M-38510/128

PROGRAMMABLE PRECISION VOLTAGE REFERENCES

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SECTION XIV

MIL-M-38510/128

PROGRAMMABLE PRECISION VOLTAGE REFERENCES

14.1 Introduction

Precision voltage references were previously characterized on MIL-M-38510/124. These were two terminal devices and developed an output voltage of 6.95 Vdc. For many applications the users desire a precision voltage reference at 10 Vdc, 5 Vdc or some other level depending upon the system application. The different voltage levels could be established with an op amp circuit, however, this would result in additional temperature and time drift to the voltage reference. Programmable precision voltage references, now available in TO-99 packages, can be readily programmed with external jumpers and have received good user acceptance.

The AD584S and the AD584T are the two references selected for this slash sheet. These devices were selected by RADC, GEOS and members of the JC-41 Committee for characterization.

Table 14-1 lists the device types specified for this characterization.

Table 14-1. Device Types Specified.

Device Type	Generic Type	Manufacturer	Output Voltage	No. of Terminals
12801	AD584S	Analog Devices	10,7.5,5,2.5V	8
12802	AD584T	Analog Devices	10,7.5,5,2.5V	8

14.2 Description of Device Types

The AD584 is a monolithic silicon voltage reference circuit. A block diagram of the circuit is shown in Figure 14-1. The heart of this circuit is a high stability 1.215 volt bandgap reference which is connected to non-inverting input of a high gain differential input operational amplifier. The feedback for this amplifier is through a series of laser trimmed, on-chip, resistors with tracking temperature coefficients. These series resistors have binary relationships of 4 Kohms, 8 Kohms and 16 Kohms, and can be readily programmed with external jumpers to change the output reference voltage. The output reference voltage can be programmed for 10 volts, 7.5 volts, 5 volts or 2.5 volts through these use of external jumpers. In addition, the feedback resistor ratios can be adjusted, with external shunt resistors, to obtain any desired voltage such as 10.24 volts, 5.12 volts, etc. Extreme care must be taken when using external resistors in order a) not to draw excessive load current and b) to match the internal resistor negative T.C. values of less than 60 ppm/^{o}C.

The reference circuit can operate from a single power supply ranging from 4.5 volts to 30 volts. The input voltage must, at all times, be at least 2.5 volts greater than the output voltage. Under these conditions the unit can source a maximum of 5 mA load current over the temperature range $-55^{o}C < T_A < +125^{o}C$.

Another feature of these voltage reference devices is the ability to strobe the output on or off. The strobe input is designed to operate from an open collector TTL gate. When the output of the TTL gate is open, the output of the voltage reference is at its programmed voltage level. When the output of the TTL gate is low, the voltage reference is approximately zero volts.

14.3 Test Development

The devices chosen for these characterization were selected and approved by a joint decision of RADC, the JC-41 Committee and the Circuit Design Engineering activity of GEOS. The devices were obtained from Analog Devices for characterization and are listed in Table 14-2.

Table 14-2. Device Types Characterized

Device Type	S/N	Manufacturer	Date Code
12801	2826,2828,	Analog Devices	None
	2829,2830		None
	61,66		016
12802	2822-2825	Analog Devices	None
	201-206		020

Test Parameter Development

The test parameters were recommended by the manufacturer for this characterization. Additional characterization tests were performed by GEOS, such as 10 mA output current, zener mode output voltage and source impedance, regulation over the full temperature range, and strobe voltage low performance. Except for the transient test parameters, tests were performed at the standard $-55^{o}C$, $25^{o}C$ and $125^{o}C$ temperatures. In addition, the parts were characterized at $0^{o}C$ and at $70^{o}C$. Power and strobe turn-on settling time and output noise were measured at $25^{o}C$ only. A list of the electrical parameters tested during characterization in Table 14-3.

Table 14-3. Test Parameters for Characterization

Item No.	Symbol	Parameter
1	Icc	Quiescent current at Vin = 15 V, 40 V
2	Vout	Referenced output voltage
3	VRLINE	Line Regulation
4	VRLOAD	Load Regulation
5	DVout/Dt	Output voltage T.C.
6	IOS	Output short circuit current
7	No	Output Noise
8	DVo/Dt	Long term stability
9	ts (power)	Settling time (power up)
10	ts (strobe)	Settling time (strobe up)
11	Vz	Zener voltage
12	Zz	Zener impedance
13	Vout	Output voltage (strobe low)
14	V_STBON	Strobe voltage for delta Vo=-10mV
15	ION	Strobe current for V_{STBON}
16	V_STBOFF	Strobe voltage for Vo=+10mV
17	IOFF	Strobe current for V_{STBOFF}
18	IMAX	Maximum strobe current
19	IMIN	Minimum strobe current
20	VoSTB	Output voltage for V_{STB}=0.4 volts

Test Circuit Development

Except for output noise, long term stability, and settling time, all test data was obtained on the S3270 using a S3270 test adapter. A schematic of this adapter is shown in Figure 14-2. This adapter provides both the control circuitry via relays to establish the various operating test modes and the proper interface between the DUT and the S3270 measurement system.

The two relays, K1 and K2, are used to provide the jumpers for programming the output voltage to the nominal values of 10 volts, 7.5 volts, 5.0 volts and 2.5 volts. Relay K3 is used for the prupose of characterizing the current input to the strobe pin as the input strobe voltage is forced to values ranging from Vin to zero volts. These measurements were included for evaluation and characterization only. Relay K4 provides the means of converting the device from its normal operating mode to a simulated "zener mode" of operation. With relay K5 activated the input voltage and output voltage pins are connected together and the DUT behaves as a two terminal shunt voltage regulator. In order to insure precise measurement of the test parameters, measurement sense lines were connected directly to each pin of the DUT socket to be measured. This eliminated possible ground loops from affecting the accuracy of the measurement. To achieve accurate results,

an external Fluke 8100B Calibrator is used to provide the proper stimulus and a Fluke DMM 8502A is used to measure the output voltages. The S3270 controls these instruments via an IEEE buss.

Bench Test Development

Test circuits for output voltage settling time and output noise were developed using copper plated "brass-boards" in order to achieve good grounding and short wire lengths between the critical parts of the circuit. The schematics for the strobe up settling time, the power-up settling time, output white noise and output 1/f noise are shown in Figures 14-3 through 14-6, respectively.

Tester Correlation

Correlation was achieved by comparing the measurements taken with a bench type setup to the measurements taken with the S3270 setup. The measurements were taken on the same device in both setups. Since the measurements require an instrument with an accuracy 10X better than the parameter limits, the correlation limits are set at 20% of the parameter limit. The data for these measurements are presented in Table 14-4.

Initially some failures were noted in the attempt to correlate bench data. The voltage measurements in the "zener mode" did not correlate. Measurements made on the bench were found to be in error as a result of an out of tolerance resistor that is used to establish input current to the DUT. Also the output short circuit current to ground could not be correlated. The S3270 tester measured the current at the output of the DUT. For convenience, the bench set up measured the input current to the DUT. The difference is the DUT quiescent current. Full agreement between the S3270 test set up and the bench test set up was obtained when these measurement problems were corrected.

14.4 Test Results and Data

Data on the test and characterization parameters was obtained from measurements on the S3270 at -55°C, 0°C, 25°C, 70°C and 125°C. A summary of these test results is presented in Table 14-5 and illustrates the data distribution and test limits for both device types. Sample data sheets for the static test parameters are presented in Tables 14-6 and 14-7 for the AD584S and the AD584T, respectively. Also, a data sheet for the dynamic test paameters is presented in Table 14-8. Data was obtained for a range of input voltage from 12.5 volts to 40 volts, and for load currents that vary over a range from zero to 10 mA. In addition, the DUT's were tested for "zener mode" operation and for strobe line operation.

All of the devices met the specifications defined in the vendors catalog. However, several of the devices failed to meet the output voltage requirements with load currents of 10 mA at temperatures of 0°C

and -55°C; and, two devices marginally failed the line regulation requirement at -55°C. Also, nearly all of the devices failed the zener mode test at 125°C with input currents of 1 mA. In addition, output voltage failures were noted at -55°C and at 125°C for the AD584T voltage reference devices when the 25°C limits are used. None of these conditions are specified by the vendor. Finally bench tests showed marginal device type failures for "1/f" noise.

14.5 Discussion of Data

The summary data presented in Table 14-5 shows the distribution of data for each parameter with respect to the suggested limits. Since the AD584S and AD584T devices have many common test parameter limits, the data obtained for these parameters were combined for presentation in Table 14-5. The only exceptions to these common test parameter limits were output voltage tolerances and output voltage T.C. tolerances. The data for these parameters was summarized separately for each device type.

As Table 14-[illegible] shows, all of the specified static test parameter measurements, except for line regulation over the full temperature range, met the respective test limits. Two of the twenty devices tested failed the line regulation limits, marginally, at -55°C, and, since these failures were marginal, new test limits have been proposed.

Four devices of each type were checked for output noise. All of these devices failed the "1/f" output noise bench tests. An oscillograph of this failure is shown in Figure 14- . The maximum peak-to-peak voltage shown in this figure is approximately 75 u volts.

Although this noise signal exceeds the initially specified limits of 50 u volts, for a 10 volt dc output it represents output voltage variations of only 7.5 PPM. This is not excessive for a .1% accurate device with a 15 PPM/C° temperature coefficient.

"White" noise and settling time were also measured on these four devices. The power up (turn on) settling time measurements were within the limits specified by the vendor. However, neither "white" noise nor the strobe up settling time are specified by the vendor.

Data taken to measure "white" noise was consistently in the range of 110 to 120 Vrms. By assuming the accepted ratio of 6:1 between peak-to-peak and rms "white" noise measurements, the measured values have an equivalent peak-to-peak value of 720 u V_{p-p}. This is equivalent to 72 PPM maximum noise variations for a 10 volt d.c. reference.

Settling time measurements were made to determine the time for the device to settle to within ±.1% of the final output voltage value. Time measurements were made by initializing either the input power or the strobe line. Time measurement data taken on strobe-up settling time was

consistantly 2-3 times longer than that taken on power-up settling time. Strobe-up settling time measurements varied from 104 to 220 usec, whereas power-up settling time measurements vaired from 60 to 110 usec.

14.6 Slash Sheet Development

Test parameters for the voltage reference devices were recommended by the manufacturer. Some additional parameters, including a) line and load regulation over the full temperature range, b) output voltage with the strobe input voltage log, c) output "white" noise, d) settling time with initialization of the strobe input line and e) long term stability were added to Table I of the slash sheet. A copy of Table I is presented in Table 14-9.

14.7 Conclusions and Recommendations

The AD584T and AD584S device types meet the needs for a general purpose programmable voltage reference. Since the devices are only .1% accurate voltage references, they cannot be given an unqualified recommendation for use in 10 and 12-bit converter applications. GEOS recommends that the additional tests described in paragraph 14.6 be included in the slash sheet to insure interchangeability as more vendors decide to manufacture these devices.

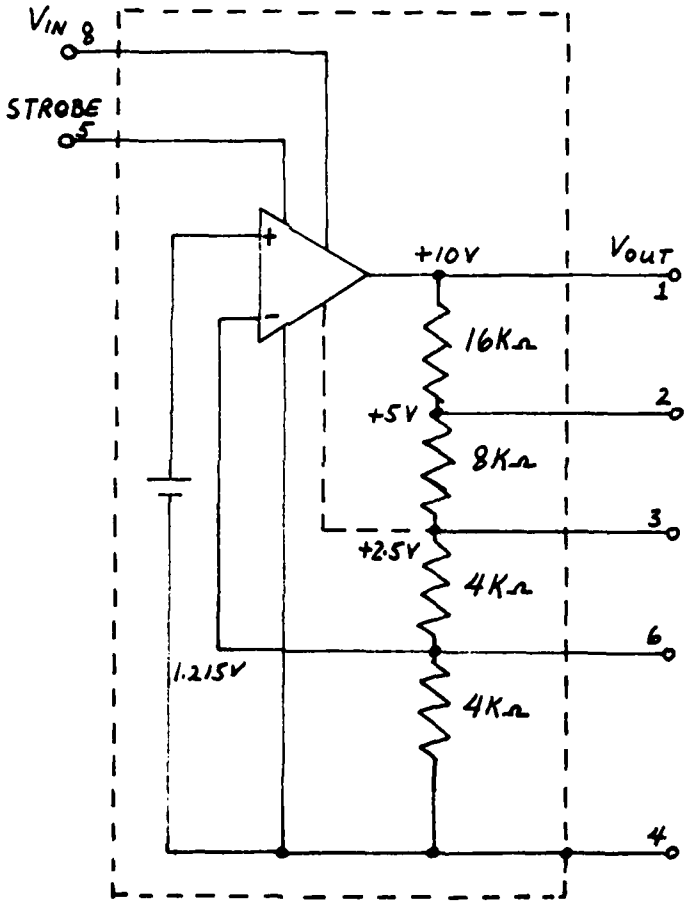


Figure 14-1. Block Diagram of AD584 Programmable Voltage Reference.

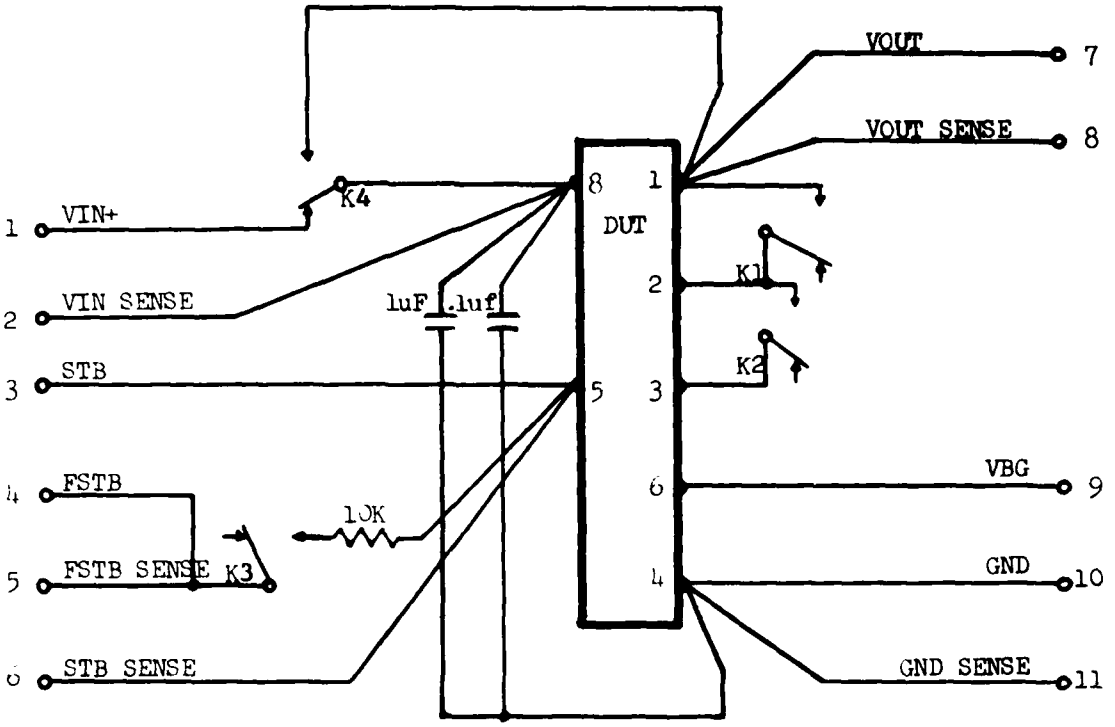


Figure 14-2. S3270 Test Circuit for Static Tests.

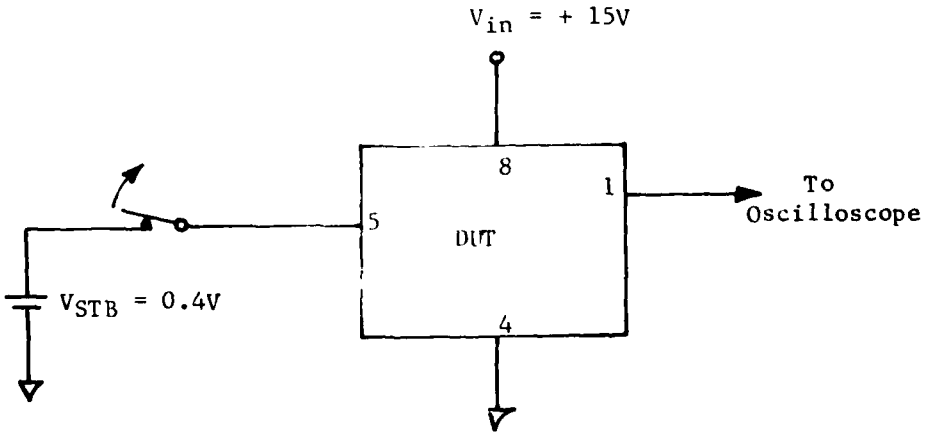
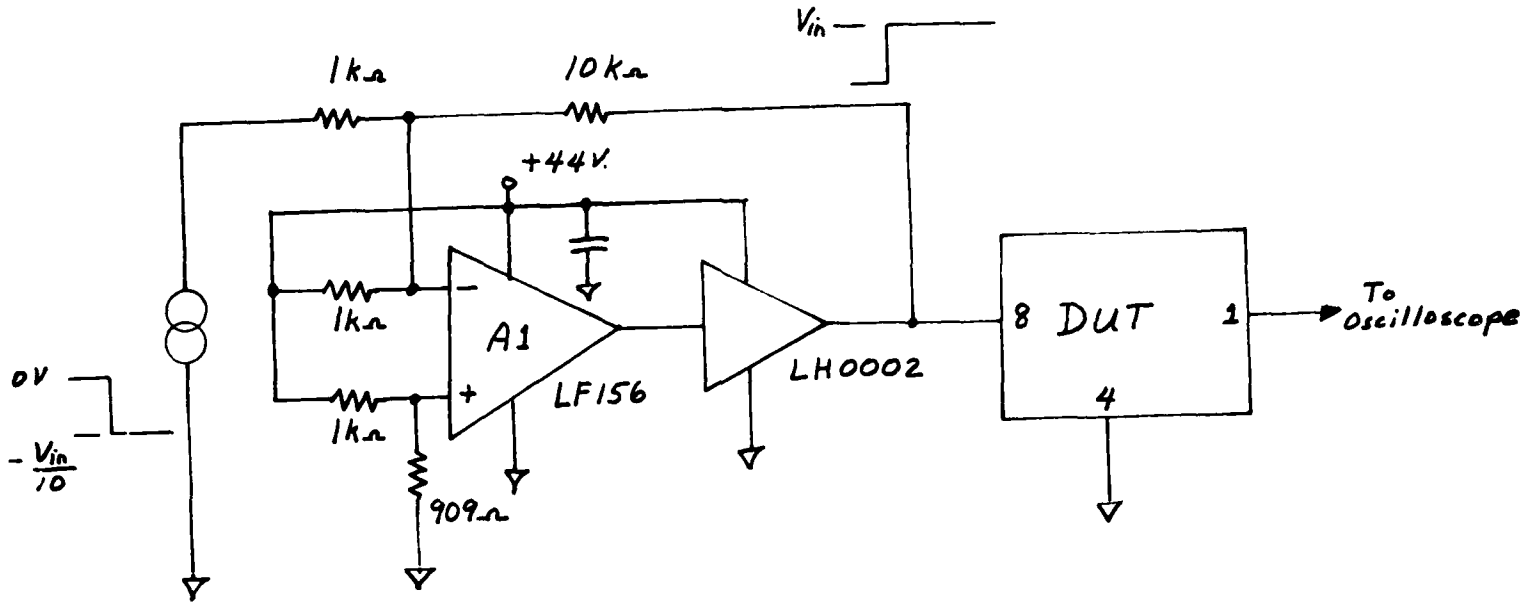


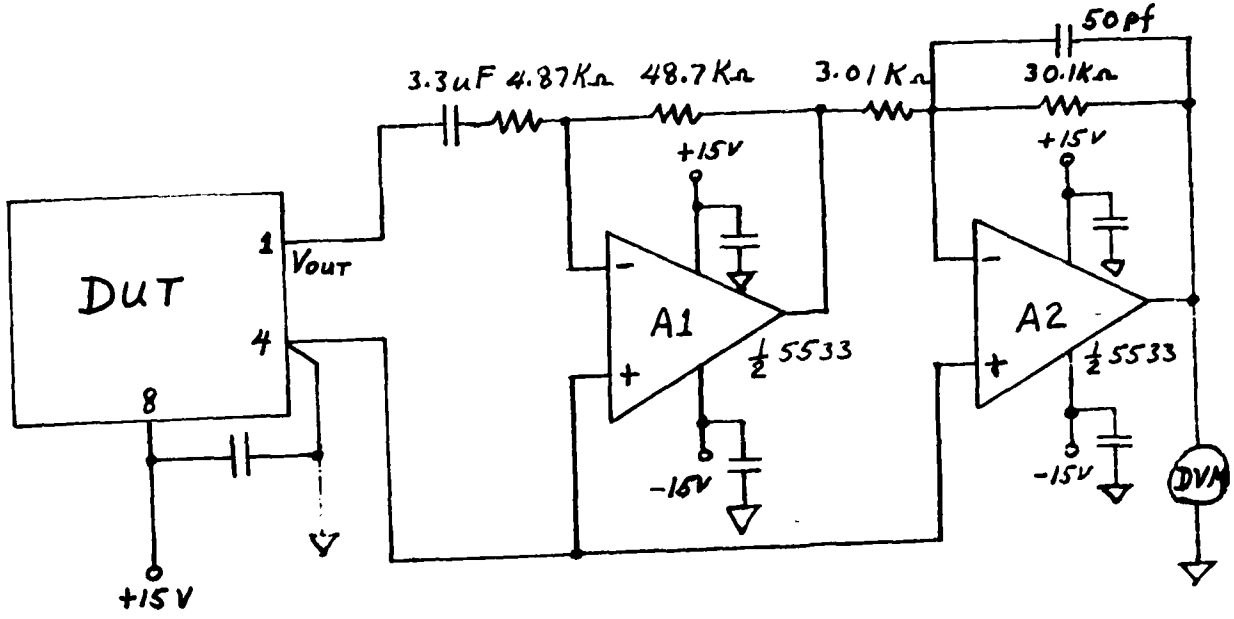
Figure 14-3. Strobe up Settling Time Test Circuit.



Notes: 1. The capacitor is 47 uF tantalum paralleled with .1 uF ceramic.

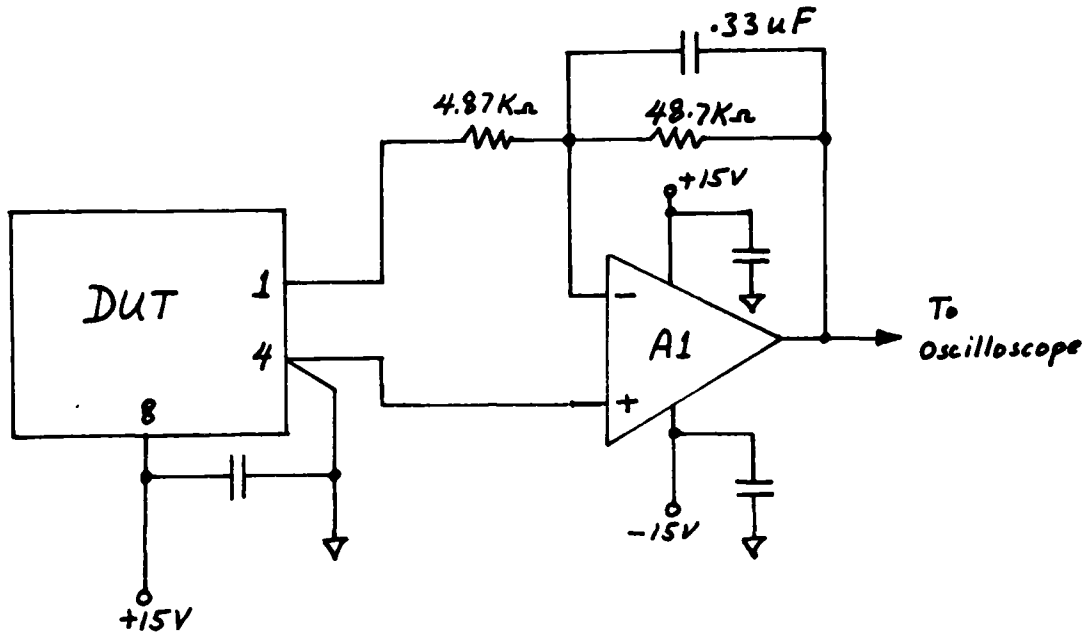
2. The oscilloscope pre-amp shall be a d-c voltage comparitor type.

Figure 14-4. Power up Settling Time Test Circuit.



Notes:
1. Unless otherwise stated, all capacitors are 47 uF tantalum paralleled with 0.1 uF ceramic.
2. The meter bandwidth shall be greater than 100 kHz.
3. A1 & A2 shall have a gain bandwidth product greater than 1 MHz and an output noise density less than 10 nV/ Hz.

Figure 14-5. Output "white" Noise Test Circuit.



Notes:
1. Unless otherwise stated, all capacitors are 47 uF tantalum paralleled with 0.1 uF ceramic.
2. The oscilloscope pre-amp shall be a d-c voltage comparitor type.
3. The oscilloscope time base shall be set to 1.0 Hz/cm and the horizontal display shall be 10 cm long.

Figure 14-6. Output "1/f" Noise Test Circuit.

Table 14-4. Correlation Data.

PARAMETER	BENCH DATA	S-3270 DATA	CORRELATION DATA	CORRELATION LIMITS
VOUT 1	9.9983V	9.99720V	1.1mV	6mV
VOUT 2	7.5041V	7.50333V	770uV	4.4mV
VOUT 3	4.9954V	4.99501V	390uV	3mV
VOUT 4	2.5002V	2.50028V	-80uV	1.5mV
ICC 1	774uA	774uA	0	
ICC 2	78uA	76uA	2uA	
ICC 3	774uA	772uA	2uA	
ICC 4	85uA	83.3uA	1.2uA	
IOS 1	-11.7mA	-11.85mA	-150uA	
IOS 2	23.5mA	24.5mA	-1mA	
VRL 1	9.9983V	9.99709V	1.21mV	6mV
VRL 2	9.9969V	9.99584V	1.06mV	6mV
VRL 3	7.5041V	7.50326V	840uV	4.4mV
VRL 4	7.5028V	7.50205V	750uV	4.4mV
VRL 5	4.9954V	4.99495V	450uV	3mV
VRL 6	4.9950V	4.99455V	450uV	3mV
VRL 7	2.5002V	2.50027V	-70uV	1.5mV
VRL 8	2.5001V	2.50007V	30uV	1.5mV
VRL 9	9.9958V	9.99457V	1.23mV	6mV
VRL 10	7.5015V	7.50083V	670uV	4.4mV
VRL 11	4.9945V	4.99422V	280uV	3mV
VRL 12	2.5000V	2.49989V	110uV	1.5mV
VRLI 1	9.9986V	9.99708V	1.52mV	6mV
VRLI 2	9.9990V	9.99761V	1.39mV	6mV
VRLI 3	9.9983V	9.99700V	1.3mV	6mV
VZ 1	9.9974V	9.99712V	280uV	6mV
VZ 2	7.5033V	7.50324V	60uV	4.4mV
VZ 3	4.9948V	4.99483V	-30uV	3mV
VZ 4	9.9970V	9.99855V	-1.55mV	6mV

Table 14-4. Correlation Data. (cont'd)

PARAMETER	BENCH DATA	S-3270 DATA	CORRELATION DATA	CORRELATION LIMITS
VZ 5	7.5035V	7.50462V	-1.12mV	4.4mV
VZ 6	4.9951V	4.99567V	-570uV	3mV
USTBON	10.68	10.2350V	445mV	
ION	-108uA	-109.5uA	-1.5uA	
VSTBOF	490mV	475mA	15mA	
IOFF	-73.3uA	-73.5uA	0.2uA	

TABLE 14-5. AD584S & AD584T Data Distribution and Limits

PARAMETER ($-55^{\circ}C \leq TA \leq 125^{\circ}C$)		* [//DATA//] * LL<----LIMIT----->HL	Unit
Quiescent current Vin=40V;	TA=25°C	* [///] * 0 < . . . . . >1.0	mA
Quiescent current Vin=15V;	TA=25°C	* [//] * 0 < . . . . . >1.0	mA
Output voltage AD584S,TA=25°C;	Vo= 10V +/-.3%	* [/] * 9.97 < . . . . . > 10.03	V
	Vo=7.5V +/-.3%	* [/] * 7.478 < . . . . . > 7.522	V
	Vo=5.0V +/-.3%	* [//] * 4.985 < . . . . . > 5.015	V
	Vo=2.5V +/-.3%	* [/] * 2.4925 < . . . . . > 2.5075	V
Output voltage AD584T,TA=25°C;	Vo= 10V +/-.1%	* [///] * 9.99 < . . . > 10.01	V
	Vo=7.5V +/-.1%	*[/////]* 7.492 < . . . > 7.508	V
	Vo=5.0V +/-.1%	*[///] * 4.994 < . . . > 5.006	V
	Vo=2.5V +/-.1%	* [//] * 2.4965 < . . . > 2.5035	V
Line regulation TA=25°C;	15V $\leq$Vin $\leq$30V	* [/] * -.002 < . 0 . > .002	%/V
	12.5V $\leq$Vin $\leq$15V	* [/] * -.005 < . 0 . > .005	%/V
Line regulation	(See Note 1) 15V $\leq$Vin $\leq$30V	[] [*/////] * -.002 < . 0 . > .002	%/V
	(See Note 2) 12.5V $\leq$Vin $\leq$15V	* [///]* [] -.005 < . 0 . > .005	%/V

TABLE 14-5. AD584S & AD584T Data Distribution and Limits (cont'd.)

PARAMETER (-55°C ≤TA ≤125°C)		* [//DATA//] * LL<----LIMIT----->HL	Unit
Load regulation (All Vo values)		* [//]*	
-5mA <TA <0mA;	TA=25°C	-50 < . . 0 . . > 50	PPM/mA
	-55°C ≤TA ≤125°C	* [/////]* -50 < . . 0 . . > 50	PPM/mA
Output voltage		*[//] *	
VSTB=.4V;	TA=25°C	0 < . . . . > 1.0	V
Output short circuit current		*[] *	
Vin=15V;	Vo=10V	0 < . . . . > 30	mA
Output voltage T.C. (AD584S)		* [//////] *	
(All Vo)	-55°C ≤TA ≤125°C	-30 < . . 0 . . > 30	PPM/C°
Output voltage T.C. (AD584T)		*[////] *	
Vo=10,7.5,5V;	-55°C ≤TA ≤125°C	-15 < . 0 . > 15	PPM/C°
		* [////]*	
Vo=2.5V;	-55°C ≤TA ≤125°C	-20 < . 0 . > 20	PPM/C°
Output noise (See Note 3)			
Vo=10V;	TA=25°C	* [////]	
	.1Hz ≤BW ≤10Hz	0 < . . . . . > 150	uVp-p
		* []	
	10Hz ≤BW ≤100KHz	0 < . . . . . > 150	uVrms
Settling time (Power up)		* [] *	
Vin=15V;	TA=25°C	0 < . . . . > 500	usec
Settling time (Strobe up)		* [///]	
Vin=15V;	TA=25°C	0 < . . . . > 500	usec

NOTE 1: Serial number 2822 and 2828 had VRLINE values of -.0023 %/V and -.0049 %/V, respectively.

2: Serial number 2822 had a VRLINE of .0091 %/V.

3: Upper limits for the output noise are being negotiated.

Table 14-6.

AD534S DEVICE TYPE-01 PIN PROGRAMMABLE PRECISION VOLTAGE REFERENCE

S/N=2826 ;DATE=02 OCT 80

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	-55C	0C	25C	70C	125C	HI-LIMIT	UNITS
VOUT1	VIN=15V IO=0MA	VO=10V STB=1	1	9.97000	9.99257	9.99679	9.99720	9.99129	9.98282	10.0300	V
VOUT2	VIN=15V IO=0MA	VO=7.5V STB=1	1	7.47800	7.49890	7.50279	7.50333	7.49925	7.49324	7.52200	V
VOUT3	VIN=15V IO=0MA	VO=5V STB=1	1	4.98500	4.99054	4.99437	4.99501	4.99282	4.98926	5.01500	V
VOUT4	VIN=15V IO=0MA	VO=2.5V STB=1	1	2.49250	2.49604	2.49956	2.50028	2.49979	2.49862	2.50750	V
ICC1	VIN=15V IO=0MA	VO=10V STB=1	8	0.000	641.5U	736.0U	774.0U	831.5U	928.0U	1.000M	A
ICC2	VIN=15V IO=0MA	VO=10V STB=0	8	0.000	149.0U	91.00U	76.00U	55.35U	40.15U	1.000M	A
ICC3	VIN=40V IO=0MA	VO=10V STB=1	8	0.000	647.0U	736.0U	772.0U	844.0U	930.0U	1.000M	A
ICC4	VIN=40V IO=0MA	VO=10V STB=0	8	0.000	160.0U	99.00U	83.85U	62.20U	45.40U	1.000M	A
IOS1	VIN=15V IO=0MA	VO=0V STB=1	1	-30.00M	-12.45M	-12.40M	-11.85M	-10.50M	-9.000M	0.000	A
IOS2	VIN=15V IO=0MA	VO=15V STB=1	1	0.000	26.80M	25.20M	24.50M	23.05M	20.90M	30.00M	A
VRL1	VIN=15V IO=0MA	VO=10V STB=1	1	9.97000	9.99244	9.99680	9.99709	9.99132	9.98250	10.0300	V
VRL2	VIN=15V IO=-5MA	VO=10V STB=1	1	9.97000	9.99162	9.99565	9.99584	9.98981	9.98078	10.0300	V
VRL3	VIN=15V IO=0MA	VO=7.5V STB=1	1	7.47800	7.49902	7.50281	7.50326	7.49920	7.49303	7.52200	V
VRL4	VIN=15V IO=-5MA	VO=7.5V STB=1	1	7.47800	7.49819	7.50170	7.50205	7.49771	7.49127	7.52200	V
VRL5	VIN=15V IO=0MA	VO=5V STB=1	1	4.98500	4.99058	4.99436	4.99495	4.99282	4.98911	5.01500	V

Table 14-6.

AD534S DEVICE TYPE-01 PIN PROGRAMMABLE PRECISION VOLTAGE REFERENCE (cont'd).
S/N=2826 ;DATE=02 OCT 80

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	-55C	0C	25C	70C	125C	HI-LIMIT	UNITS
VRL6	VIN=15V IO=-5MA	VC=5V STB=1	1	4.98500	4.99041	4.99404	4.99455	4.99236	4.98860	5.01500	V
VRL7	VIN=15V IO=0MA	VO=2.5V STB=1	1	2.49250	2.49607	2.49956	2.50027	2.49979	2.49856	2.50750	V
VRL8	VIN=15V IO=-5MA	VO=2.5V STB=1	1	2.49250	2.49608	2.49942	2.50007	2.49951	2.49830	2.50750	V
VRL9	VIN=15V IO=-10MA	VO=10V STB=1	1	9.97000	1.66571%	1.51790%	9.99457	9.98841	9.97898	10.0300	V
VRL10	VIN=15V IO=-10MA	VO=7.5V STB=1	1	7.47800	1.65415%	7.50056	7.50083	7.49628	7.48957	7.52200	V
VRL11	VIN=15V IO=-10MA	VO=5V STB=1	1	4.98500	1.63047%	4.99373	4.99422	4.99184	4.98807	5.01500	V
VRL12	VIN=15V IO=-10MA	VO=2.5V STB=1	1	2.49250	2.49615	2.49929	2.49989	2.49925	2.49801	2.50750	V
VRLI1	VIN=15V IO=0MA	VO=10V STB=1	1	9.97000	9.99247	9.99676	9.99708	9.99127	9.98233	10.0300	V
VRLI2	VIN=30V IO=0MA	VO=10V STB=1	1	9.97000	9.99253	9.99729	9.99761	9.99176	9.98297	10.0300	V
VRLI3	VIN=12.5V IO=0MA	VO=10V STB=1	1	9.97000	9.99238	9.99669	9.99700	9.99124	9.98233	10.0300	V
VRLI4	VIN=40V IO=0MA	VO=10V STB=1	1	9.97000	9.99249	9.99750	9.99783	9.99202	9.98315	10.0300	V
VZ1	VIN=10V IIN=1MA	VO=10V STB=1	1	9.97000	9.99295	9.99683	9.99712	9.99050	8.88636%	10.0300	V
VZ2	VIN=7.5V IIN=1MA	VO=7.5V STB=1	1	7.47800	7.49935	7.50274	7.50324	7.49869	6.76528%	7.52200	V
VZ3	VIN=5V IIN=1MA	VO=5V STB=1	1	4.98500	4.99038	4.99422	4.99483	4.99230	4.58728%	5.01500	V
VZ4	VIN=10V IIN=4MA	VO=10V STB=1	1	9.97000	9.99380	9.99799	9.99855	9.99331	9.98419	10.0300	V

Table 14-6.

AD584S DEVICE TYPE-01 PIN PROGRAMMABLE PRECISION VOLTAGE REFERENCE. (cont'd)
S/N=2826 ;DATE=02 OCT 80

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	-55C	0C	25C	70C	125C	HI-LIMIT	UNITS
VZ5	VIN=7.5V IIN=4MA	VO=7.5V STB=1	1	7.47800	7.50027	7.50398	7.50462	7.50120	7.49490	7.52800	V
VZ6	VIN=5V IIN=4MA	VO=5V STB=1	1	4.98500	4.99095	4.99489	4.99567	4.99389	4.99030	5.01500	V
VSTBON	VIN=15V IO=0MA	VO=10V STB=1	5	9.00000	10.2350	10.2350	10.2350	10.2350	10.2350	11.0000	V
ION	VIN=15V IO=0MA	VO=10V STB=1	-	-500.0U	-74.50U	-98.00U	-109.5U	-127.5U	-146.0U	100.0U	A
VSTBOF	VIN=15V IO=0MA	VO=10V STB=1	5	0.00000	680.000M	545.000M	475.000M	355.000M	210.000M	1.00000	V
IOFF	VIN=15V IO=0MA	VO=10V STB=1	-	-500.0U	-132.5U	-84.00U	-73.50U	-51.00U	-38.00U	100.0U	A
IMAX	VIN=15V IO=0MA	VO=10V STB=1	-	-500.0U	-60.50U	-31.50U	-60.50U	-31.50U	-31.50U	100.0U	A
IMIN	VIN=15V IO=0MA	VO=10V STB=1	-	-500.0U	-126.5U	-126.5U	-70.50U	-126.5U	-126.5U	100.0U	A
VOSTB	VIN=15V F=0.4V	VO=10V STB=1	1	0.00000	4.73400M	36.2780M	78.9140M	169.635M	284.220M	1.00000	V

Table 14-6.

AD584S DEVICE TYPE - 01 PIN PROGRAMMABLE PRECISION VOLTAGE REFERENCE (cont'd)

S/N = 2826

SYMBOL	TEST CONDITIONS		LO-LIMIT	-55°C	0°C	25°C	70°C	125°C	HI-LIMIT	UNITS
VRLINE	VO = 10V STB = OPEN IL = 0mA	12.5V < VIN < 15V	-.005	0.0004	0.0003	0.0003	0.0001	0	+.005	%/V
		15V < VIN < 30V	-.002	0	0.0004	0.0004	0.0003	0.0004	+.002	
		15V < VIN < 40V		0	0.0003	0.0003	0.0003	0.0003		
VRLOAD	VIN = 15V STB = OPEN -5mA < IL < 0mA	VO = 10V	-50	16.4	23.0	25.0	30.2	34.5	+50	PPM/mA
		VO = 7.5V		22.1	29.6	32.3	39.7	47.0		
		VO = 5V		6.8	12.8	16.3	18.4	20.5		
		VO = 2.5V		-0.8	11.2	16.0	22.4	20.8		
	VIN = 15V STB = OPEN -10mA < IL < 0mA	VO = 10V		*	*	25.2	29.1	35.3		
		VO = 7.5V		*	30.0	32.4	38.9	46.2		
		VO = 5V		*	12.6	14.6	19.6	20.8		
		VO = 2.5V		-3.2	10.8	15.2	21.6	22.0		
** DV_{OUT}/DT	VIN = 15V STB = OPEN IL = 0mA	VO = 10V	-30	-5.8	-7.4	-	-11.2	-21.2	+30	PPM/°C
		VO = 7.5V		-1.6	-2.9	-	-5.1	-11.5		
		VO = 5V		13.1	12.1	-	9.7	4.4		
		VO = 2.5V		14.4	13.4	-	11.5	6.6		
Zz	VIN = 15V STB = OPEN 1mA < IIN < 4mA	VO = 10V	-	0.283	0.387	0.477	0.937	***	1.0	OHM
		VO = 7.5V		0.307	0.413	0.460	0.837	***		
		VO = 5V		0.190	0.223	0.280	0.530	***		

* OVER 100 PPM/mA ** DV_{OUT}/DT FROM 25°C *** OVER 50 OHMs

AD-A108 247 GENERAL ELECTRIC CO PITTSFIELD MA ELECTRONIC SYSTEMS DIV F/G 9/5
ELECTRICAL CHARACTERIZATION AND SPECIFICATION OF SPECIAL PURPOS--ETC(U)
JUN 81 J S KULPINSKI, L CARROZZA, T SIMONSEN F30602-78-C-0195

UNCLASSIFIED RADC-TR-81-74 NL

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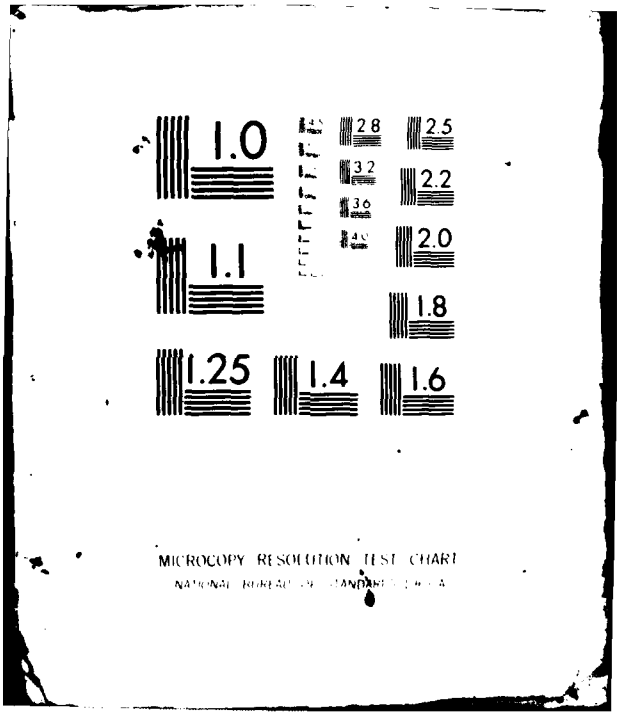
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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

Table 14-7.

AD584T PIN PROGRAMMABLE PRECISION VOLTAGE REFERENCE
S/N=2825 ;DATE=03 OCT 80

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	-55C	0C	25C	70C	125C	HI-LIMIT	UNITS
VOUT1	VIN=15V IO=0MA	VO=10V STB=1	1	9.99000	9.99554	10.0010	10.0036	10.0031	10.0051	10.0100	V
VOUT2	VIN=15V IO=0MA	VO=7.5V STB=1	1	7.49200	7.50013	7.50473	7.50672	7.50654	7.50830*	7.50800	V
VOUT3	VIN=15V IO=0MA	VO=5V STB=1	1	4.99400	4.99359*	4.99680	4.99814	4.99806	4.99935	5.00600	V
VOUT4	VIN=15V IO=0MA	VO=2.5V STB=1	1	2.49650	2.49759	2.49989	2.50067	2.50085	2.50176	2.50350	V
ICC1	VIN=15V IO=0MA	VO=10V STB=1	8	0.000	649.5U	738.0U	766.0U	828.0U	895.5U	1.000M	A
ICC2	VIN=15V IO=0MA	VO=10V STB=0	8	0.000	72.00U	46.05U	40.05U	30.55U	23.25U	1.000M	A
ICC3	VIN=40V IO=0MA	VO=10V STB=1	8	0.000	656.0U	737.0U	764.0U	823.0U	895.0U	1.000M	A
ICC4	VIN=40V IO=0MA	VO=10V STB=0	8	0.000	73.40U	47.15U	41.40U	31.95U	24.35U	1.000M	A
IOS1	VIN=15V IO=0MA	VO=0V STB=1	1	-30.00M	-13.80M	-13.10M	-12.50M	-11.25M	-9.850M	0.000	A
IOS2	VIN=15V IO=0MA	VO=15V STB=1	1	0.000	27.30M	25.30M	24.65M	23.20M	21.10M	30.00M	A
VRL1	VIN=15V IO=0MA	VO=10V STB=1	1	9.99000	9.99484	10.0010	10.0035	10.0031	10.0052	10.0100	V
VRL2	VIN=15V IO=-5MA	VO=10V STB=1	1	9.99000	9.99325	9.99991	10.0024	10.0018	10.0038	10.0100	V
VRL3	VIN=15V IO=0MA	VO=7.5V STB=1	1	7.49200	7.49871	7.50468	7.50670	7.50656	7.50842*	7.50800	V
VRL4	VIN=15V IO=-5MA	VO=7.5V STB=1	1	7.49200	7.49806	7.50361	7.50553	7.50520	7.50699	7.50800	V
VRL5	VIN=15V IO=0MA	VO=5V STB=1	1	4.99400	4.99335*	4.99676	4.99812	4.99807	4.99946	5.00600	V

Table 14-7.

AD534T PIN PROGRAMMABLE PRECISION VOLTAGE REFERENCE (cont'd)
S/N=2825 ;DATE=03 OCT 80

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	-55C	0C	25C	70C	125C	HI-LIMIT	UNITS
VZS	VIN=7.5V IIN=4MA	VO=7.5V STB=1	1	7.49200	7.49953	7.50595	7.50825M	7.50865M	7.51142M	7.50800	V
VZ6	VIN=5V IIN=4MA	VO=5V STB=1	1	4.99400	4.99374M	4.99745	4.99902	4.99938	5.00141	5.00600	V
VSTBON	VIN=15V IO=0MA	VO=10V STB=1	5	9.00000	10.2350	10.2350	10.2350	10.2350	10.2350	11.0000	V
ION	VIN=15V IO=0MA	VO=10V STB=1	-	-500.0U	-86.00U	-106.5U	-111.5U	-127.0U	-151.5U	100.0U	A
VSTROF	VIN=15V IO=0MA	VO=10V STB=1	5	0.00000	660.000M	510.000M	455.000M	340.000M	215.000M	1.00000	V
IOFF	VIN=15V IO=0MA	VO=10V STB=1	-	-500.0U	-61.50U	-41.50U	-35.50U	-31.00U	-24.00U	100.0U	A
IMAX	VIN=15V IO=0MA	VO=10V STB=1	-	-500.0U	-30.00U	-16.00U	-30.00U	-16.00U	-16.00U	100.0U	A
IMIN	VIN=15V IO=0MA	VO=10V STB=1	-	-500.0J	-66.00U	-66.00U	-39.50U	-66.00U	-66.00U	100.0U	A
VOSTB	VIN=15V F=0.4V	VO=10V STB=1	1	0.00000	530.000U	209.000U	1.72900M	32.2590M	114.262M	1.00000	V

Table 14-7.

AD584T PIN PROGRAMMABLE PRECISION VOLTAGE REFERENCE (cont'd)
S/N=2825 ;DATE=03 OCT 80

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	-55C	0C	25C	70C	125C	HI-LIMIT	UNITS
VRL6	VIN=15V IO=-5MA	VO=5V STB=1	1	4.99400	4.99313*	4.99646	4.99778	4.99768	4.99888	5.00600	V
VRL7	VIN=15V IO=0MA	VO=2.5V STB=1	1	2.49650	2.49753	2.49986	2.50067	2.50087	2.50183	2.50350	V
VRL8	VIN=15V IO=-5MA	VO=2.5V STB=1	1	2.49650	2.49749	2.49978	2.50047	2.50063	2.50161	2.50350	V
VRL9	VIN=15V IO=-10MA	VO=10V STB=1	1	9.99000	1.72556*	9.99882	10.0012	10.0004	10.0025	10.0100	V
VRL10	VIN=15V IO=-10MA	VO=7.5V STB=1	1	7.49200	7.49672	7.50252	7.50435	7.50386	7.50563	7.50800	V
VRL11	VIN=15V IO=-10MA	VO=5V STB=1	1	4.99400	4.99303*	4.99616	4.99744	4.99728	4.99878	5.00600	V
VRL12	VIN=15V IO=-10MA	VO=2.5V STB=1	1	2.49650	2.49747	2.49953	2.50028	2.50039	2.50142	2.50350	V
VRLI1	VIN=15V IO=0MA	VO=10V STB=1	1	9.99000	9.99300	10.0009	10.0035	10.0031	10.0055	10.0100	V
VRLI2	VIN=30V IO=0MA	VO=10V STB=1	1	9.99000	9.99289	10.0007	10.0032	10.0028	10.0052	10.0100	V
VRLI3	VIN=12.5V IO=0MA	VO=10V STB=1	1	9.99000	9.99306	10.0009	10.0036	10.0032	10.0056	10.0100	V
VRLI4	VIN=40V IO=0MA	VO=10V STB=1	1	9.99000	9.99318	10.0006	10.0031	10.0026	10.0051	10.0100	V
VZ1	VIN=10V IIN=1MA	VO=10V STB=1	1	9.99000	9.99361	10.0012	10.0039	10.0032	9.97749*	10.0100	V
VZ2	VIN=7.5V IIN=1MA	VO=7.5V STB=1	1	7.49200	7.49894	7.50490	7.50704	7.50681	7.48845*	7.50800	V
VZ3	VIN=5V IIN=1MA	VO=5V STB=1	1	4.99400	4.99337*	4.99686	4.99831	4.99822	4.98655*	5.00600	V
VZ4	VIN=10V IIN=4MA	VO=10V STB=1	1	9.99000	9.99434	10.0021	10.0050	10.0051	10.0083	10.0100	V

Table 14-7.

AD584T DEVICE TYPE - 02 PIN PROGRAMMABLE PRECISION VOLTAGE REFERENCE (cont'd)
S/N = 2825

SYMBOL	TEST CONDITIONS		LO-LIMIT	-55°C	0°C	25°C	70°C	125°C	HI-LIMIT	UNITS
VRLINE	VO = 10V STB = OPEN IL = 0mA	12.5V < VIN < 15V	-.005	-0.0002	-0.0001	-0.0003	-0.0005	-0.0005	+.005	%/V
		15V < VIN < 30V	-.002	-0.0001	-0.0002	-0.0002	-0.0002	-0.0002	+.002	
		15V < VIN < 40V		0.0001	-0.0001	-0.0002	-0.0002	-0.0002		
VRLOAD	VIN = 15V STB = OPEN -5mA < IL < 0mA	VO = 10V	-50	31.8	21.0	22.6	25.8	28.4	+50	PPM/mA
		VO = 7.5V		17.3	28.5	31.2	36.2	38.1		
		VO = 5V		8.8	12.0	13.6	15.6	15.2		
		VO = 2.5V		3.2	12.8	16.0	19.2	17.6		
	VIN = 15V STB = OPEN -10mA < IL < 0mA	VO = 10V		*	21.4	23.0	26.3	27.1		
		VO = 7.5V		26.5	28.8	31.3	36.0	37.2		
		VO = 5V		6.4	12.0	13.6	15.8	13.6		
		VO = 2.5V		2.4	13.2	15.6	19.2	16.4		
** DV_{OUT}/DT	VIN = 15V STB = OPEN IL = 0mA	VO = 10V	-15	-10.0	-11.0	-	-11.4	-15.4	+15	PPM/°C
		VO = 7.5V		-10.2	-10.6	-	-10.7	-12.5		
		VO = 5V		1.1	0.5	-	0.4	-1.6		
		VO = 2.5V	-20	-1.5	-2.1	-	-2.4	-4.4	+20	
Zz	VIN = 15V STB = OPEN 1mA < IIN < 4mA	VO = 10V	-	0.243	0.330	0.383	0.637	10.280	1.0	OHM
		VO = 7.5V		0.197	0.350	0.403	0.613	7.657		
		VO = 5V		0.123	0.197	0.237	0.387	4.953		

* OVER 100 PPM/mA ** DV_{OUT}/DT FROM 25°C *** OVER 50 OHMs

TABLE 14-8. DYNAMIC BENCH TEST MEASUREMENTS (T_A = 25°C)

Test Parameter	Conditions	Limits	Generic Type: AD 584T Serial Number 2822	2823	2824	2825	AD 584S Serial Number 2826	2828	2829	2830	Unit
Output Noise	V_{in} = 15V; V_o = 10V I_L = 0 mA										
	0.1 Hz BW 10Hz	Later	75	75	75	75	100	125	140	125	uV_{p-p}
	10 Hz BW 100Hz	Later	.12	.12	.12	.12	.11	.11	.11	.11	mV_{rms}
Settling Time (Power up)	V_{in} = 15V; V_o = 10V I_L = 0 mA	500	110	99	104	100	77	66.5	74	60	usec
	I_L = 5 mA	(max)	104	94	97	96	71	61.5	68	56	"
	V_{in} = 40V; Vo = 10V I_L = 0 mA	"	280	240	250	235	230	188	200	170	"
	I_L = -5mA	"	250	235	245	230	218	185	188	163	"
Settling Time (Strobe up)	V_{in} = 15V; V_o = 10V I_L = 0 mA	"	220	215	210	215	143	152	119	104	"
	I_L = -5mA	"	273	260	263	283	165	188	126	111	"
	V_{in} = 40V; V_o = 10V I_L = 0 mA	"	343	340	330	328	245	220	188	170	"
	I_L = -5mA	"	385	365	370	375	263	253	198	178	"

Table 14-9. Electrical performance characteristics for device types 01&02

Characteristic	Symbol	Conditions:	Device Type	Limits Min	Limits Max	Unit
Quiescent current	ICC	Vin=38V ; TA=25°C Vo= 10V 1/	01,02	0	1.0	mA
		TA=25°C Vo= 10V	01,02	0	1.0	mA
Output voltage	VOUT	TA=25°C Vo= 10V	01	9.97	10.03	V
		Vo= 10V	02	9.99	10.01	V
		Vo=7.5V	01	7.478	7.522	V
		Vo=7.5V	02	7.492	7.508	V
		Vo=5.0V	01	4.985	5.015	V
		Vo=5.0V	02	4.994	5.006	V
		Vo=2.5V	01	2.4925	2.5075	V
		Vo=2.5V	02	2.4965	2.5035	V
Line regulation	VRLINE	12.5V <Vin <15V; TA=25°C Vo= 10V,7.5V,5.0V,2.5V	01,02	-.005	+.005	%/V
		15V <Vin <30V; TA=25°C Vo= 10V	01,02	-.002	+.002	%/V
		12.5V <Vin <15V Vo= 10V,7.5V,5.0V,2.5V	01,02	-.007	+.007	%/V
		15V <Vin <30V Vo= 10V	01,02	-.005	+.005	%/V
Load regulation	VRLOAD	-5mA <IL <0mA ; TA=25°C Vo= 10V,7.5V,5.0V,2.5V	01,02	-50	+50	PPM /mA
		-5mA <IL <0mA Vo= 10V,7.5V,5.0V,2.5V	01,02	-75	+75	PPM /mA
Output short circuit current	IOS	Vo= 10V	10,02	-	30	mA
Output voltage (Strobe low)	VOUT	Vo= 10V ; Vstb=0.4V	01,02	-	1	V

Table IV-9. Electrical performance characteristics for device types 01&02 (Continued)

Characteristic	Symbol	Conditions:	Device Type	Limits Min	Limits Max	Unit
Output voltage temperature coefficient	DVOUT /DT	-55°C <TA <25°C 25°C <TA <125°C Vo= 10V,7.5V,5.0V,2.5V Vo= 10V,7.5V,5.0V Vo=2.5V	01 02 02	-30 -15 -20	+30 +15 +20	PPM /Co
Output noise	No	Vo= 10V ; TA=25°C 0.1Hz <BW <10Hz 10Hz <BW <100Khz	01,02 01,02	-	50 150	uVp-p uVrms
Settling time to .1% of final value (Power up)	ts(p) (power)	Vo= 10V ; TA=25°C IL 0mA IL=-5mA	01,02 01,02	- -	500 500	usec usec
Settling time to .1% of final value (Strobe up)	ts(s) (strobe)	Vo= 10V ; TA=25°C IL=0mA IL=-5mA	01,02 01,02	- -	500 500	usec usec
Long term stability	DVOUT /Dt	Vo= 10V ; TA=25°C IL=0mA ; t=1000hrs	01,02	-	25	PPM /Khrs

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